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Numerical Simulation, Electrostatic and Physical Compact Modeling of C8-BTBT-C8 Organic Thin Film Transistor

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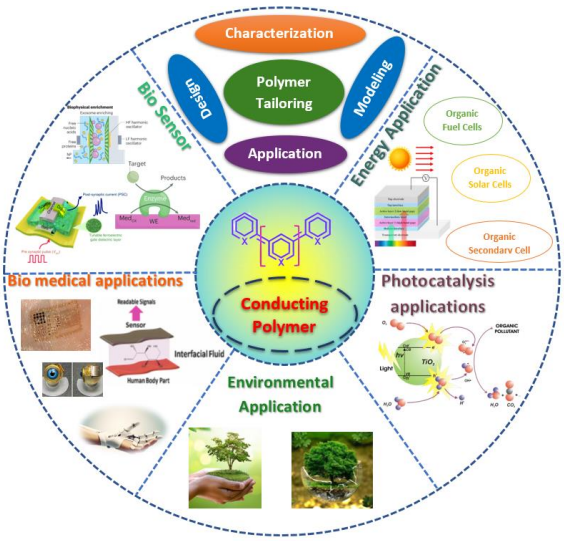
ABSTRACT

This paper presents numerical simulation and compact modeling of 2,7-Dioctyl {1} benzothieno {3,2-b}{1} benzothiophene (C8-BTBT-C8) organic semiconductor-based TFT. It shows the entire modeling process flow of this organic semiconductor (OSC) and tests the device realization using a ring oscillator. The paper comprises OSC characterisation, band-gap modeling, electrostatic modeling, and capacitance modeling. The TCAD model consists of the Hopping and Pool Frenkel premise and characterizes the Density of State (DOS) for traps in deep and tail states. The findings from this research provide valuable information for improving OTFT models, enhancing their predictive accuracy, and advancing the understanding of organic semiconductor device behavior. The electrostatics demonstrate device structure dependency.



Graphical Abstract

Keywords: *Organic Thin Film Transistor (OTFT), C8-BTBT-C8, Density of State (DOS), Charge transportation, Electrostatics model, Compact model*

1. INTRODUCTION

Organic electronics are a nascent area of technology. Replacing inorganic with organic materials is a challenge also. Despite this challenge, organic materials are suitable for photovoltaic light diodes and large-area electronics[1-2]. However, efficient, competitive, and low-cost fabrication still requires significant research effort as theoretical understanding, material properties, and process techniques[3-4]. It represents an entire value-added chain. A long-term global market of a hundred million Euros is predicted for organic electronics. However, implementation for marketable products is a realm of global competition. The solution processability of organic semiconductors enables the implementation of a wide variety of lightweight, low-cost, flexible, foldable, and even disposable OSC devices such as LEDs[7], AMOLED displays[8-9],bio-sensors[10], OTFT [1-2] and solar cells[11-12]. The incorporation of organic materials in optoelectronics has revolutionized the field by enabling efficient and flexible devices for light emission, detection, and modulation, opening

up new possibilities for advanced optical technologies[13]. The rapid advances in neuromorphic devices are paving the way for hardware implementation of neuromorphic computing systems, promising unprecedented capabilities for future artificial intelligence applications with enhanced efficiency, scalability, and cognitive computing capabilities[14]. The Organic Thin Film Transistor (OTFT) is a basic building brick of organic electronics. Collaboration between academia and industry is addressing the rising demand for organic semiconductor devices[15]. The accessible EDA technology is viable with existing silicon devices. So, the compact model is imperative to fabricate the Organic Semiconductor (OSC) devices. This model works as a bridge between the semiconductor device and circuit design.

The device physics is essential to define any semiconductor. The inspection of basic physical parameters of molecules and charge transportation mechanism helps to improve OSC device performance. All these parameters depend on particular semiconductor material characteristics. Compared to the silicon industry model, organic transistors lack an eventual device model. The charge carrier movement is quite different in OTFT compared to the crystalline Si-transistor. The existing MOSFET model could not fit different disordered OSCs. So, device modeling is necessary for the sense of Density of State (DOS) and charge transportation. Previously, some models were used by modifying the Si model[16]. But it could not describe the characteristics well. Because the model had mostly fitting parameters, the drain current is calculated with the help of other variables and a correction coefficient was introduced. These types of models strongly depend on the device and its structure. It is not based on device physics. In ref.[17] the model was based on drift-diffusion and the Poisson equation. The researchers made an effort for current density, mobility modeling, and density of state. The model forecasts the almost behaviour of pentacene TFT. However, the OSC could not be characterised fully by its physical parameters. One paper [18] concentrated on charge quantities generated by electric fields. The trapped charge and mobile charge were calculated separately then a total charge density equation was developed. However, the characteristics were mismatched in the logarithmic scale. In other words, the leakage current was not matched. A depth study on gate leakage current was done in this paper[19]. The current-voltage equation was updated with a channel length modifier parameter. But it was also dependent on MOSFET models and tested on one OSC (PTAA). In ref. [20] the contacts effect was observed and the current-voltage characteristics formula was updated. Another paper [21] worked on pentacene with poly-vinyl phenol. The Model was dependent on the current density equation to solve the drain current. This paper developed the relationship between metal work function and other OSC parameters. Ref. [22] showed a self-consistent coupling algorithm for biosensor OTFT and concentrated on only P3HT OSC. In ref. [23] the researchers work on the pentacene TFT model again. The space charge limited current model was used to calculate the charge transportation. The trapped and free charge was calculated. The Poisson equation was updated with new formulas[24]. The Monte Carlo approach was used to define the current-voltage relation. The contact resistance and capacitance relations were developed with hopping transportation. The model was successful for Pentacene OTFT. The study shows that the model should have these attributes; a) Congruous behaviour, b) Structure symmetrical, c) Enough input physical parameter variable, d) Easily conversable, e) Tuneable for various experimental data, and e) Flexibility for upgradation. To our best knowledge, there is no Technology Computer-Aided Design (TCAD) model reported for C8-BTBT semiconductors that includes semiconductor physical parameters to forecast TFT characteristics. The universal model for OTFT also does not support new synthesized OSC. In this paper the TCAD model targets the understanding and improvement of organic electronics and the TCAD to SPICE model flow under the DTCO environment is useful for logical circuit creation [25].

2. PROCESS FLOW OF MODELING

Three types of models are used to develop a device technology. Process model, TCAD model, and Compact or SPICE model. In Design Technology Co-Optimization (DTCO) could be done at three levels as shown in Figure 1. For these levels, many tools are in the industry i.e. SILVACO, Synopsys, and Nano FEM (Open source). Among them, SILVACO is the oldest company that provides all tools for DTCO. Here I am discussing some simulators that work at an individual level.

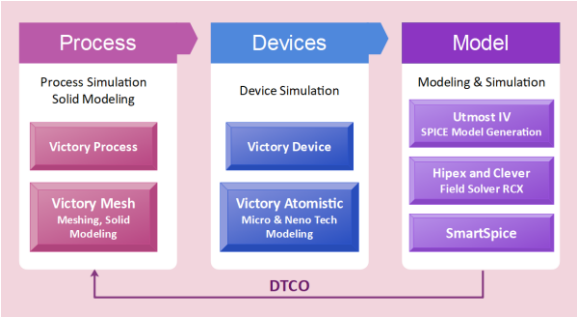


Figure 1. Process flow of modelling.

The thought behind the process simulator is to impersonate the prefabricated processes that are utilized to create devices. Such cycles include etching, deposition, and implantation of various types. The advancement of models for each of these processes is a different field of R&D. The TCAD engineer takes the proper models and takes on them to remove the drawbacks of the test system. The perfect process simulator follows a similar process flow to the targeted device. SILVACO provides two simulators for fabrication process simulation.

Simulation gives data about the innermost charge distribution and the terminal attributes of the device and accordingly has the option to anticipate the device conduction. There exist two in-general techniques around here, first, an analytical methodology that utilizes geometries with resolved equations and solves these equations for different locals such as space-charge, quasi-neutral, and so on. In the first methodology, just a little data can be accessible about the inward condition of the device. The other methodology that will be talked about in more detail is the numerical methodology that addresses the fundamental principles of semiconductors and modelled them. ITRS roadmaps show that TCAD simulators reduce production costs by up to 30%. TCAD is part of a Design Technology Co-Optimization (DTCO) flow. In this process, designs improve across multiple domains –Process, Device Element, Layout, SPICE, and RC extraction. A full TCAD to SPICE flow under a DTCO environment gives accurate actionable output for circuit design optimization.

A compact model is a numerical portrayal of an electrical device as utilized by circuit architects to copy the electrical component characteristics in circuit technology. These models are expected to mathematically figure out the device attributes

(charge flow and noise as an element of the terminal voltages) exactly and quickly enough to mimic complete circuits. Both passive and active devices could be simulated by Compact models in IC design. The off-chip devices are being modelled for system-in-package continuously.

3. TCAD MODELING

The SILVACO ATLAS is used to define semiconductor material parameters. It calculates the model parameters by applying Maxwell's ordinance on 2d/3d mesh points and uses the Poisson equation solution for boundary conditions of the charge. Accordingly, both AC and DC transient models of any device could be developed by ATLAS[26].

3.1. Semiconductor Fundamental Modeling

A transistor on and off operation always depends on semiconductor material characteristics. The 2,7-Dioctyl{1}benzothieno{3,2-b}{1}benzothiophene (C8-BTBT-C8) has some sigma (σ) and pi (π) bonds as shown in Figure 2(a) & (b). In the molecule, weak pi (π) bonds are built from the 'p' orbital electrons and that orbit is far away from nuclei. The pi bonds get shorter than their standard length because of the alternative pi, sigma bonds sequence. In the result, pi bond localization and delocalization (Figure 3(a)) start the conduction in the OSC layer. Alternative bonding and anti-bonding create a prohibited energy gap. In this manner, the band gap is determined by the arrangement of particles.

A free-charge molecular [27] is the foundation of conjugated polymers. It is defined by minimum factor and explained quantitatively as an insulator, semiconductor, or conductor made of a linear chain of carbon atoms. Expect a line of 'N' atoms isolated by a distance 'd', so the all-out length of the chain is $(N-1) \times d$ and approximately 'Nd' for a large amount of N. As indicated by the quantum-mechanical model for a free molecule in a 1-d box (potential zero inside and endless outside):

$$E_n = \left(\frac{\hbar^2}{8m}\right) \times \left(\frac{n^2}{(Nd)^2}\right), \text{ with } n = 1,2,3 \ldots \quad (1).$$

where: $\hbar$ is Planck's constant, m indicates electron mass, and n indicates quantum numeral. In Figure 4, the three-dimension distance of d is shown, and d will be calculated as a 3d Matrix.

It is expected that 'N' p-orbitals give two e^- per molecule to form a pi bond. The Highest Occupied Molecular Orbital (HOMO) energy is calculated using eq.(2) and the Least Unoccupied Molecular Orbital (LUMO) energy is calculated using eq.(3).

$$E(HOMO) = \left(\frac{\hbar^2}{8m}\right) \times \left(\frac{(N/2)^2}{(Nd)^2}\right) \quad (2).$$

$$E(LUMO) = \left(\frac{\hbar^2}{8m}\right) \times \left(\frac{(N/2+1)^2}{(Nd)^2}\right) \quad (3).$$

Thus, energy is expected to energize an e^- in eq. (4).

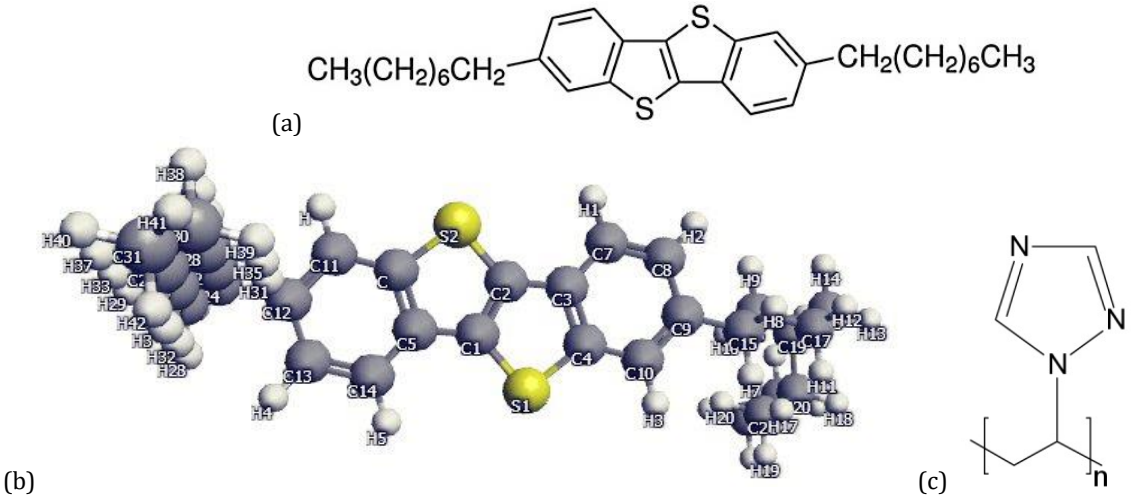


Figure 2. (a) Chemical structure of C8-BTBT (b) Molecular structure of C8-BTBT (c) Chemical structure of PVT

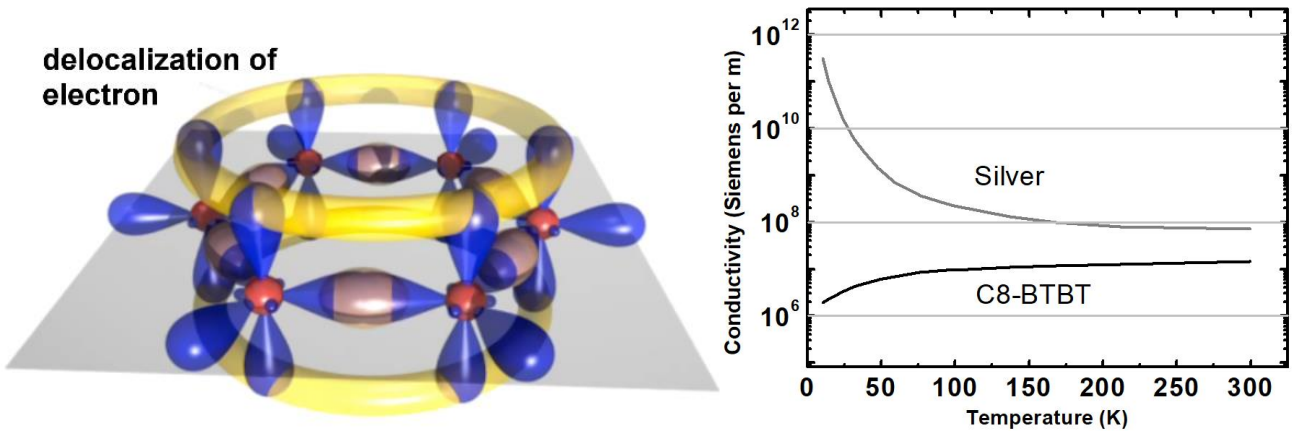


Figure 3. (a)Delocalization of π electron (b) **Conductivity comparison between Metal (Ag) and typical OSC (C8-BTBT)**

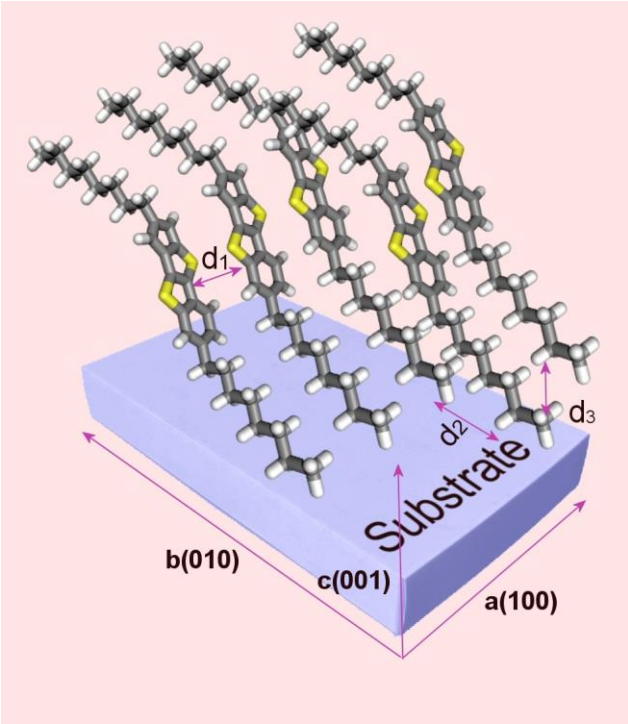


Figure 5. Average distance between molecule to molecule in 3d.

$$E_G = E(LUMO) - E(HOMO)$$

$$E_G = \left(\frac{h^2}{8m}\right) \times \left(\frac{N+1}{(Nd)^2}\right) \approx [h^2/8md^2]/N \text{ for large N} \quad (4).$$

Any semiconductor energy bandgap can be formulated by a numerical relation of a reliant variable. The temperature affects the band gap moreover. A small increment in temperature also raises the valence band energy median and it is shown as an exponential impact at the high electric field. As a result, the lower energy band gap expands the charge current amount at a similar voltage level, and it raises the temperature once more. This process starts a compound chain. However, under five Voltage there isn't a sufficient electric field that compounds the chain.

In Figure 3(b), the conductivity of metal and OSC (C8-BTBT-C8) is compared at high temperatures. While the metal exhibits superconductivity at a lower temperature, the OSC shows higher conductivity, reaching up to 10^7Siemens/m. It confirms that it is quite sufficient for charge conduction. In this TCAD model, eq.(5) is defined for the C8-BTBT OSC band gap[28], Here E_{g0} is a theoretical band gap [23] that is evaluated by eq. (4) and it could be extracted also by experimental work at room temperature. 'T' is the temperature variable[29] and E_{G_α} & E_{G_β} are fitting parameters.

$$E_g(T_L) = E_{g0} + E_{G_\alpha}\left[\frac{300^2}{300 + E_{G_\beta}} - \frac{T^2}{T + E_{G_\beta}}\right] + \Delta E_g \quad (5).$$

$$\Delta E_g = -\zeta_c\left[\frac{\epsilon_s^5}{D}\left(m_0 + \zeta_B * T^2 \frac{\epsilon_s}{D}\right)\right]^{-\frac{1}{4}} \quad (6).$$

Generally, OSC is oxide for p-type sub-atomic doping and reduction is used for n-type sub-atomic doping. The eq. (6) is the higher doping correction that depends on OSC dielectric ϵ_s and m_0, the mass of e^- at rest condition (9.11×10^{-31}kg). 'D' is the doping concentration. The ζ_B and ζ_c are defined for fitting and correction. These two functions can address the band gap of C8-BTBT.

Table 1. Semiconductor Band Gap Parameters

Parameter	Value	Units
E_{g0}[30]	3.32	eV
E_{G_α}	3.85×10^{-4}	eV/K
E_{G_β}	565	K
ζ_c	3.1×10^{-5}	$eVcm^{-3/4}$
ζ_B	2.9×10^{12}	$cm^{-3}K^{-2}$
N	2×10^{17}	cm^{-3}
ϵ_s	3.6	(ratio)

3.2. Density of States (DOS)

Disordered semiconductors are characterized by localized functions and extended energy states in the forbidden energy gap. Transportation of charge is only possible by thermal activation, tunneling, hopping, or a hybrid of both. In hopping transportation supplementary energy to surmount the energy barricade is given by thermal vibrations or an electric field. The

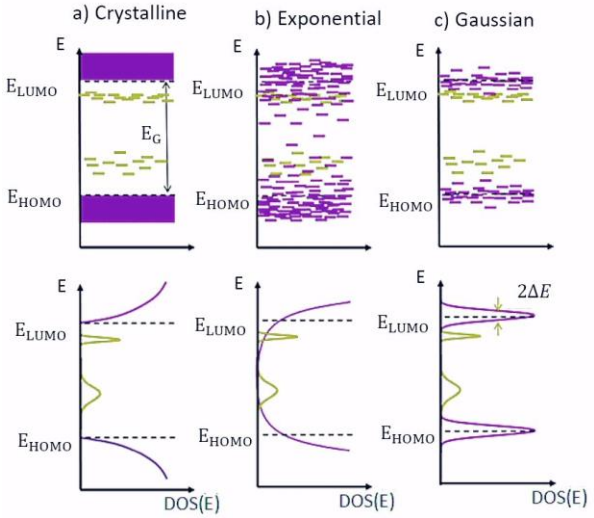
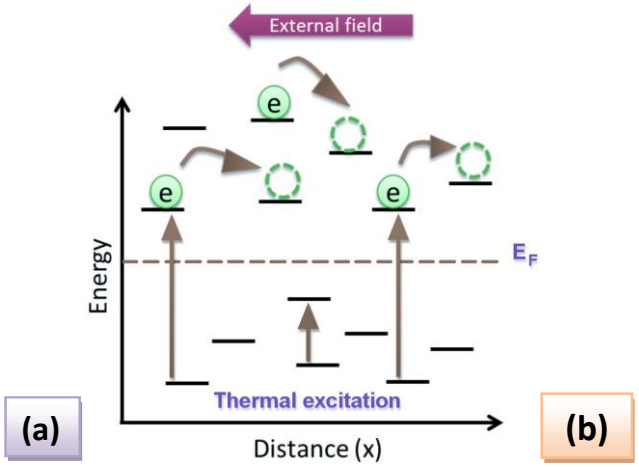


Figure 4. Density of State (a) Crystalline (b) Exponential (c) Gaussian.

effectiveness of hop studies includes the height of the potential barricade to the following hop site and additionally the presence of thermal vibrations (temperature). For a tunneling cycle, the transition probability relies upon the shape of the potential gap, i.e. width, and height. A mix of tunneling and hoping operation is frequently utilized and named thermally or phonon-assist tunneling. The potential barrier is depicted in two sorts. First is uniform and second is non-uniform. The uniform type is described previously, while the non-uniform type can be further categorized into two types: exponential and Gaussian, as shown in Figure 5 [31].

In exponential DOS[32], to characterize the boundary condition for surface charge density p_s and channel p_{ch}, the transporter density at OSC/metal coupling is calculated by Boltzmann's insights so that p is emphatically injection-limited following.



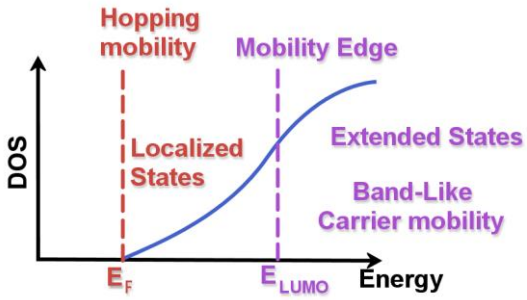


Figure 7. Comparison of the region of different charge transportation.

Figure 6. (a) Hopping Transportation and (b) Multiple trapping and release

$$p = N_V exp\left(\frac{E_V - E_F}{K_B T}\right) \quad (7).$$

$$N_V(E_p) = \frac{N_{t,P}}{\sqrt{2\pi}\sigma_P} \cdot exp\left(-\frac{E_P^2}{2\pi\sigma_P^2}\right) \quad (8).$$

$$N_{t,p} = \frac{1}{\theta_P^3} \quad (9).$$

.

All the symbols have their prevailing meaning. E_V is the valance band energy level as defined by uniform DOS. E_F is the fermi level and T is the temperature variable. $N_V(E)$ is the distribution for modeling holes. E_P is the hole energy in the valance band, and σ_P is the distribution width. The densities of sites $N_{t,P}$ is calculated using eq. (9). θ_P is the localization length of the hole. All these parameters are calculated for minority charge carriers also by following the same procedure. The DOS in Gaussian distribution as the acceptor states is described by eq. (10). In this equation N_{IA} is the density of the acceptor for intrinsic traps and N_A is the total density of the doped acceptor. E_A is the energy difference between the doping and intrinsic states for the acceptor. σ_{IA} is the Gaussian distribution width of the acceptor as intrinsic OSC and σ_A is the Gaussian distribution width of the doped acceptor. In the entire function, E is the energy variable.

$$g_A(E) = \frac{N_{IA}}{\sqrt{2\pi}\,\sigma_{IA}} exp\left(-\frac{(E - E_c)^2}{2\,\sigma_{IA}^2}\right) + \frac{N_A}{\sqrt{2\pi}\,\sigma_A} exp\left(-\frac{(E - E_c + E_A)^2}{2\,\sigma_A^2}\right) \quad (10).$$

In steady state, the probabilities of occupation are given by eq.(11):

$$f_{tA} = \frac{v_n\sigma_{AE}\, n + v_p\sigma_{AH}\, n_i\, exp\left[\frac{E_i - E}{kT_L}\right]}{v_n\sigma_{AE}\left(n + n_i\, exp\left[\frac{E - E_i}{kT_L}\right]\right) + v_p\sigma_{AH}\left(p + n_i\, exp\left[\frac{E_i - E}{kT_L}\right]\right)} \quad (11).$$

Here, v_n and v_p are e^- and hole thermal velocity respectively, n_i is the intrinsic hole concentration, σ_{AE}, and σ_{AH} are $e^-$and hole capture cross-sections respectively. Thus, the concentration of the acceptor is given by eq. (12):

$$n_A = \int_{E_v}^{E_{tr}} gA(E) f_{tA}(E, n, p) dE \quad (12).$$

Here, E_{tr} is required to transport energy for the hole. The lattice of former semiconductor materials and their extremely low density of defects permits one to precisely portray the charge transport through delocalized energy groups isolated by an energy band gap. Most of the OSC is nebulous and rich in structure defects subsequently requiring extra-ordinary models for charge transportation to be accustomed and expanded; also, charges can run, with various mobilities, inside the atomic chain, between nearby particles, or between various spaces, mostly called as grains (entomb grain).

3.3. Charge transportation

The complexity of charge transport in OSC comes from the weaker intermolecular atomic bond in the solid state. A direct consequence of the feeble Van der Waals forces is the minimal orbital overlap, which results in restricted charge mobility. In general, the range of (crystalline) semiconductors is a few eV, on the other hand, OSCs have a range of 2 to 3.8 eV. In addition, understanding and creating charge-transportation models that cover an enormous number of material classes is still a challenge. Three types of charge transportation can occur under the domain of charge states energy also shown in Figure 6; a) Band-like transportation, b) Hopping transportation, and c) Pool Frenkel or MTR.

3.3.1. Band-Like transportation

Conversely, in very well-ordered crystal structures, such as those found in inorganic semiconductors and highly organized OSC, charge transport is considered possible within boundary conditions. Computing the Schrodinger condition inside these boundary limits gives an energy function in two intermittent bands. Between these bands, there is no solution to the equation, and so it is unphysical for charge carriers to exist within that space. Due to the periodic nature of the crystal structure, the wavefunctions, and consequently the electrons, are delocalized across the bands, allowing electrons to extend throughout the entire crystal. This sort of transport model, not at all like hopping, will prompt huge conduction and enable materials with possibly extremely high flows and mobilities. All these calculations are related to energy band gap estimation. The effective mobility from this transportation is shown in eq.(13). μ_0 is zero field mobility.

$$\mu_b = \mu_0 exp\left(-\frac{E_V - E_F}{kT}\right) \quad (13).$$

3.3.2. Hopping Transportation

Due to disordered energy, the charge transportation in an amorphous semiconductor is restricted by confinement in localized states. This means that the mobility of charge carriers is thermally activated, and transport occurs through hopping from one localized site to the next as shown in Figure 7(a). This kind of transport is called hopping[33]. The progress of jumping between two local sites upon the cross-over of the electronic wave relation of these two destinations. At the point when a charge transporter jumps to a site with a lower (higher) site, the energy difference is adjusted by the emission (absorption) of a phonon. It might be invisible light radiation or not but it causes heat. So, at operation time, it ignites the temperature and conduction loop. The mobility due to hopping is defined as μ_{n_hop} and μ_{p_hop}. Eq.(14) is allied to the positive charge carrier. Here V_{0p_hop} is the attempt frequency to jump a hole in the conduction band, β_{p_hop} is the percolation relation, $g_a(E)$ is the DOS for the acceptor conduction energy band, and γ_{p_hop} is equal to 1/hole localization radius. Similarly, in eq. (15) subscript n stands for $e^-$and all these parameters correspond to the previous description.

$$\mu_{p_{hop}} = \frac{qV_{0p_{hop}}}{kT}\left[\int_{-\infty}^{Err_p} g_d(E)dE\right]^{-\frac{2}{3}} exp\left[-2\left(\frac{3\beta_{p\_hop}}{4\pi}\right)^{1/3}\gamma_{p\_hop}\left[\int_{-\infty}^{Err_n} g_d(E)dE\right]^{-1/3}\right] \quad (14).$$

$$\mu_{n_{hop}} = \frac{qV_{0n_{hop}}}{kT}\left[\int_{-\infty}^{Err_n} g_a(E)dE\right]^{-\frac{2}{3}} exp\left[-2\left(\frac{3\beta_{n\_hop}}{4\pi}\right)^{1/3}\gamma_{n\_hop}\left[\int_{-\infty}^{Err_n} g_a(E)dE\right]^{-1/3}\right] \quad (15).$$

3.3.3. Poole-Frenkel Mobility Model

The Poole-Frenkel model [34] depends on multiple trap and release (MTR) phenomena. A few unique materials, like small-molecule OSC and the new IGZO semiconductors, have the propensity to shape the polycrystalline film. These semiconductors show systematic positioning and delocalized orbitals cross-over, compared to another effective charge movement, which is a lot higher than amorphous surfaces. The charge carrier transport characteristics of these materials can't be sensed by only the grain-boundary theory and hopping mechanism. As opposed to the grain-boundary approach or hopping mechanism, the Poole-Frenkel model is realised for some materials [35]. This theory accepts that charge transportation also occurs in extended states [36]. The vast majority of charge transporters are caught in confined states [37]. When the local state energy has a lower mobility edge, the expanded states act as shallow traps[38], whereby the charge transporter can be emitted (released) by thermal stimuli. Yet, if energy is far underneath mobility edge energy, charge transporters can't be thermally energized.

$$\mu_{p\_pf}(E) = \mu_{p0} exp\left(\left(\frac{\beta_{p_{pf}}}{kT} - \gamma_{p_{pf}}\right)\sqrt{|E|} - \frac{\delta_{p_{pf}}}{kT}\right) \quad (16).$$

$$\mu_{n\_pf}(E) = \mu_{n0} exp\left(\left(\frac{\beta_{n_{pf}}}{kT} - \gamma_{n_{pf}}\right)\sqrt{|E|} - \frac{\delta_{n_{pf}}}{kT}\right) \quad (17).$$

Here μ_{p0} is hole mobility, and δ_{p_pf} is hole activation energy at zero electric fields. β_{p_pf} and β_{p_pf} denote the Poole-Frenkel factors. E is the applied electric field variable. In the steady state of any device charge generation/recombination rates are in equilibrium. This rate could be estimated using eq. (18), and total effective charge mobility using eq.(19).

$$R_{n,p} = \int_{E_V}^{E_C}\left[\frac{v_n v_p \sigma_{AE}\sigma_{AH}(np - n_i^2)g_A(E)}{v_n\sigma_{AE}\left(n + n_i exp\left[\frac{E - E_i}{kT}\right]\right) + v_p\sigma_{AH}\left(p + n_i exp\right.} + \frac{v_n v_p \sigma_{DE}\sigma_{DH}(np - n_i^2)g_D(E)}{v_n\sigma_{DE}\left(n + n_i exp\left[\frac{E - E_i}{kT}\right]\right) + v_p\sigma_{DH}\left(p + n_i exp\left[\frac{E_i}{k}\right.\right.}\right. \quad (18).$$

$$\frac{1}{\mu_{effective}} = \frac{1}{\mu_b} + \frac{1}{\mu_{hop}} + \frac{1}{\mu_{pf}} \quad (19).$$

4. MODEL SIMULATION

Since the expense of trial investigation of any technology is higher and it incorporates a peril deal of time and cost, TCAD becomes a vital stage to examine any innovation. The realization and optimization of the semiconductor device process are required studies at the phenomenon level. The TCAD additionally gives GUI which reduces the time taken to understand and generalize the fundamentals. In [39] A. Ablat et al, experimented in 2018 to understand the effect of a hole injection layer on OSC film. A highly doped n^{++} (approx. ~ 10^{19}) silicon substrate was utilized as gate substrate. They experimented with MoO_3 and WoO_3 both hole injection layers on Au and Ag contacts at various channel lengths. The result showed a better on/off ratio and mobility in MoO_3 / Ag combinational contact. Here we examine our TCAD model from this data that has BGTC (Bottom Gate Top Contacts) structure. Poly (1-vinyl-1, 2, 4-triazole) (PVT) acts as a passivation layer and increases OSC conductivity by accumulating charge ions on the interface layer of PVT and OSC. After defining the structure shown in Figure 8, the model is deployed in DeckBuild. The ATLAS simulator simulates all these equations based on continuity Poisson's Equation.

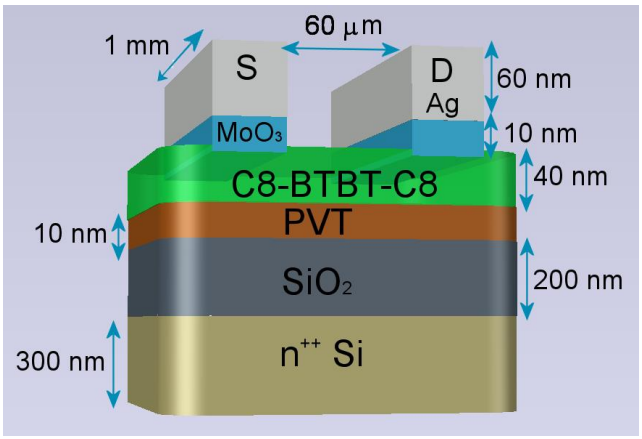


Figure 8. Structure and dimensions of C8-BTBT device.

$$\vec{J}_p = qp\mu_p\vec{E}_p - qD_p\nabla p \quad (25).$$

where:

$$\vec{E}_n = -\nabla\left(\psi + \frac{kT}{q}\ln n_{ie}\right);\ \vec{E}_p = -\nabla\left(\psi - \frac{kT}{q}\ln\ n_{ie}\right) \quad (26).$$

$$D_n = \frac{kT}{q}\mu_n\ ;D_p = \frac{kT}{q}\mu_p \quad (27).$$

Here n_{ie} is charge intrinsic concentration and μ_p, μ_p is hole and electron mobility at zero electric fields. The resultant hole concentration is plotted as Figure 9(a). For device mathematical compilation different solution approaches are utilized depending on the situation. It is also conceivable to use a combinational mathematical approach to get the solutions. There are three kinds of approaches used for acquiring results for semiconductor devices[41]. These are addressed by a) de-coupled (GUMMEL), b) completely coupled (NEWTON), and c) BLOCK. In NEWTON elucidation, each emphasis of the Newton technique addresses a linearized form of the whole non-

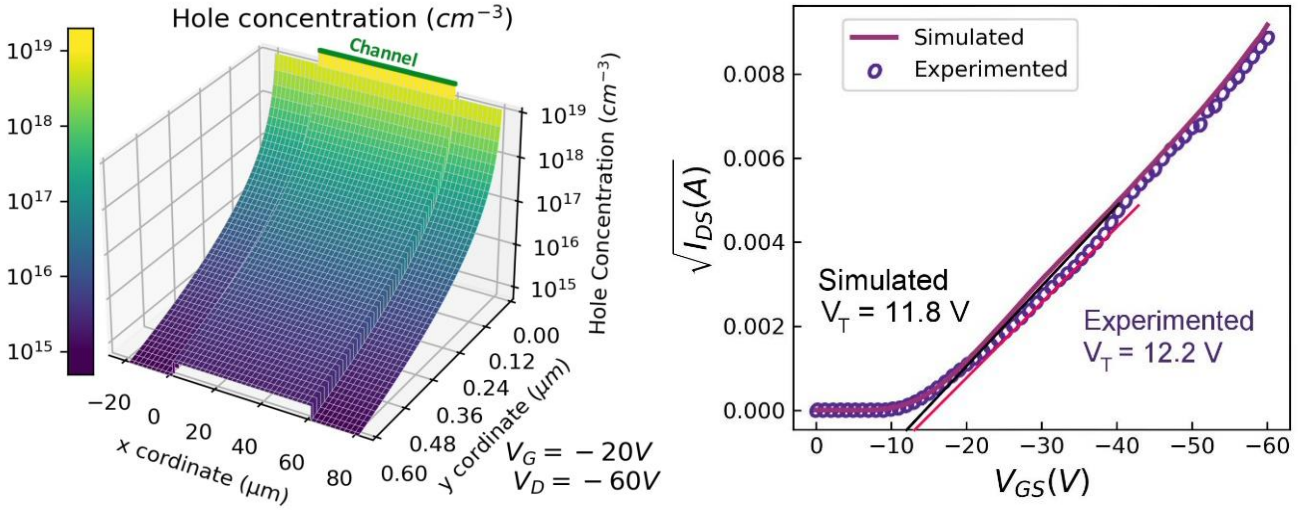


Figure 8. (a) Hole concentration in OSC layer. (b) Threshold voltage extraction simulated and experimental work of C8-BTBT-C8.

$$Div(\varepsilon\nabla\psi) = -\rho\ ;\ \vec{E} = -\nabla\psi \quad (20).$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. The reference potential can be defined in various ways. Here ρ is defined by eq.(21):

$$\rho = q[p - n + N_D^+ - N_A^-] \quad (21).$$

N_D^+ is the total donor density, and N_A^- is the total acceptor density. The dynamics of charge carrier distribution over time are also described by eq.(22) and (23).

$$\frac{\partial n}{\partial t} = \frac{1}{q}div\overrightarrow{J_n} + G_n - R_n \quad (22).$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}div\overrightarrow{J_p} + G_p - R_p \quad (23).$$

where $\overrightarrow{J_p}$ and $\overrightarrow{J_n}$ are the hole and electron current densities, $G_p$and G_n are the generation rates for holes and electrons, R_p and R_n are the recombination rates for holes and electrons, and q is the magnitude of the charge on an electron[40].

The current density is calculated by the drift-diffusion model and the final equation is:

$$\vec{J}_n = qn\mu_n\vec{E}_n + qD_n\nabla n \quad (24).$$

straight arithmetical framework. The size of the issue is moderately enormous, and every emphasis consumes a large amount of time. Despite this, the problem will typically converge in time (in around three to eight attempts) if the initial guess is adequately near the last solution. Every emphasis of Gummel's strategy tackles the sub-issues of the problem. The sub-issues are acquired by linearizing an equation of the set concerning its preliminary solution variable while holding different variables at their latest calculated values. By solving this linear subsequent system, the corrections for one variable are calculated. One stage of the Gummel cycle is finished when the methodology has been performed for every autonomous variable. The Gummel method commonly converges slower, yet the strategy will often endure poor initial guesses. In BLOCK the result is acquired by addressing a few equations by the coupled technique, while others are performed by the de-coupled approach. So, the BLOCK method has been used for numerical simulation.

5. VERIFICATION AND RESULT DISCUSSION

In ref. [29], Ablat et al. investigated the performance of bottom-gate, top-contact (BGTC) C8-BTBT-C8 OTFT devices with either gold (Au) or silver (Ag) as source/drain electrodes, with and without molybdenum oxide MoO_3 interlayers. They evaluated

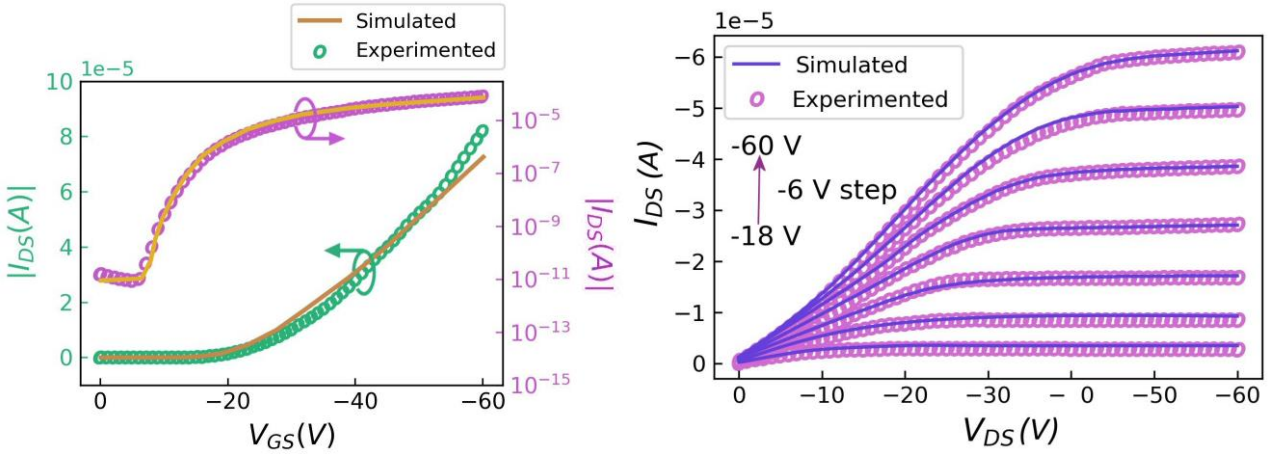


Figure 9. (a) Comparison of Simulated and Experimental Data [29] of I_{DS} vs V_{GS} for C8-BTBT-C8 (b) Comparison of Simulated and Experimental data [29] of I_{DS} vs V_{DS} for C8-BTBT-C8 OSC.

the output characteristics at various gate voltages and observed that all six-drain current-drain voltage ($I_{DS} - V_{DS}$) plots exhibited exceptional behavior in both the linear and saturation regions. The paper showed that there were significant variations in device performance among different source/drain electrodes, particularly in the linear region. Ag electrodes resulted in higher mobility than Au electrodes for C8-BTBT-based devices, but also exhibited higher contact resistance. The incorporation of MoO_3 interlayers further increased the output current and enhanced linearity at low V_{DS}, suggesting a reduction in contact resistance. The MoO_3/Ag electrode configuration produced the highest on-state current. The experimented data in Figure 8 is extracted from this paper.

The model has been simulated on SILVACO. At first, the structure dimensions were defined and the SOPRA file was generated. The device characteristics (I_{DS} vs V_{GS} and I_{DS} vs V_{DS}) have been produced. Here we can see the device characteristics are reasonably matched. The I_{DS} vs V_{GS} has matched on both log and liner scales at one point and I_{DS} vs V_{DS} has been calculated at six gate voltage points as shown in Figure 10. The threshold voltage is extracted as shown in Figure 9(b). Some mismatch of I_{DS} vs V_{GS} is due to exponential charge conduction at high voltage. Here PVT increases total current by promoting hole transportation on the interface layer and increases the on-off ratio also.

However, the +ve charge conductivity [42] of the doped PVT layer could be a critical property for any OTFT to turn into a high-performance device. In Figure 11 threshold voltage is extracted and compared with experimented data.

6. ELECTROSTATIC MODELING

The charge and electric potential distribution are key to measuring the device. The electrostatics modelling helps to understand the device's operation and helps to improve device structure for better performance. Here at any point x in the OSC channel can be represented by the illustration Figure 11 and corresponding variables are defined in Table 3. In this figure, the conduction band and valance band are shown, and some variables are shown i.e. work function difference, conduction band to combined fermi level differences, and the voltage developed across the layers (that depend on conduction band energies). At first, charge conservation is applied to the entire structure.

$$Q_g = -\left(qn_{it} - qn_l - qn_{buf}\right) \quad (28).$$

where Q_g denotes the charge density at the gate electrode. The potential gains /drops across layers are as eq. (29),(30),(31).

Table 2. Comparison of performance parameters

Parameters	Formula	Experimental Values	Simulated Values	Unit
Capacitance per unit area (C_{ox})	$C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} = \frac{\epsilon_0 \epsilon_r A}{T_{OX}}$	0.19	0.19	nF/cm^2
Threshold Voltage (V_T)	Graphically extracted	1.4	1.55	volt
Transconductance (G_m)	$G_m = \frac{\partial I_{DS}}{\partial V_{GS}}$	$1x10^{-8}$	5.82×10^{-9}	siemens
Mobility in the linear region (μ_{lin}) (at $V_{GS} = -10V$)	$\mu_{LIN} = \frac{LG_M}{WC_{OX}V_{DS}}$	$2.7x10^{-5}$	$1.6x10^{-5}$	$cm^2/V-s$
Mobility in the saturation region (μ_{sat}) (at $V_{GS} = -45V$)	$\mu_{SAT} = \frac{2L}{WC_{OX}}\left(\frac{d\sqrt{I_{DS}}}{dV_G}\right)^2$	$2.62x10^{-2}$	$3.11x10^{-2}$	$cm^2/V-s$
Sub-threshold Slope (SS)	$SS = \left(\frac{d\log(I_{DS})}{dV_{GS}}\Big\|max\right)^{-1}$	0.087	0.075	Volt/decade
On-Off ratio	I_{on} / I_{off}	10^6	10^6	(ratio)

$$V_{ox} = \frac{Q_g}{C_{ox}} \quad (29).$$

$$V_{PVT} = \frac{-Q_g + \sigma_{PVT} - \sigma_{PVT} - qn_{it}}{C_{PVT}} = \frac{-Q_g - qn_{it}}{C_{PVT}} \quad (30).$$

$$V_{OSC} = \frac{-Q_g + \sigma_{PVT} - qn_{it} - \sigma_{PVT} + \sigma_{OSC} + qn_l - \sigma_{OSC}}{C_{OSC}} \quad (31).$$

$$= \frac{-Q_g - qn_{it} + qn_l}{C_{OSC}}$$

Table 3. Symbol description and value used in electrostatic modeling.

Symbol	Description	Value (Unit)
ϕ_{m-ox}	Surface barrier height at the gated region	3.81 V
$\chi_{P,O}$	Conduction band offset at the PVT/OSC interface	1.74V
n_{buf}	The density of space charge in the buffer	$1.2 \times 10^{12}/cm^2$
n_{it}	The density of interface charge in the PVT layer	$1.8 \times 10^{13}/cm^2$
σ_{PVT}	PVT spontaneous polarization charge density	$2.4 \times 10^{-6}C/cm^2$
σ_{OSC}	OSC spontaneous polarization charge density	$2.7 \times 10^{-6}C/cm^2$
V_{g-ch}	Gate-to-channel potential difference at any point x.	Variable
E_f^l	Difference between the Fermi level and the conduction band of OSC.	Intermediate variable
E_f^u	Difference between the Fermi level and the conduction band of the hole injection layer.	Intermediate variable

where $V_{OX}(C_{OX}), V_{PVT}(C_{PVT})$, and $V_{OSC}(C_{OSC})$ are the voltage (area capacitance) across the SiO_2, PVT, and C-8 BTBT (OSC) layers respectively. According to Poisson's equation electric fields on interface layers are eq. (32), (33)

$$\mathcal{E}_{PVT} = \frac{-Q_g - qn_{it}}{\epsilon_{PVT}} = \frac{qn_l + qn_{buf}}{\epsilon_{PVT}} \quad (32).$$

$$\mathcal{E}_{OSC} = \frac{-Q_g - qn_{it} + qn_l}{\epsilon_{OSC}} = \frac{qn_{buf}}{\epsilon_{OSC}} \quad (33).$$

By examination of the band diagram [43], doing potential balance y=0 (gate) to (y=630 nm) S/D electrode.

$$\phi_{m-ox} - V_{g-ch} + V_{ox} - \chi_{P,O} + \frac{E_f^l}{q} = 0 \quad (34).$$

Substituting V_{OX} from eq.(28) and (29), we can rewrite eq. (34) as:

$$E_f^l = qV_{gov}^l + \frac{q(qn_{it} - qn_l - qn_{buf})}{C_{ox}} \quad (35).$$

where qV_{gov}^l is supposed as

$$V_{gov}^l = V_{g-ch} - \phi_{m-ox} + \chi_{P,O} \quad (36).$$

We can redo all calculations for the hole injection layer and get.

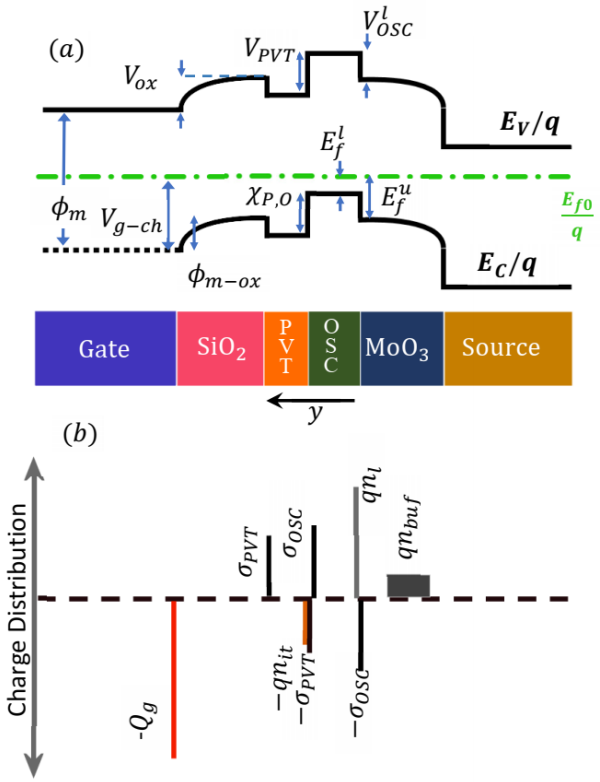


Figure 10. (a) Band- Diagram and voltage across layers along (-) y direction. The symbols used in the diagram are defined in Table 3. (b) Illustration of charge distribution at on state.

$$E_f^u = qV_{gov}^u + \frac{q(qn_{it} - qn_l - qn_{buf})}{C_{ox}} + q(qn_{it} - qn_l - qn_{buf})\left(\frac{1}{C_{PVT}} + \frac{1}{C_{OSC}}\right) \quad (37).$$

where V_{gov}^u is defined as

$$V_{gov}^u = V_{g-ch} - \&\phi_{m-ox} + \chi_{P,O} + \frac{\sigma_{PVT}}{C_{PVT}} + \frac{\sigma_{OSC}}{C_{OSC}} - qn_{it}\left(\frac{1}{C_{PVT}} + \frac{1}{C_{OSC}}\right) \quad (38).$$

Suppose, the quasi-constant electric field is accruing the OSC, the j^{th} sub-band energy E_j from the edge of the conduction band is shown with the solution of the Schrodinger equation [44],

$$E_j = q\left(\frac{\hbar^2}{2m}\right)^{\frac{1}{3}}\left(\frac{3}{2}\pi q\mathcal{E}\right)^{\frac{2}{3}}\left(j + \frac{3}{4}\right)^{\frac{2}{3}} \quad (39).$$

where ħ denotes the minimized Planck's constant and m is the e^-effective mass in OSC. The first sub-band is calculated as:

$$E_{c1}^l = \alpha(\mathcal{E}_{OSC}^l)^{\frac{2}{3}} \quad (40).$$

where α is an experimentally compared value, which is equal to $2.1920 \times 10^{-25} Kg^{\frac{1}{3}} m^{\frac{4}{3}} A^{\frac{2}{3}}$.

Charge density equation can be gained with the help of Fermi-Dirac statistics and DOS under a parabolical distribution relationship, as

$$n_l = D_n kT ln\left[1 + exp\left(\frac{E_f^l - E_{c1}^l}{kT}\right)\right] \quad (41).$$

Plugging eq. (33), eq. (35) and eq. (40) in above eq.(41), we get charge density in the channel as eq. (42):

$$n_l = D_n kT ln\left[1 + exp\left(\frac{qV_{gov}^u}{kT} + \frac{q(qn_{it} - qn_l - qn_{buf})}{C_{ox}kT} - \frac{\alpha}{kT}\left(\frac{qn_{buf}}{\epsilon_{OSC}}\right)^{\frac{2}{3}}\right)\right] \quad (42).$$

The channel threshold voltage is obtained from Fig.12. as eq. (43)

$$V_T^l = \phi_{m-ox} - \chi_{P,O} - \frac{qn_{it} - qn_l - qn_{buf}}{C_{ox}} \quad (43).$$

7. COMPACT MODELING, PARAMETER COMPUTATION

A compact model [45] of a device is a mathematical depiction of the behavior that can be modified with physical parameters. The model is used for (CAD) tools to analyze ICs or circuits. Compact models are a bundle of analytical formulations with technology-specific device model frameworks that characterize the device behavior of a manufacturing technique and are used to solve by a circuit simulator for IC or circuit design. Compact models responsible for a realistic examination of representative IC tech. It has been used since the origination of ICs (the year 1958), plays a vital role in the nanometer-scale SOC design epoch. Nowadays, compact models are the utmost significant brick of the process design kit[44], that bridge the device technology and circuit creators. In technology noise characteristics are becoming a massive challenge for model designers and circuit creators[46]. A good compact model must clearly describe all material device effects and also suitably create them to maintain high computing efficiency. Equations of device models have developed from a variety of sample equivalent circuits. These circuits represent the following modes: AC, DC, transient, and noise. Figure 12 shows a similar circuit for transient and DC analysis. During DC simulation, capacitances are omitted.

The i_{ds} current is the key component of the DC analysis. The partial derivatives given below are the main components of the simulation for AC, DC, transient, and noise assessments. The change in i_{ds} can be measured with two voltage variables v_{gs} and v_{ds}. These terms are called Transconductance and Output conductance [47] and are calculated as eq.(44) & (45).

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const} \quad (44).$$

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=const} \quad (45).$$

In the amorphous TFT model, the drain current is determined by the intrinsic voltages (V_{GS} and V_{DS}, respectively) and is given by:

$$I_{DS} = G_{ch} \cdot V_{dse} \cdot (1 + \lambda \cdot V_{DS}) \quad (46).$$

where G_{ch} is channel conductance, λ is the output conductance fitting parameter, and V_{dse} is a modified drain-source variable that helps to adjust the effects of channel conduction.

$$V_{dse} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{dsat}}\right)^M\right]^{\frac{1}{M}}} \quad (47).$$

V_{dsat} is the Saturation drain voltage that could be extracted experimentally. This could be modelled with the following equation:

$$V_{dsat} = \alpha_{SAT}(Temp) \cdot V_{gte}; \quad (48).$$

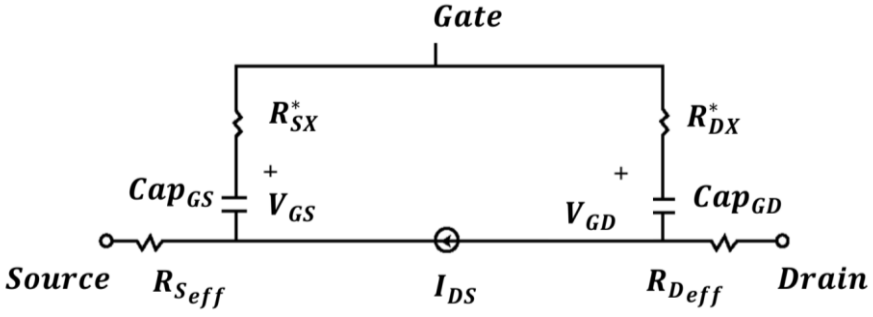
$$\alpha_{SAT}(Temp) = \alpha_{SAT} + K_{ASAT}.(Temp - 300K)$$

'm' is the Knee shape fitting parameter. Parameter m is responsible for transfiguration linear to saturation regimes. It is extracted by two straight lines approximating the saturation and linear regimes[48]. The current where these two straight lines intersect is $I_{lin} = I_{sat} - \Delta I \approx I_{sat}/2^{1/M}$. So, m could be calculated as eq.(49)

$$m \approx \frac{log\,(2)}{log[I_{sat}/(I_{lin})]} \approx \frac{log\,(2)}{log[I_{sat}/(I_{sat} - \Delta I)]} \quad (49).$$

α_{SAT} is the model parameter in the saturation region. K_{ASAT} is the temperature coefficient of α_{SAT}.

$$V_{gte} = \frac{V_{MIN}}{2} \cdot \left[1 + \frac{V_{gt}}{V_{MIN}} + \sqrt{\Delta^2 + \left(\frac{V_{gt}}{V_{MIN}} - 1\right)^2}\right] \quad (50).$$



Note: (*) R_{SX} and R_{DX} are optional resistors used to account for frequency dispersion effects.

Figure 11. OTFT Equivalent Circuit for Transient Analysis

$$V_{gt} = V_{gs} - V_{TO}(Temp);\ V_{TO}(Temp) = V_{TO} + K_{VT}(Temp - 300K) \quad (51).$$

The gate voltage value is modified for temperature dependency and convergence. So the parameter is set as transition width parameter (Δ) and convergence parameter (V_{MIN}) for the desired resolution or sampling size. K_{VT} is the temperature coefficient of the threshold voltage. Convergence is part of the prime goals in creating an effective circuit simulator or device model. From the standpoint of a device model, higher convergence is achieved if the chosen model exhibits continuity as in device current in addition to its 1st and 2nd derivatives. V_{TO} is temperature dependent zero biased threshold voltage parameter. Total conductance depends on contact resistance and can be modified as eq. (52)

$$G_{ch} = \frac{G_{chi}}{1 + G_{chi} \cdot \left(R_{S_{eff}} + R_{D_{eff}}\right)} \quad (52).$$

$R_{S_{eff}}$ and $R_{D_{eff}}$ is the effective resistance of sources and drain terminals and G_{chi} channel conductance computed as a popular methodology [49] as eq.(53)

$$G_{chi} = \frac{q \cdot N_s \cdot W_{eff} \cdot \mu_{BAND}}{L_{eff}} \quad (53).$$

where μ_{BAND} is the conduction band mobility. N_s is a unified parameter of charge density in the channel, and it is divided into two factors, the first depends on threshold voltage temperature function and the second depends on flat band voltage[50]. Thus, gate voltage dependency is calculated as:

$$N_s = \frac{N_{sa} \cdot N_{sb}}{N_{sa} + N_{sb}} \quad (54).$$

$$N_{sa} = \frac{\epsilon_{r_{di}} \cdot \epsilon_0 \cdot V_{gte}}{q \cdot t_{di}} \cdot \left(\frac{V_{gte}}{V_{AA}}\right)^{\gamma} \quad (55).$$

$$N_{sb} = \left(\frac{TM \cdot V_{gfbe} \cdot \epsilon_{r_{di}}}{V0 \cdot t_{di} \cdot \epsilon_{r_{sb}}}\right)^{\frac{2 \cdot V_0}{V_e}};\ V_e = \frac{2 \cdot V_0 \cdot V_{tho}}{2 \cdot V_0 - V_{th}}; \quad (56).$$

$$TM = \sqrt{\frac{\epsilon_{r_{sb}} \cdot \epsilon_0}{2 \cdot q \cdot G_{MIN}}} \quad (57).$$

$$V_{th} = \frac{k \cdot Temp}{q};\ V_{tho} = \frac{k \cdot Temp\_Normal\ (300K)}{q} \quad (58).$$

t_{di} is dielectric thickness, $\varepsilon_{r_{di}}$ is the relative permittivity of the gate dielectric and all other parameters are previously described. Γ controls the dependence of the channel conductance on the gate voltage overdrive and is also called the power law mobility factor. V_{aa} is minimum field effect mobility characteristic voltage. It is used to determine by tail states DOS. V_{aa} and γ are set in such a way that convergence becomes easy. TM is a temperature & bias independent value that describes combined DOS. G_{MIN} deep states DOS minimum density. V_0 deep states DOS characteristic voltage. V_e is the difference between normal and current temperature converted to equivalent voltage from the Boltzmann equivalent voltage-temperature relation, V_{th} is the equivalent voltage on variable temperature and V_{th0} is voltage allied on normal room temperature equivalent. Here flat band voltage [50] correction is considered as eq. (50) and becomes eq. (59).

$$V_{gfbe} = \frac{V_{MIN}}{2} \cdot \left[1 + \frac{V_{gfb}}{V_{MIN}} + \sqrt{\Delta^2 + \left(\frac{V_{gfb}}{V_{MIN}} - 1\right)^2}\right] \quad (59).$$

$$V_{gfb} = V_{gs} - V_{FB} \quad (60).$$

Here we should know that fundamentally (V_{FB}) flat band voltage is equal to $q\phi_m - q\phi_s$ difference between the contact work-function and the OSC work-function. Capacitance is an important characteristic of a thin-film transistor (TFT) that affects the device's switching speed, power consumption, and overall performance. The two main types of capacitance in a TFT are gate capacitance and channel capacitance, which can be expressed mathematically. The total capacitance of a TFT is the sum of these two capacitances and is an important parameter that affects the device's performance. The gate capacitance could be divided into two parts, the first is gate-drain (Cap_{gd}) and the second is gate-source (Cap_{gs}). These capacitances are calculated as:

$$Cap_{gs} = C_f + \frac{2 \cdot C_{gc}}{3} \cdot \left[1 - \left(\frac{V_{dsat} - V_{dse}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right] \quad (61).$$

$$Cap_{gd} = C_f + \frac{2 \cdot C_{gc}}{3} \cdot \left[1 - \left(\frac{V_{dsat}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right] \quad (62).$$

$$C_f = 0.5 \cdot \epsilon_{r_{di}} \cdot \varepsilon_0 \cdot W_{eff} \quad (63).$$

$$\epsilon_{r_{di}} = (t_{SiO2} + t_{PVT}) \cdot \frac{\epsilon_{PVT} \cdot \epsilon_{SiO2}}{\epsilon_{PVT} \cdot t_{SiO2} + \epsilon_{SiO2} \cdot t_{PVT}} \quad (64).$$

The channel capacitance could be estimated by a change in channel charge density with respect to the gate-to-source voltage.

$$C_{gc} = q \cdot \frac{dN_{sc}}{dV_{GS}} \quad (65).$$

Like eq. (54) the N_{sc} consists of two variables but in N_{sa} gamma dependency is eliminated and N_{sac} is introduced.

$$N_{sc} = \frac{N_{sac} \cdot N_{sb}}{N_{sac} + N_{sb}} \quad (66).$$

$$N_{sac} = \frac{\epsilon_{r_{di}} \cdot \epsilon_0 \cdot V_{gte}}{q \cdot t_{di}} \quad (67).$$

All the parameters and variables are discussed previously.

8. SIMULATION OF LOGIC CIRCUIT

Compared to unipolar inverters, where power is constantly dissipated through a load resistance, complementary circuits offer significantly reduced static and dynamic power consumption because one transistor operates in its off state. However, to obtain complementary inverters with a high gain, large noise margin, and good signal integrity, it is essential to have balanced charge carrier transport in the n-type and p-type transistors. The threshold voltage (V_T) is of particular importance because it determines the trip point of the inverter the input bias at which the gate inverts the output signal. For standard silicon complementary metal–oxide–semiconductor (CMOS) transistors, the threshold voltage at the onset of inversion can be accurately set by the amount of doping applied by ion implantation. But in OSC it isn't straightforward. The present state of the art in organic digital logic circuit creation and execution is highly complex in terms of manufacturing, with distinct p- and n-type OSC OTFTs having varied threshold voltages of CMOS technology which is

undesirable. As a result, distinct p- and n-type OSC complementary digital logic circuits are yet struggling to find a market fit. However, a unipolar-based digital inverter[51] circuit has advantages and disadvantages. In this work, our objective was to create a functional logic inverter circuit through a basic attempt. Regardless of the numerous basic causes behind each oscillatory conduct, the study of each oscillator is centered on measuring the initial conditions or the oscillator frequency precisely. Following the analysis and validation of these major properties, various figures of merit delineate the oscillators to allow comparison and categorization. According to the needs of the target application, these properties might be referred to as physical characteristics (integrability, resources, bias conditions) or frequency performance (quality factor Q, jitter, or phase noise).

The previously mentioned compact model is used for basic logic circuit emulation using only p-channel C8-BTBT-C8-based OTFTs. The zero-gate source load (ZGSL) type inverter circuit was developed. After that, a ring oscillator as shown in Figure 13(a) is utilized to examine OTFT. Figure 13(b) shows the output of the ring oscillator. We chose a monopolar arrangement with an equal threshold voltage and set an equal channel length for both the driver and load TFTs. The driver and load current are equivalent in the steady state. The simulation findings of the ring oscillator highlight its commendable performance, especially in terms of frequency of oscillation and power consumption. Initiating the oscillation involves a strategic process where the supply voltage (V_{DD}) undergoes a controlled ramp to -40 V within the initial 0.05 ms of the simulation. This deliberate voltage ramping technique serves as the catalyst for the oscillator to enter its oscillatory state. Post the initial Vdd ramp, the oscillator seamlessly transitions into a steady-state operation.

Notably, the simulated oscillation frequency stands at an impressive 1.6 kHz, with a delay time of 0.08 ms. This frequency is a testament to the oscillator's efficiency in swiftly toggling between high and low states. It is crucial to highlight that the frequency's robust performance is intricately linked to the magnitude of the load capacitances, underscoring the influence of circuit parameters on the oscillation behavior. Furthermore, the low power consumption of 1.5 milliwatts further accentuates the oscillator's viability for energy-efficient electronic applications. These findings collectively underscore the promising potential of the C8-BTBT-C8 OTFT-based ring oscillator in achieving a balance between high-frequency operation and low-power consumption, positioning it as a valuable component in advanced electronic circuits. Figure 13(b) shows the output of the ring oscillator. We chose a monopolar arrangement with an equal threshold voltage and set an equal channel length for both the driver and load TFTs. The driver and load current are equivalent in the steady state.

Two p-channel OTFTs are used in this circuit, one as a load transistor and the other as a driver. The load OTFT remains

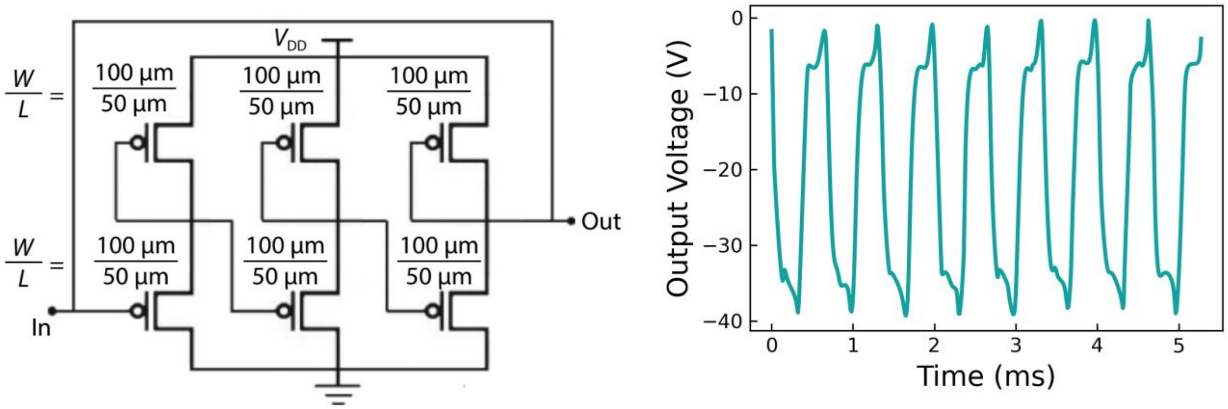


Figure 12. (a) Ring oscillator schematic. (b) Illustration of charge distribution at on state.

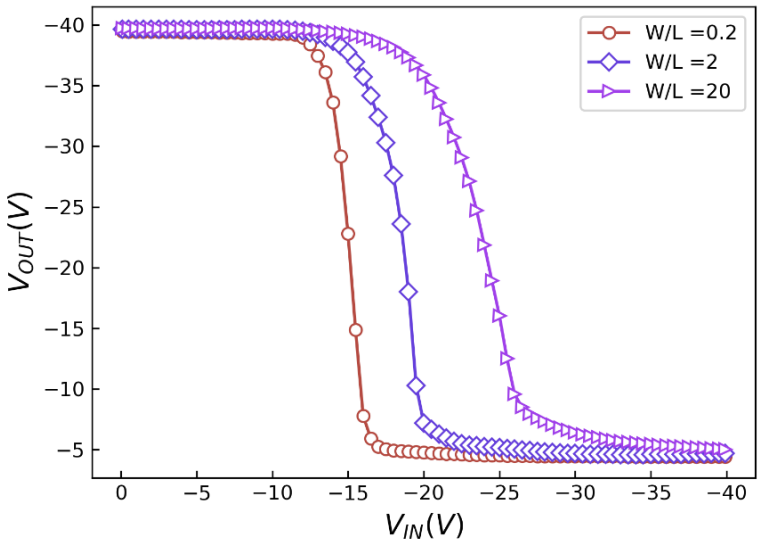


Figure 13. The inverter voltage transfer characteristics for various W/L ratios of the driver OTFT.

"on," but the driver OTFT alternates between "on" and "off" according to the input signal voltage. Once the input signal voltage is below the threshold voltage, the driver OTFT shuts off; when the voltage exceeds the threshold voltage, the driver OTFT switches on. The relative size of the load and driving OTFTs affect the inverter circuit's efficacy. The load OTFT, in particular, has a width (W) of 100 μm and a length (L) of 50 μm, resulting in a W/L ratio of 100/50. Figure 14 illustrates the voltage output characteristics plot of the circuit, which shows how the inverter reacts to varying input voltages for various W/L ratios changed in the driver OTFT (0.2,2,20).

9. CONCLUSION

We discuss the potential of organic electronics in the market. Some work on different materials, contact engineering, and other modeling are discussed. The process flow of any device modeling (material to device and circuits) is discussed. The TCAD modeling of C8-BTBT-C8 is performed with the help of device physics. The DOS is described well with the Gaussian and the tail distribution. Hopping, pool Frenkel, and band-like transportation are defined for this OSC, and the parameters are calculated by iteration method and some are found from the literature review. This model is simulated on the SILVACO TCAD platform. All the curves and performance parameters match within an acceptable margin of error. Then electrostatic modelling is done to improve performance depending on the structure. Finally, a compact model and circuit simulation are done to verify the model and to examine the potential for circuit realization. In the modeling, we realize that capacitance also depends upon charge distribution and DOS. At three points the W/L ratio is varied, and the effect of size is observed. The compact model could help in circuit realization. OTFTs could be established as a dominant player in the realm of large-area electronics with lower fabrication costs.

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