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Implementation of Taguchi Method in Improving the Logic Gates Performance based on Carbon Nanotube Field Effect Transistor Technology

M. F. Abdul Hadi[1], H. Hussin[1,*], M. Muhamad[1], Y. Abd. Wahab[2]

[1]School of Electrical Engineering, College of Engineering, Universiti Teknologi MARA, 40450 Shah Alam, Selangor, Malaysia
[2]Nanotechnology & Catalysis Research Centre, University of Malaya, Kuala Lumpur, Malaysia

ABSTRACT

The International Roadmap for Device and Systems (IRDS) 2022 has emphasized the potential of CNTFETs to replace CMOS technology. Therefore, the substitution of silicon with carbon nanotubes (CNTs) has the potential to open new possibilities for the semiconductor industry, due to their compact size and superior electrical properties. Thus, this project utilized Cadence Virtuoso software to develop an optimized CNTFET design using Taguchi method. In this design, the Taguchi method was implemented to determine the best combination of design parameter and material for optimum CNTFET performance. The design parameter and material that had been chosen were the diameter of carbon nanotube, dielectric material and oxide thickness. The optimized CNTFET model is implemented in circuit study to analyse the propagation delay and power consumption. Five circuits had been designed from the optimized CNTFET which are the inverter, AND, OR, NAND and NOR circuit. The Taguchi Optimization method resulted in significant reductions in the power-delay product (PDP) for all circuits examined, ranging from 7.9954% for the AND circuit to an exceptional 99.9622% for the inverter circuit. These findings highlight the potential for improved power efficiency and faster circuit operation when utilizing the Taguchi Optimization approach.

Keywords: Carbon nanotube, Taguchi method, power consumption, delay, ANOVA

1. INTRODUCTION

In the current era, technology is advancing and evolving at a breakneck pace. To sustain this forward momentum, the semiconductor and microelectronics industry has adopted Moore's Law as a guiding principle for technological enhancement. According to Moore's Law, the number of transistors on a chip roughly doubles every two years [1]. This principle has ignited fierce competition among companies in the semiconductor and microelectronics sector, as they vie to create high-performance devices that can meet the ever-increasing demands of modern society. To fulfill these requirements, the industry has been concentrating on the production of Metal Oxide Semiconductor Field-effect transistors (MOSFETs) for several decades [2]. The downsizing of MOSFETs permits a greater number of transistors to be integrated onto a single chip, resulting in improved circuit performance and enhanced functionality [3]. Nonetheless, due to physical constraints, the relentless adherence to Moore's Law may eventually lead to the pinnacle of MOSFET technology. Several nanoelectronic devices have emerged as potential alternatives to MOSFETs, aiming to address their inherent limitations. Among these innovative devices is the Carbon Nanotube Field-Effect Transistor (CNTFET). Carbon nanotubes (CNTs), essentially rolled-up single sheets of graphite, were first discovered by Japanese researcher Sumio Iijima in 1991 [4]. In CNTFETs, CNTs replace bulk silicon as the channel material, although the overall design closely resembles that of a standard MOSFET [5]. Prior research has indicated that CNTFETs offer

* Corresponding authors: hanimh@uitm.edu.my

superior performance in terms of propagation delay and power consumption when compared to MOSFETs[6]–[8]. To evaluate the performance of these transistors, one can observe the results when both types of transistors are incorporated into a circuit. Through circuit analysis, it becomes possible to extract data on propagation delay and power consumption. The CNTFET's enhanced performance can be attributed to the unique properties of carbon nanotubes, which allow for high current density and ballistic transport, facilitating efficient electron transfer between terminals [9].

While extensive research has been conducted on the CNTFET structure, there remains significant room for improvement to elevate its performance, particularly with regard to optimization techniques. Multiple methods are available for enhancing the performance of CNTFETs across various structures. Consequently, this study aims to pinpoint the optimal CNTFET structure capable of delivering superior performance in terms of propagation delay and power consumption. Propagation delay is a critical parameter in digital circuit design, dictating the time it takes for a signal transition to travel from input to output. Conversely, power consumption quantifies the electrical energy expended by the circuit during its operation.

2. METHODOLOGY

The objective of this research is to enhance the performance of the CNTFET by utilizing the Taguchi method to optimize key design parameters. These parameters encompass the diameter of the carbon nanotube (CNT), the thickness of the oxide layer, and the selection of dielectric materials. Through the optimization of these variables, improvements in the CNTFET's operational efficiency can be achieved. In the transistor level, the current ratio, I_{on}/I_{off} need to be observed during the optimization process. The I_{on}/I_{off} is the ratio between on-current, I_{on} and off-current, I_{off} which can be extracted in IV graph. The value of I_{on} is extracted when Vgs=Vdd while I_{off} is extracted when Vgs=0. To get a better CNTFET performance, I_{on} need to be larger while having I_{off} small. Thus, producing a CNTFET with larger I_{on}/I_{off} can optimize the capabilities of the CNTFET. The enhanced CNTFET configuration will subsequently be implemented in a basic logic circuit to conduct additional assessments of power consumption and delay.

2.1 Factor and Level of CNTFET Parameters

In order to enhance the efficiency of the CNTFET, three critical parameters were pinpointed: the carbon nanotube (CNT) diameter, the oxide layer thickness, and the selection of dielectric material. These design parameters have been consistently employed in previous research to improve CNTFET performance, with their specific value ranges established through prior studies and simulation outcomes.

The range of manipulated CNT diameters was determined by referring to previous simulations of CNTFETs, and options of 0.783 nm, 1.251 nm, and 2.000 nm were chosen [10][11]. The sizes of the oxide layer were also ascertained based on prior simulated models, offering choices of 0.5 nm, 1.0 nm, and 1.5 nm. [12][13]. The dielectric layer in the transistor was varied such as Sio_2 (3.9), HfO_2 (16), and ZrO_2 (25) [14]. The parameter is tabulated in Table 1. The parameter varied into three levels: level 0, level 1, and level 2. Level 0 represents the smallest value for each parameter, while level 2 represents the largest value for each parameter. Every combination between parameter and level is simulated using Cadence Virtuoso software based on Stanford University CNFET model [15]. The structure of Stanford University CNFET model is shown in Figure 1.

Table 1 Factor and level used for each of the parameters to simulate the CNTFET model

Symbol	Parameters	Level		
		0	**1**	**2**
A	**Diameter of CNT, nm**	0.783	1.251	2.000
B	**Oxide Thickness, nm**	0.5	1	1.5
C	**Dielectric Materials**	3.9	16	25

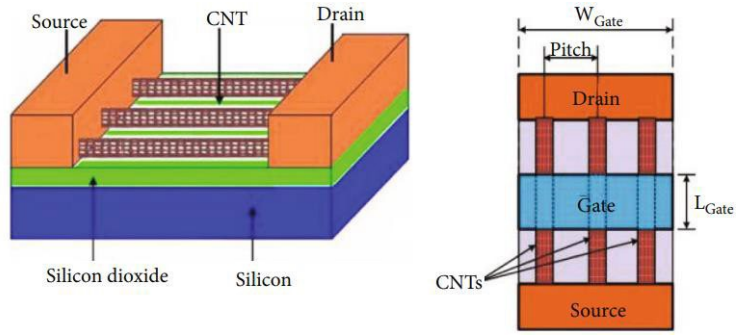

Figure 1. Carbon nanotube field effect transistor (CNFET). (a) Schematic. (b) Top view [15]
Taguchi method.

In order to boost the performance of CNTFETs and meet the demands of the industry, it is imperative to employ enhanced tools and techniques for further optimization. The Taguchi method stands out as a statistically proven technique that offers exceptional value in addressing this challenge. This approach provides practicality by efficiently resolving complex issues with minimal experimental trials across various domains. Through the utilization of the Taguchi method, a significant reduction in the time required for experimental investigations can be achieved. This method allows for the thorough examination of the impact of multiple factors on CNTFET performance.

The Taguchi method leverages the signal-to-noise ratio (SNR) as a measure for assessing the quality characteristic of CNTFETs. The selection of SNR type depends on the nature of the response, as indicated by Equations (1-3). When the objective is to maximize the response variable, the LTB type of SNR is chosen. Conversely, if the goal is to minimize the response variable, the STB type of SNR is employed. The NTB type of SNR is utilized when there is a specific target value desired for the response variable.

Larger the better (LTB): $$\frac{S}{N} = -10\log\frac{1}{n}\left(\sum\frac{1}{y^2}\right) \quad (1)$$

Smaller the better (STB): $$\frac{S}{N} = -10\log\frac{1}{n}\left(\sum y^2\right) \quad (2)$$

Nominal the better (NTB): $$\frac{S}{N} = 10\log\left(\frac{\hat{y}^2}{s_y^2}\right) \quad (3)$$

2.3 Investigation on CNTFET Logic Gates

Propagation delay, t_p is a crucial response parameter of digital circuit design that determines the time delay for a signal transition to propagate from input to output. Propagation delay refers to the time delay that occurs when a signal transition propagates from input to output due to binary input signals changing in value as in Figure 2. The t_p can be determined by using Equation 4 where t_{pHL} represents the time it takes for the output to change from a high to a low level when the input changes. It is measured between the 90% and 10% levels of the output signal's amplitude. Meanwhile, t_{pLH} indicates the time it takes for the output to change from a low to a high level when the input changes. Like t_{pHL}, it is measured between the 90% and 10% levels of the output signal's amplitude.

$$\frac{t_{pHL} + t_{pLH}}{2} = t_p \tag{4}$$

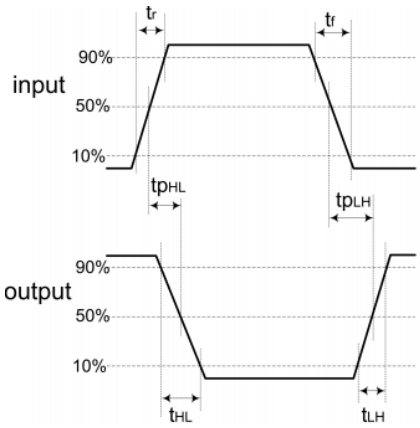

Figure 2. Calculation of the propagation delay of the circuit.

When a digital circuit transitions, a transient phase occurs in which both the high and low transistors exhibit partial conduction, enabling a current to pass through the circuit. This leads to a momentary spike in power usage, referred as dynamic power [16]. The study allows for the calculation of dynamic power dissipation in the circuit by analyzing the current and voltage values from the DC response graph during transition events. On the other hand, static power dissipation, often referred to as leakage power, pertains to the power consumption of a digital circuit or electronic device when it is not actively engaged in switching or any circuit-related operations. [16]. The total power consumption in the circuit, as expressed in Equation 5, results from the combination of dynamic power dissipation and static power dissipation. This static power dissipation is attributed to the leakage currents that traverse the transistors when they are in an off-state, generating power dissipation.

$$Ptotal = Pdynamic + Pstatic \tag{5}$$

Hence, after determining the most significant combination parameters for CNTFET (optimized CNTFET), those parameters are applied to the basic logic circuit which is the inverter, AND gate, OR gate, NAND gate, and NOR gate circuit as in Figure 3 to study its performance in terms of propagation delay and power consumption.

3. RESULTS AND DISCUSSION

3.1 Orthogonal Array

By using the simulated value of the CNTFET's I_{on} /I_{off}, the SNR of the I_{on}/I_{off} can be calculated for each of the combination factors. For this research study, the Minitab 21.2 had been used to calculate the SNR value. The Larger-the-Better (LTB) formula from Equation 1 is used to evaluate the value of the SNR. The LTB formula is selected for this optimization process is due to the I_{on} /Io_{ff} need to be high in order to get the best CNTFET performance. This is parallel to Taguchi's objective which to find the combination of parameter settings that maximize the SNR. By optimizing for the highest SNR, you aim to improve product quality and minimize the effects of noise and variability. The result from this process is tabulated in Table 2.

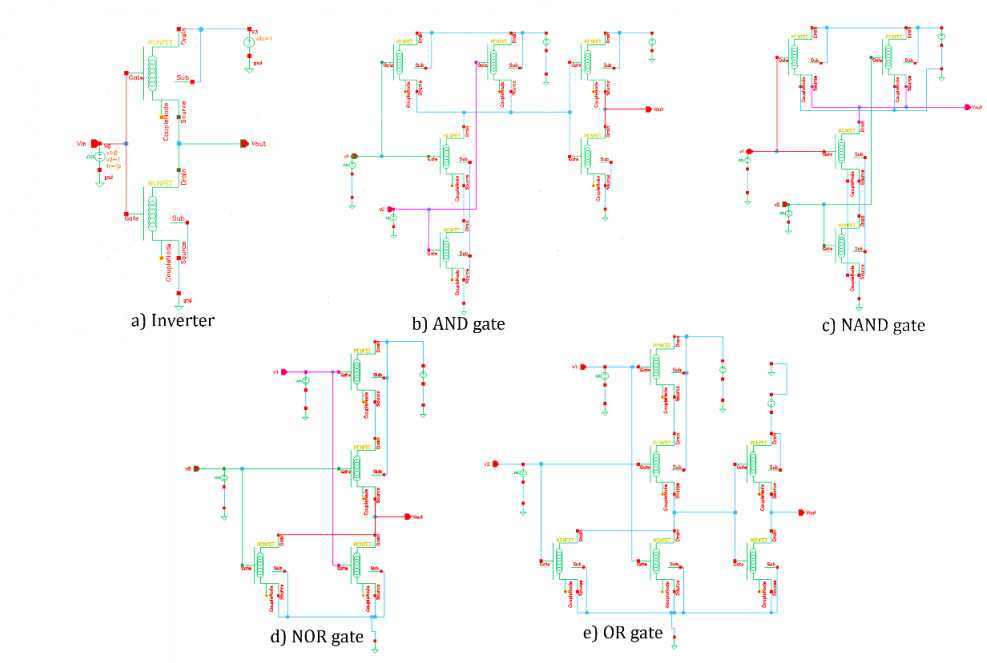

Figure 3. The optimized CNTFET is applied into the logic circuit such as a) Inverter, b) AND gate, c) NAND gate, d) NOR gate and e) OR gate.

3.2 Signal-to-Noise Ratio

From the SNR in the orthogonal array, the Minitab 21.2 will generate a SNR graph. The result for the SNR graph is displayed in Figure 4. The combination factors that produced the highest I_{on}/I_{off} was A0B0C2. This was the best combination to produce the optimum I_{on}/I_{off} for CNTFET, representing the 0.783 nm of CNT diameter, 0.5 nm of oxide thickness and ZrO_2 (25) as the dielectric material. The result of highest SNR in Table 2 is aligned with the highest simulated values indicates that the simulation model is a good representation of the real system. This alignment can boost confidence in the accuracy of the simulation model and its ability to predict real-world outcomes for Taguchi application for optimization.

The SNR graph can also determine the most significant parameters towards I_{on} /I_{off}. This can be calculated by observing the slope of each process parameter which is the difference between the value of SNR at the highest point and the value SNR at the lowest point. In the case of the I_{on} /I_{off} response variable, the most significant contribution parameter is the diameter of CNT followed by dielectric material and oxide thickness.

3.3 Analysis of Variance (ANOVA)

The ANOVA table includes various statistics such as degrees of freedom (DF), sequential sum of squares (Seq SS), mean square, F-value, P-value, and contribution percentage. In the context of this study, the primary interest lies in assessing the contribution percentages of parameters that underwent modifications during the optimization process in the CNTFET. Table 3 reveals that the CNT diameter exhibited the most significant contribution percentage at 99.26%, while oxide thickness contributed a mere 0.04%, and the dielectric material accounted for 0.68% of the variance. It is clear from the results that the CNT diameter (99.26%) is the most predominant parameter affecting the I_{on} /I_{off} of the CNTFET. The percent of error for I_{on} /I_{off} (0.02%) is considerably low. It was also shown that the dielectric material is the second most effective parameter according to ANOVA statistical analysis followed by oxide thickness of the CNTFET.

The result from Table 3 have a similar trend to the result from SNR graph in Figure 4 in term of parameter contribution effect towards $Ion/Ioff$ of the CNTFET. These two methods (Taguchi method and ANOVA) consider diameter of the CNT have a dominant effect towards I_{on}/I_{off} followed by dielectric material and oxide thickness. However, the ANOVA can provide a better measurement in term of percentage value which can be analyse easily in the ANOVA table.

Table 2 Orthogonal array for simulated and calculated SNR of $Ion/Ioff$ in cadence virtuoso simulation

Exp no	Factors			Simulated values	SNR values
	A	B	C	I_{on}/I_{off}	I_{on}/I_{off}
1	0	0	0	4.360E+09	192.790668
2	0	1	1	1.350E+10	202.6060582
3	0	2	2	1.576E+10	203.9505926
4	1	0	0	2.264E+06	127.0993082
5	1	1	1	3.988E+06	132.0142411
6	1	2	2	4.455E+06	132.9767673
7	2	0	0	2.910E+02	49.27801277
8	2	1	1	5.972E+02	55.52294374
9	2	2	2	6.640E+02	56.44330889
10	0	0	1	1.651E+10	204.356534
11	0	1	2	1.721E+10	204.713297
12	0	2	0	2.208E+09	186.8783322
13	1	0	1	4.727E+06	133.4923128
14	1	1	2	4.931E+06	133.8589559
15	1	2	0	1.267E+06	122.0572196
16	2	0	1	6.947E+02	56.83636231
17	2	1	2	7.103E+02	57.02885879
18	2	2	0	1.957E+02	45.83215797
19	0	0	2	1.953E+10	205.8149681
20	0	1	0	2.808E+09	188.9675774
21	0	2	1	1.170E+10	201.3650872
22	1	0	2	5.787E+06	135.2495637
23	1	1	0	1.588E+06	124.0151379

24	1	2	1	3.682E+06	131.3211659
25	2	0	2	7.861E+02	57.90950166
26	2	1	0	2.242E+02	47.01395695
27	2	2	1	5.374E+02	54.6061385

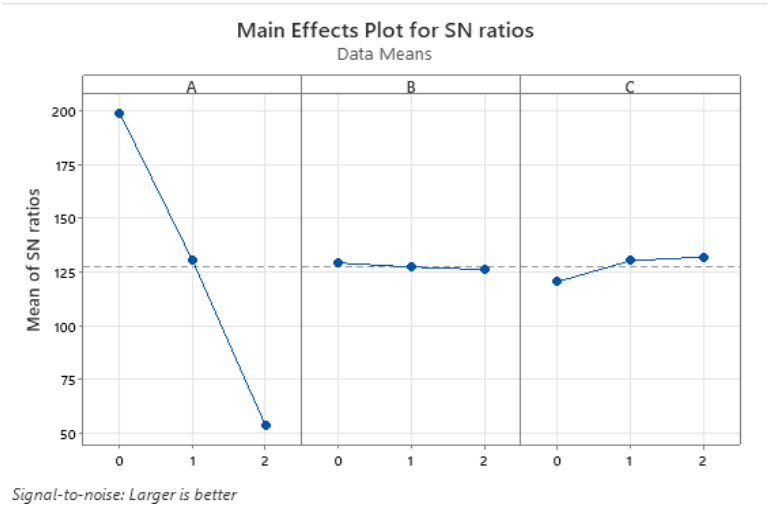

Figure 4. SNR graph of the CNTFET I_{on}/I_{off} .

Table 3 Analysis of variance for transformed response

Factors	DF	Seq SS	Contribution	F-Value	P-Value
A	2	0.427233	99.26%	55175.90	0.0000000000000000
B	2	0.000181	0.04%	23.39	0.0000057982186168
C	2	0.002946	0.68%	380.49	0.0000000000000001
Error	20	0.000077	0.02%		
Total	26	0.430437	100.00%		

3.4 Circuit Application

In this research, we employed the Taguchi method to fine-tune three critical parameters, which were subsequently incorporated into the circuit design. The most effective combination for achieving the optimal I_{on}/I_{off} in CNTFETs involved a CNT diameter of 0.783 nm, an oxide thickness of 0.5 nm, and the use of 〖ZrO〗_2 (25) as the dielectric material of choice. This optimized CNTFET configuration is expected to significantly enhance performance, particularly in terms of propagation delay.

To evaluate its efficacy, we designed five circuits using Cadence Virtuoso, including an inverter, AND gate, OR gate, NAND gate, and NOR gate. The results, specifically the extracted propagation delay, are presented in Table 4. These optimized circuit designs were then compared to several existing designs. Notably, most circuits resulting from the Taguchi optimization exhibited superior propagation delay performance compared to previous research. The inverter circuit from Taguchi optimization can provide the shortest propagation delay compared to the model in [17] and [18] with 4.2 ps. Furthermore, the NAND and NOR circuit also have the best propagation delay as opposed to the rest of the other model with both have 6.8 ps. However, for the AND

circuit, the model design in [18] produced the shortest delay compared to the model design in [19] and Taguchi optimized model. The Taguchi optimized model generated 47.9% longer propagation delay compare to model in [18]. The OR circuit from the CNTFET design in [19] outperformed the rest of the model design. There are only 10.1% differences between this model design and the Taguchi optimized design.

Table 4 Propagation delay comparison of CNTFET circuit

Design	**Propagation Delay (ps)**				
	Inverter	AND	OR	NAND	NOR
Taguchi Optimization design	4.2	29.0	29.0	6.8	6.8
Stanford University CNFET model	0.50	1.7	1.7	0.65	0.65
[17]	95.1	-	-	161.0	99.5
[18]	17.40	17.8	45.9	17.9	67.0
[20]	-	-	-	62.7	-
[19]	-	25.3	26.2	-	-

The result of DC response from the simulated circuit designs can be used to determine the power consumption of the circuit. The result of the extracted power consumption is tabulated in Table 5. These optimized circuit designs are compared with several existing designs. From the results, all of the circuit design from Taguchi optimization have better power consumption compared to the previous research in [17]–[20].

Table 5 Power consumption comparison of CNTFET circuit

Design	**Power Consumption (uW)**				
	Inverter	AND	OR	NAND	NOR
Taguchi Optimization design	4.34E-6	2.50E-6	4.56E-6	2.50E-6	4.54E-6
Stanford University CNFET model	9.65E-2	1.019E-4	1.044E-1	5.221E-2	1.044E-1
[17]	0.261	-	-	0.353	0.388
[18]	0.206	0.478	0.994	0.472	0.297
[20]	-	-	-	4.860	-
[19]	-	0.140	0.150	-	-

The performance of the circuit also can be evaluated using power-delay product (PDP). PDP is a measure of the trade-off between the power consumption of a circuit and the time it takes to perform the switching event. Commonly, this parameter had been used to measure the quality and performance of the devices [21]. PDP value can be obtained by multiplying the total power consumption and propagation delay of the circuit [22][23]. The PDP comparison data between circuit designed from the CNTFET optimized model and Stanford University CNFET model is presented in Table 6.

Table 6 The PDP data between the circuit designed from the CNTFET optimized model and Stanford University CNTFET model

Model	Power-delay product (PDP), x E-23 J				
	Inverter	AND	OR	NAND	NOR
Taguchi Optimization	1.82	7.27	13.2	1.7	3.09
Stanford University CNFET model	4830	17.3	17800	3390	6790

The data reveals a significant and consistent decrease in the power delay product (PDP) when comparing the Taguchi Optimization method with the Stanford University CNFET model across various logic circuits. The Taguchi Optimization approach delivered impressive PDP reductions, ranging from 7.9954% to 99.9622%, for inverter, AND, OR, NAND, and NOR circuits. These results underscore the effectiveness of Taguchi Optimization in enhancing both power efficiency and circuit speed, presenting substantial prospects for designing energy-efficient and high-performance circuits.

4. CONCLUSION

The implementation of the Taguchi method to optimize the CNTFET design parameters yielded positive results. This method effectively identifies the most optimal combination of design parameters that can maximize the performance of the CNTFET device. Based on this study, it was concluded that a CNT diameter of 0.783 nm, an oxide thickness of 0.5 nm, and ZrO_2 (25) as the chosen dielectric material can significantly enhance the I_{on}/I_{off}. Furthermore, by employing the Taguchi method in conjunction with ANOVA, it was determined that the CNT diameter has the greatest influence on the I_{on}/I_{off}, accounting for 99.26% of the observed contribution. The optimized CNTFET design not only improves circuit performance in terms of propagation delay and power consumption but also exhibits favourable characteristics in specific circuit configurations. The study revealed that the Taguchi optimized CNTFET circuit achieved the best PDP value compared for each of the circuit design. Thus, by utilizing this method, developers can focus on optimizing a specific design parameter to enhance the overall performance of the CNTFET.

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REFERENCES

[1] S. Tyagi, “Moore’s law: A CMOS scaling perspective,” in Proceedings of the International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA, (2007) pp. 10– 15.

[2] A. M. Hashim, H. H. Ping, & C. Y. Pin, “Characterization of MOSFET-like carbon nanotube field effect transistor,” AIP Conf. Proc., vol. 1217, (2010) pp. 11–18.

[3] S. Chopra & S. Subramaniam, Int. J. Innov. Sci. Eng. Technol., vol. 2, no. 4, (2015) pp. 1055–1057.

[4] W. Hoenlein, Hoenlein, W. Kreupl, F. Duesberg, G. S. Graham, A. P. Liebau, M. Seidel, R. Unger, E.., Mater. Sci. Eng. C, vol. 23, no. 6–8, (2003) pp. 663–669.

[5] S. K. Sinha & S. Chaudhury, J. Semicond., vol. 35, no. 11 (2014) pp. 114002.
[6] N. Syamira & H. Hussin, ECS J. Solid State Sci. Technol., vol. 9, no. 4, (2020) p. 041003.
[7] M. Khatri, A. Sharma, A. Mehra, & S. Anand, "Comparative Analysis of 20NM Based CNTFET for Different Logic Circuits," Proc. 2nd Int. Conf. Trends Electron. Informatics, ICOEI 2018, no. 2, (2018) pp. 1–5.
[8] A. K. V. V. Sarma, "A Comparison between MOSFET based and CNTFET based Analog to Digital Converter," in IEEE Proc. (2018) pp. 2634–2637.
[9] Y. Wu, X. Lin, & M. Zhang, J. Nanomater., vol. 2013 (2013), pp. 1-17.
[10] B. P. Shrivastava, "Low power, high speed carbon nanotube FET based level shifter," in Proceedings of the International Conference on Inventive Computing and Informatics, ICICI 2017, (2018) pp. 273–277.
[11] A. Laribi & A. G. Bouazza, Int. J. Electr. Comput. Eng., vol. 8, no. 6, (2018) p. 4941
[12] M. F. Abdul Hadi, H. Hussin, M. Muhamad, N. Soin, & Y. A. Wahab, "Effects of Different Oxide Thicknesses on the Characteristics of CNTFET," in Proceedings - 2021 IEEE Regional Symposium on Micro and Nanoelectronics, RSM 2021, IEEE, (2021) pp. 58–61.
[13] S. Ziauddin Ahmed, M. S. Shawkat, M. I. H. Chowdhury, & S. M. Mominuzzaman, "Current-voltage characteristics of ballistic schottky barrier GNRFET and CNTFET: Effect of gate oxide thickness," in 2015 IEEE 10th International Conference on Nano/Micro Engineered and Molecular Systems, NEMS 2015, IEEE, (2015) pp. 388–390.
[14] S. R. V. N. R. Shailendra, "Analysis of quantum capacitance on different dielectrics and its dependence on threshold voltage of CNTFET," in IEEE Proc., (2017) pp. 213–217.
[15] P. Wong, "Stanford University Virtual Source CNFET Model." https://nano.stanford.edu/downloads/vs-cnfet-model.
[16] S. A. Pon & V. Jeyalakshmi, 2020 6th Int. Conf. Adv. Comput. Commun. Syst. ICACCS 2020, (2020) pp. 115–121.
[17] S. I. Sayed, M. M. Abutaleb, & Z. B. Nossair, "Optimization of CNFET Parameters for High Performance Digital Circuits," Adv. Mater. Sci. Eng., vol. 2016, (2016) pp. 1-9.
[18] C. Yalung, D. Tantraviwat, S. Uatrongjit, & W. Yamwong, "Impact of High-k Materials and Tube Numbers on CNFET Gate's Performances," in IEEE Proc., IEEE, (2023) pp. 66–72.
[19] A. Raina, S. Dewan, & P. Reena Monica, "Energy Efficient Digital Circuits Using Hybrid MTJ and CNTFET," in Proceedings - 2020 6th IEEE International Symposium on Smart Electronic Systems, iSES 2020, (2020) pp. 127–132.
[20] P. Venkatramana, P. Nagarajan, & S. J. Basha, 2023 International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI), IEEE, (2023) pp. 1–5.
[21] Z. Han, J. Phys. Conf. Ser., vol. 1754, no. 1, (2021) 012131.
[22] P. A. G. Sankar & K. Udhayakumar, J. Semicond., vol. 35, no. 7, (2014) pp. 1–13.
[23] N. Nandhagopal, A. Vasantharaj, V. M. Jeevitha, & S. Ayisha, Int. J. Adv. Sci. Technol., vol. 29, no. 5, (2020) pp. 10213–10219.