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# Impact of Nanowire Radius and Channel Thickness with High-k Gate Dielectric in GAA-JLT

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**ABSTRACT**

*As the transistor's size becomes smaller, degradation in the short-channel effects (SCEs) becomes more apparent. This leads to research work on multi-gate transistors such as the Fin-Field Effect Transistor (FinFET) and Gate-All-Around (GAA) transistor, where the 3D architecture have been shown to have superior performance as compared to conventional planar transistor. Transistor without junctions (JLT) which realizes a single type of doping has also been gaining popularity for biosensor applications due to its superior electrostatic performances in terms of Drain-Induced Barrier Lowering (DIBL), off-state leakage current (Ioff) and Subthreshold Slope (SS). In this work, the impact of changes in parameters such as the gate oxide material, nanowire radius and channel thickness toward the performance of a Gate-all-around JLT (GAA-JLT) have been studied using TCAD simulator. It was found that smaller nanowire radius and thicker channel produces lower DIBL, Ioff and SS, with the use of HfO2 as gate oxide materials shows better results than Si3N4. Meanwhile, the impact of parameters variations seemed to be negligible on the on-state current (Ion). The outcome of this work can be used as a basis to understand the impact of structural parameters variations towards the performance of a more complex GAA-JLT structure.*

**Keywords:** Gate-all-around (GAA), junctionless transistor, nanowire radius, channel thickness, gate oxide materials

## 1. INTRODUCTION

As the trend of device downscaling continues, conventional transistor with junctions is found to have its limitations and challenges. One of the challenges involves the formation of ultra sharp doping profiles at the source and drain junctions during the manufacturing process. In order to address this limitation, transistors which have uniform doping profiles between the channel and the source/drain region are introduced, known as the junctionless transistor (JLT). Meanwhile, 3D transistor structures such as the Fin-field Effect Transistor (FinFET) and Gate-all-around (GAA) transistor serve as alternative to improve the short-channel effects (SCEs) often associated with shorter gate length devices and planar transistor [1]–[9]. Figure 1 shows an example of a planar, FinFET and GAA transistor. One of the biggest advantages of GAA is that the silicon thickness can be comparable (or even double of) the gate length ($L_g$), instead of 1/2-2/3 $L_g$ in FinFET [10] . In this work, the impact of varying the gate oxide material, nanowire radius and channel thickness towards the electrostatic performance of a gate-all-around junctionless transistor (GAA-JLT) was investigated in terms of the Drain-Induced Barrier Lowering (DIBL), off-state leakage current ($I_{off}$) and Subthreshold Slope (SS).

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DIBL is measured as the difference in the threshold voltage, $V_{th}$ between a low and high drain bias, $V_d$ as shown in (1), where low $V_d$ is typically between 50-100 mV whereas high $V_d$ is typically 1 V. The barrier height's reduction for channel carriers at the edge of the source occurs as a result of drain electric field upon application of high $V_d$.

In this work, DIBL is extracted at drain current, $I_d$ of 10-7 A for two drain voltages i.e. $V_d$ = 50 mV and $V_d$ = 1.0V. Meanwhile, $I_{off}$ refers to $I_d$ @ $V_g$ = 0 V while SS is measured as in (2). One of the applications of GAA-JLT are in nanoelectronics with ferroelectric nanosheet and in biosensors [11]. Other area of studies by other researchers include the efficiency in heat dissipation and better thermal stability in GAA-JLT beyond CMOS alternative [12].

$$DIBL = (V_{thlin} - V_{thsat}) / (V_{dsat} - V_{dlin}) \quad (1)$$

$$SS = (dV_g/d\log_{10}I_d) \quad (2)$$

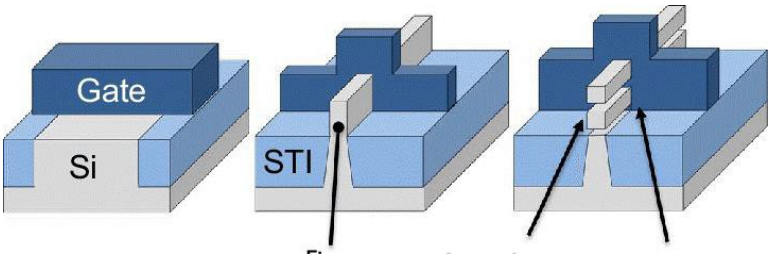


**Figure 1.** Three-dimensional view of (a) planar (b) FinFET and (b) GAA transistor.

## 2. METHODOLOGY

A gate-all-around junctionless transistor (GAA-JLT) is modeled in ATLAS 3D in order to study the impact of variations in parameters such as the gate oxide materials, nanowire radius and channel thickness as listed in Table 1. First, two different high-k dielectric materials of $HfO_2$ (k = 25) and $Si_3N_4$ (k = 7.9) with equivalent oxide thickness (EOT) of 1.2 nm were used in the simulations. The use of high-k dielectric materials to replace the conventional $SiO_2$ enables the dielectric thickness to be increased at the same capacitance, thereby suppressing the leakage current. Table 2 summarizes the thickness of the gate dielectric used in the simulations as obtained from (3), where $t_{high\text{-}k}$ refers to the thickness of the high-k dielectric, $k_{SiO2}$ is the dielectric constant of $SiO_2$ and $k_{high\text{-}k}$ is the dielectric constant of the high-k dielectric materials.

$$EOT = t_{high\text{-}k} (k_{SiO2}/k_{high\text{-}k}) \quad (3)$$

Next, the impact of variations in the nanowire radius was studied, followed by the variations in the channel thickness for both $Si_3N_4$ and $HfO_2$. Some of the physical models being used in the simulations include the Shockley-Read-Hall (srh) recombination model using fixed lifetimes and field-dependent mobility model (fldmob).

**Table 1** Parameter variations in the simulations of GAA-JLT

| Parameters | Types / Values |
|---|---|
| Gate oxide materials | $Si_3N_4$, $HfO_2$ |
| Nanowire radius | 10 nm, 12 nm, 14 nm |
| Channel thickness | 10 nm, 18 nm, 20 nm |

Table 2 Dielectric materials and the corresponding gate oxide thickness used in the simulations

| High-k dielectric material | Dielectric constant | Gate oxide thickness (nm) | EOT (nm) |
|---|---|---|---|
| $Si_3N_4$ | 7.9 | 2.43 | 1.2 |
| $HfO_2$ | 25 | 7.69 | 1.2 |

## 3. RESULTS AND DISCUSSIONS

### 3.1 Results for Variations in Nanowire Radius (10, 12 and 14 nm)

First, the nanowire radius was varied for 10, 12 and 14 nm to see the effects on the electrical characteristics. Table 3 summarizes the overall results obtained for both $HfO_2$ and $Si_3N_4$ while Figure 2 shows an example of the corresponding Id-Vg graph extracted for $HfO_2$ only.

It can be seen that smaller nanowire radius (of 10 nm) exhibits the best performance in terms of lowest leakage current ($I_{off}$), DIBL and SS for both dielectrics of $HfO_2$ and $Si_3N_4$. For instance, the results of $I_{off}$ obtained is in the range of ~ $10^{-13}$ A/μm for both $Si_3N_4$ and $HfO_2$ with nanowire radius of 10 nm which is comparable to reported fabricated GAA nanowire transistor reported in [5]. The change in the nanowire radius from 10 to 12 and to 14 causes the $I_{off}$ to increase in one decade. As the radius is reduced, the gate has better control over the channel as compared to influence exerted by the source and drain [13].

It is apparent however that $HfO_2$ shows superior electrostatic performance than $Si_3N_4$ in terms of $I_{off}$, DIBL and SS for all the 10, 12 and 14 nm nanowire radius variations. For instance, the DIBL for $HfO_2$ are 22% lower than $Si_3N_4$ at 10 nm radius and the same trend can be observed for 12 and 14 nm radius consecutively. This is in agreement with [7] that states $I_{off}$ reduces and subsequently SS is also reduced to its theoretical limits as relative permittivity is raised. [7] also state that $V_{th}$ increases when $I_{off}$ decreases as the dielectric constant of high-k oxide is raised, leading to reduction in DIBL. However, the effects seem to be negligible on the on-state current, $I_{on}$ where variations in the nanowire radius and dielectric materials seem to give the results in ~$10^{-5}$ A/μm for all.

**Table 3** Results of DIBL, $I_{off}$ and $I_{on}$ for different nanowire radius of 10nm, 12nm and 14nm for $HfO_2$ and $Si_3N_4$

| High-k dielectric | Nanowire radius (nm) | DIBL (mV/V) | $I_{off}$ (A/μm) | $I_{on}$ (A/μm) | Subthreshold Slope (mV/dec) |
|---|---|---|---|---|---|
| $HfO_2$ | 10 | 17.9 | $2.33x10^{-13}$ | $4.11x10^{-5}$ | 61.80 |
| $HfO_2$ | 12 | 40.0 | $2.01x10^{-12}$ | $5.64x10^{-5}$ | 67.00 |
| $HfO_2$ | 14 | 69.5 | $1.82x10^{-11}$ | $5.64x10^{-5}$ | 74.57 |
| $Si_3N_4$ | 10 | 23.2 | $3.11x10^{-13}$ | $3.83x10^{-5}$ | 63.20 |
| $Si_3N_4$ | 12 | 51.7 | $2.99x10^{-12}$ | $5.09x10^{-5}$ | 69.87 |
| $Si_3N_4$ | 14 | 83.2 | $2.55x10^{-11}$ | $5.09x10^{-5}$ | 77.83 |

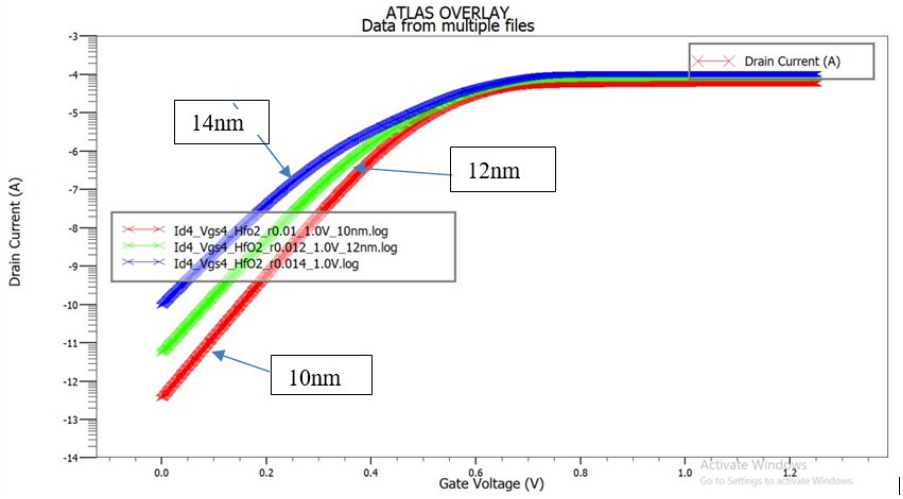


**Figure 2.** Plot of log Id-Vg for GAA-JLT with HfO2 gate oxide for different nanowire radius of 10nm, 12 nm and 14 nm.

### 3.2 Results for Variations in Channel Thickness (10, 18 and 20 nm)

Next, the channel thickness was varied for 10, 18 and 20 nm to see the effects on the electrical characteristics. It can be seen from Table 4 that thinner channel (10 nm) leads to degradation in the electrical parameters of DIBL, $I_{off}$ and SS. In terms of different dielectric materials, $HfO_2$ with higher dielectric constant again exhibits better performance as thicker gate oxide can be employed, thus mitigating issues such as direct tunnelling and leakage current [14]. From the results, it can be seen that the degradation in DIBL is more apparent for $Si_3N_4$ as compared to $HfO_2$. For instance, as the thickness of the channel decreases from 20 to 10 nm, the degradation in DIBL for $HfO_2$ double to ~ 50%. However, the impact is quite small and negligible for SS.

**Table 4** Results of DIBL, Ioff and SS for different channel thickness of 10 nm, 18 nm and 20 nm for $HfO_2$ and $Si_3N_4$

| High-k dielectric | Channel Thickness (nm) | DIBL (mV/V) | $I_{off}$ (A/µm) | $I_{on}$ (A/µm) | Subthreshold Slope (mV/dec) |
|---|---|---|---|---|---|
| $HfO_2$ | 10 | 35.79 | $9.49x10^{-12}$ | $5.25 \times 10^{-5}$ | 62.49 |
| $HfO_2$ | 18 | 21.05 | $5.22x10^{-13}$ | $5.25 \times 10^{-5}$ | 61.58 |
| $HfO_2$ | 20 | 17.89 | $3.57x10^{-13}$ | $5.25 \times 10^{-5}$ | 61.45 |
| $Si_3N_4$ | 10 | 47.37 | $1.72x10^{-11}$ | $5.24 \times 10^{-5}$ | 64.09 |
| $Si_3N_4$ | 18 | 28.42 | $8.69x10^{-13}$ | $5.23 \times 10^{-5}$ | 63.00 |
| $Si_3N_4$ | 20 | 23.15 | $5.80x10^{-13}$ | $5.23 \times 10^{-5}$ | 62.74 |

### 3.3 Results of Electrostatic Performance with $HfO_2$ and $Si_3N_4$ as Gate Dielectric

Table 5 and 6 shows the summary of the electrostatic performance of the GAA-JLT with varied nanowire radius and channel thickness respectively, when compared using different gate dielectric materials. Earlier in Table 3, it can be seen that the degradation of the DIBL, $I_{off}$ and SS is more apparent in $Si_3N_4$ as compared to $HfO_2$ for all nanowire radiuses. The same trend can be observed in Table 4 when various channel thicknesses were simulated.

From Table 5 it can be observed that changing the gate dielectric material from $HfO_2$ to $Si_3N_4$ has quite a profound impact on the results of DIBL, while the effect on SS is quite small and negligible. By using $Si_3N_4$, the DIBL degrade for about 16% - 20% for all nanowire radius of 10, 12 and 14 nm, whereas the degradation in SS is only of 2% - 4%.

**Table 5** Results of % degradation of DIBL and SS for different nanowire radiuses for $Si_3N_4$ when compared to $HfO_2$

| Nanowire radius (nm) | % degradation in DIBL | % degradation in SS |
|---|---|---|
| 10 | 22.8 | 2.2 |
| 12 | 22.6 | 4.1 |
| 14 | 16.5 | 4.2 |

From Table 6, the same trend can be observed when the channel thickness is varied. Again, using $Si_3N_4$ as the gate oxide materials leads to degradation in DIBL, while the effect on SS is quite negligible. By using $Si_3N_4$, the DIBL degrade for about 22% - 26% whereas the degradation in SS is only around ~ 2%.

**Table 6** Results of % degradation of DIBL and SS for different channel thickness for $Si_3N_4$ when compared to $HfO_2$

| Channel thickness (nm) | % degradation in DIBL | % degradation in SS |
|---|---|---|
| 10 | 24.4 | 2.5 |
| 18 | 25.9 | 2.3 |
| 20 | 22.7 | 2.1 |

## 4. CONCLUSION

In this work, implications of different nanowire radius and channel thickness towards the performance of a GAA-JLT were investigated, by using two different high-k dielectric materials of $HfO_2$ and $Si_3N_4$. It was found that smaller nanowire radius and thicker channel thickness produces lower DIBL, $I_{off}$ and SS with $HfO_2$ of higher dielectric constant showing better electrostatic performance.

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