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Simulation and Characterization of an Inverter Logic Gate by Utilizing InGaAs-Based Planar Devices

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ABSTRACT

Electronic circuits known as logic gates can perform basic logical operations like inverters, AND, and OR gates. These logic gates serve as the basis for digital electronics, and they are a common component in various electronic devices, such as computers, smartphones, and other types of digital systems. This research presents an inverter logic gate made of planar devices, which have significantly simpler structures than multi-layered transistors and diodes, namely the self-switching diode (SSD) and side-gated transistor (SGT). The inverter logic gate is realized by simply connecting both SSD and SGT in parallel. The electrical characteristics and performances of the inverter logic gate are assessed based on InGaAs material using SILVACO Inc.'s ATLAS device simulator software. The simulation results show that the functionality of the proposed planar inverter is comparable to that of a conventional inverter logic gate based on the standard truth table of the device. This has demonstrated the feasibility of building logic gates using a combination of SSDs and SGTs. In addition, the planar structure of SSD and SGT allows for a relatively low-cost device fabrication process as well as offering a high-frequency operation due to low parasitic elements in the devices.

Keywords: Inverter, self-switching diode, side-gated transistor

1. INTRODUCTION

In computer science, electronics, and telecommunications, logic gates are electronic devices that carry out logical operations on one or more binary inputs resulting in a binary output based on predefined rules. In an integrated circuit, the logic gate is one of the most important components, and it additionally performs an essential part in various electronic technology applications. Molecular logic gates applications have recently begun replacing conventional silicon-based electronic computers in research on biological sensors, heavy metal ion detection, disease diagnosis, and treatment [1].

Utilizing nanometer-scale unipolar planar devices such as the self-switching diode (SSD) and side-gated transistor (SGT) in realizing logic gates is an alternative method, and can be used in high-frequency applications [2], [3]. Both SSD and SGT are made in only one nanolithography step by insulating trenches in a semiconductor layer [4]. Previously, the realization and fabrication of SSDs have been demonstrated using a variety of materials including silicon, zinc oxide, and GaAs as reported in [5]- [7]. Utilizing "green" materials with high mobility such as graphene for

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environmental sustainability will enhance the devices' working frequencies and rectifying abilities, as well as their responsiveness and noise-equivalent power [7]. More details on SSDs and SGTs can be found elsewhere [8]- [10].

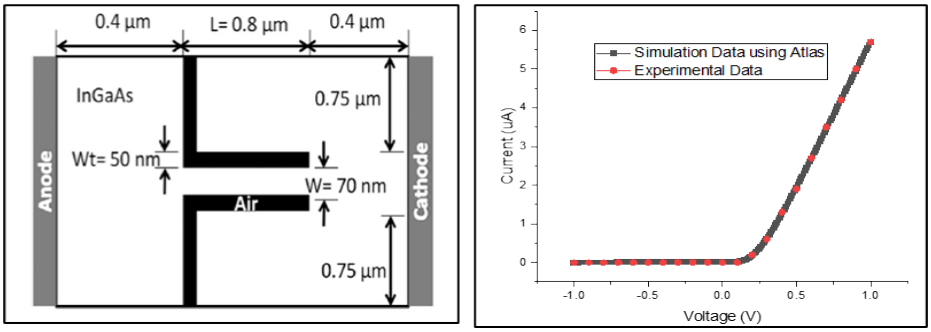
The fabrication of a typical logic gate includes several steps. Additional fabrication steps make processes more difficult and expensive. The use of planar SSD and SGT technology for realizing logic gates will definitely reduce the whole device fabrication process as well as lowering the relative cost of the process. Previously, Song et al. constructed a simple logic OR gate using two InGaAs-based SSDs connected in series and separated by an insulator trench [4]. Thus, this research proposed the realization of an InGaAs-based inverter logic gate by utilizing SSD and SGT that can operate at room temperature. This is similar to the inverter reported by Jin et al. in [11] but using zinc oxide thin film material. The characterization and performance of the InGaAs-based inverter logic gate proposed in this work are evaluated using SILVACO Inc.'s ATLAS device simulator software.

2. METHODOLOGY

2.1 InGaAs-based SSD Validation

This research describes the simulation of a new concept of InGaAs-based SSD inverter logic gate design that uses a single nanolithography fabrication process to create insulating trenches in a semiconductor layer. The first stage in creating an InGaAs-based SSD is to validate the simulator, material specifications, and physical models used for the device. Identifying the physical structure of the device, determining the physical model applied, and examining the electrical characteristics are the three main steps in doing device analysis using SILVACO Inc.'s ATLAS device simulator software. The result obtained will then be compared with those from earlier studies to validate the device for usage in the following work.

Figure 1 (a) displays the optimized architecture for zero-bias rectification of an InGaAs-based SSD. The device's characterization was carried out in SILVACO Inc.'s ATLAS device simulator software, a two-dimensional (2D) device simulator, using a top-view simulation that mainly used the x-y plane. The geometry of the device's etched trenches on an InGaAs-based SSD uses air as the dielectric (black area). The dimensions of the channel length (L), width (W), and trench width (W_t) of the SSD are set to be 0.80 μm, 0.07 μm, and 0.05 μm, respectively. The simulation parameters were $N_{db} = 1 \times 10^{17}$ cm^{-3} for the estimated of approximate negative background doping and $\sigma = -3.75 \times 10^{11}$ cm^{-2} for the interface charge density [12]. Figure 1(b) shows the comparison between our simulation result generated by the SILVACO Inc.'s ATLAS device simulator and the current-voltage (I-V) characteristic result of the published work in [13].

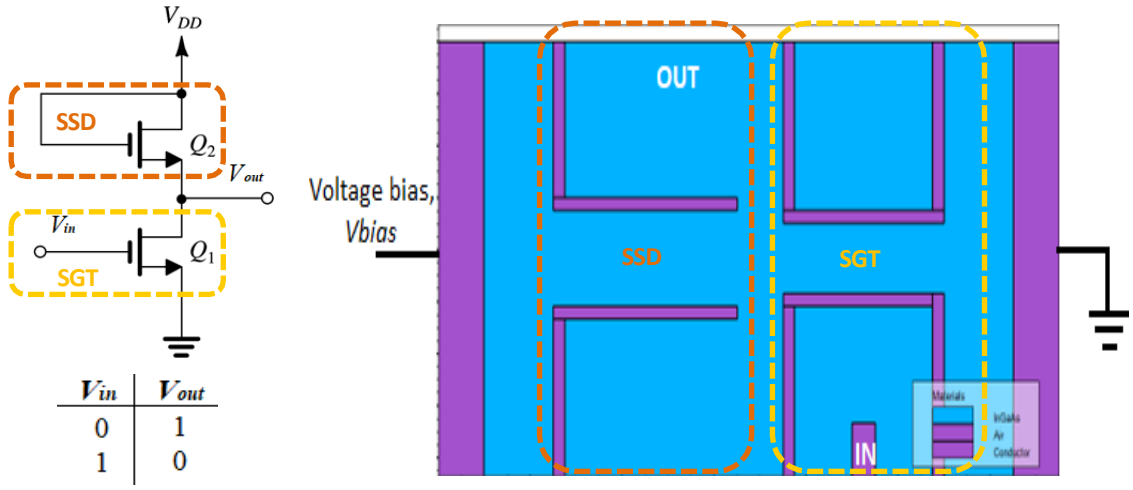


(a) (b)

Figure 1. (a) InGaAs-based SSD architecture optimized for zero-bias rectification [13]. (b) I-V characteristics of the InGaAs-based SSD validation simulation produced by the SILVACO Inc.'s ATLAS device simulator.

2.2 InGaAs-based SSD's Inverter Logic Gate Design

A basic inverter logic gate has a single input and output. The input signal is either complimented or reversed, resulting in an output opposite to the input. The inverter logic gates schematic and its function table, as shown in Figure 2(a), the InGaAs-based SSDs and SGTs were utilized to create the structure of the logic gate [see Figure 2(b)]. The simulation, by means of a SILVACO Inc.'s ATLAS device simulator, was carried out using various SSD and SGT width sizes. By adjusting the SSD and SGT width sizes, the output of the inverter was made as swing-free as possible. The structural analysis potential distribution, the electron velocity distribution, and the functioning of the inverter logic gate have all been evaluated concerning the input.



V_{in}	V_{out}
0	1
1	0

(a) (b)

Figure 2. (a) Inverter logic gates schematic with its function table. (b) Top view image of inverter logic gates based on InGaAs SSD and SGT structures.

3. RESULTS AND DISCUSSION

3.1 Electrical Characteristics and Potential Distribution

InGaAs-based inverter logic gate was simulated with input value given to the terminal IN, V_{in}, with the voltage value was either 0 V (LOW) or 1.5 V (HIGH). The value of V_{bias} was set at 1.5 V. The investigation of various width of SGT, W_{SGT} is shown in Figure 3 with a fixed SSD with W_{SSD} of 0.27 µm. Table 1 summarised the input and output voltage results for the optimal outcome, which demonstrated the basic operation of an inverter gate by using SGT and SSD components with trench widths of 0.26 µm and 0.27 µm, respectively. As can be observed, the logic voltage levels obtained were poorer than the expected values. Nevertheless, in principle, the operation of the inverter was correct and further development and study on this device can be done in future.

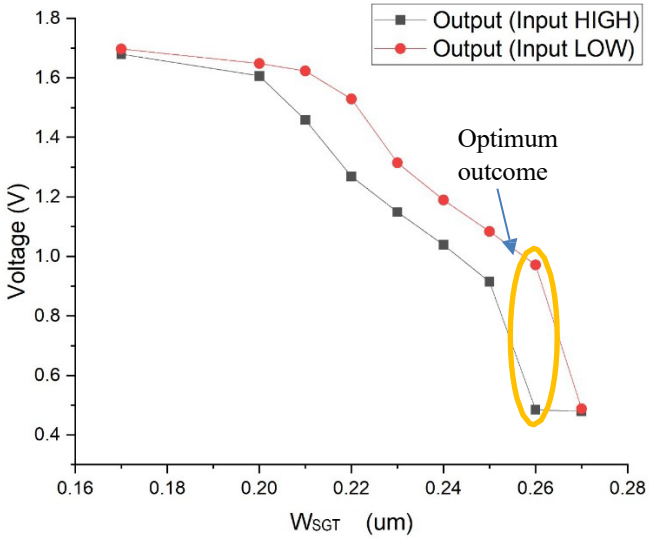


Figure 3. Analysis of SGT trench width (WSGT) with various sizes with a fixed SSD with WSSD of 0.27 µm.

Table 1 InGaAs-based Inverter logic gate simulation result.

SGT & SSD size (µm)	Simulated Input (V)	Simulated Output (V)
	0.0233 (LOW)	0.9715
0.26 & 0.27	1.5125 (HIGH)	0.4846

Figure 4 depicts a measured voltage transfer curve for inverter ports with V_{in} varies from 0 – 1.5 V. The simulation results show the correct operation of an inverter. However, the outputs do not come close to the ground or 1.5 V of the supply voltages. The highest output voltage obtained (i.e., 0.9715 V) is limited by the resistive voltage division due to the leakage current through the SGTs. On the other hand, the lowest voltage obtained (i.e., 0.4846 V) is limited might be due to the possibility that the current flowing across SGT is only some percentages of the intended value. Markku et al. has discussed this in [14]. The potential distribution and cutting point for the provided input voltages of 0 V and 1.5 V are shown in Figure 5(a) and Figure 5(b).

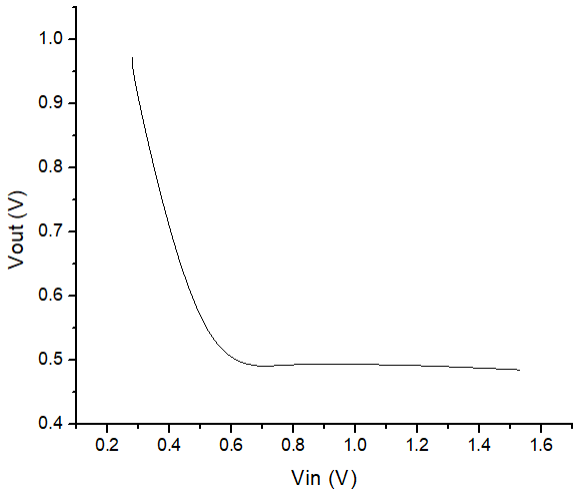


Figure 4. Input-output voltage characteristic curve.

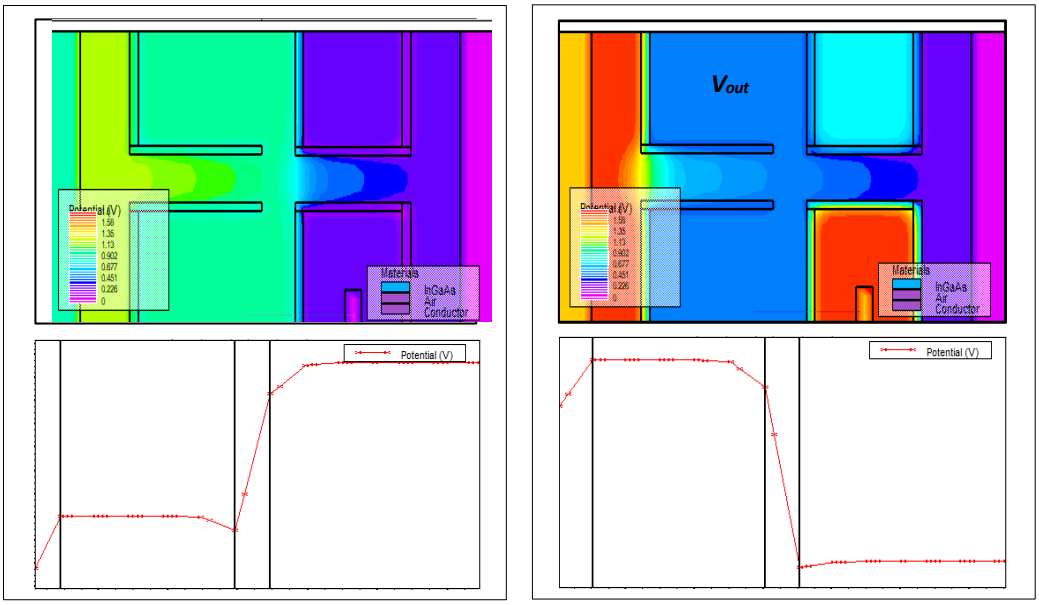
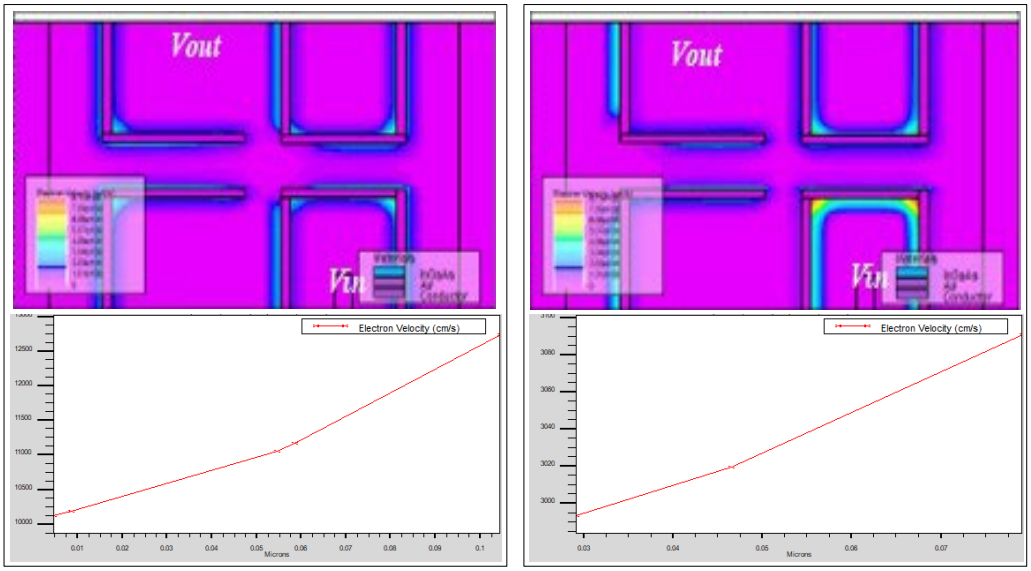


Figure 5: Potential distribution in InGaAs-based Inverter logic gate for given input I (a) Vin = 0 V (b) Vin =1.5 V.

3.2 Electron Velocity

Figures 6(a) and 6(b) illustrate the analysis of electron velocity for input V_{in} of 0 V and 1.5 V, respectively. The cutline of the output is taken at the V_{out} point to look at the output electron velocity. Figure 6(a) illustrates the outcome of a given input V_{in} of 0 V, which causes the SSD channel to be open and the SGT channel to close, resulting in a current obtained straight from the device's HIGH (~ 1.5 V) anode voltage. While when the V_{in} is delivered at 1.5 V, the SSD channel will be closed, the SGT channel will be opened, and the output will be directly connected to the ground, causing the output potential to become LOW (~ 0 V). The outcome of V_{in} LOW results in an electron velocity of 11,500 cm/s, whereas V_{in} HIGH results in an electron velocity of 3,000 cm/s.



(a) (b)

Figure 6. Electron velocity in InGaAs-based Inverter logic gate for a given input
(a) Vin = 0 V (b) Vin = 1.5 V

4. CONCLUSION

In conclusion, utilizing the SILVACO Inc.'s ATLAS device simulator software, a working InGaAs-based inverter logic gate consisting of an SSD and SGT has been successfully developed and simulated. The simulated design demonstrated an acceptable output result and a good inverter logic gate output response to the input with SGT and SSD components with trench widths of 0.26 µm and 0.27 µm. The maximum output voltage obtained was 0.9715 V for input LOW, and the lowest voltage obtained was 0.4846 V for input HIGH. V_{in} LOW produces an electron velocity of 11,500 cm/s, whereas V_{in} HIGH produces an electron velocity of 3,000 cm/s. The outcomes of this InGaAs-based inverter logic gate characterization may help create a logic gate for an advanced integrated circuit and serve as a guide and foundation for advanced design circuits and fabrication that may be employed in circuits for digital systems.

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