

Design and performance analysis of ALU architectures based on quantum-dot cellular automata

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ABSTRACT

Quantum-dot cellular automata (QCA) nanotechnology addresses the limitations of Short-Channel Effects (SCE) in metal-oxide-semiconductor field-effect transistors (MOSFETs) at the ultra-nanoscale. The area required for QCA-based circuits is significantly less than that for MOSFET circuits because logic formation relies entirely on electron flow. QCA nanotechnology offers high speed and reduced energy dissipation. The arithmetic and logical unit (ALU) is a key component of a processor. Therefore, this paper evaluates various ALU designs in QCA nanotechnology and provides a competitive analysis. The different quantitative measurements are considered for comparison purposes. The literature offers various multi-layer implementations of ALUs. There is a need for an efficient design of a single-layer ALU in QCA nanotechnology that utilizes a minimal number of QCA cells and clocking phases. An ALU design without any crossing mechanism and a multi-layer configuration consists of only 57 QCA cells and has a 0.75 clock delay. Compared to existing designs, the proposed ALU achieves up to 94% reduction in QCA cell count, 97% reduction in layout area, and nearly 99.6% improvement in area-delay product, based on worst-case values from previously reported designs. A comparative evaluation against multiple benchmarks demonstrates superior area, delay, and functional output performance. These findings underscore the proposed ALU's potential for scalable, low-power QCA-based processors.

Keywords: QCA, ALU, Latency, Energy dissipation, Nanoscience, VLSI

1. INTRODUCTION

The era of metal-oxide-semiconductor field-effect transistors (MOSFETs) touches the fundamental limits of materials. Further reducing the material's size generates secondary effects on the dominant mode. These secondary effects create problems, especially in the ultra-nanoscale region. Over the past few decades, complementary metal-oxide-semiconductor (CMOS) technology has dominated the very-large-scale integration (VLSI) industry and reached several significant milestones. The semiconductor industry has followed Moore's Law for years, which states that the transistor density will be doubled on integrated circuits approximately every two years. This trend has driven continual gains in performance, power efficiency, and cost per function. However, current device performance and new architectures in ultra-nanoscale (sub-10 nm) reach the extreme limits of Moore's Law due to inevitable physical limits related to increased leakage current, power density, and quantum tunneling effects. The costs and complexity of manufacturing increase significantly at advanced nodes. Since Moore's Law is approaching its limits and will inevitably plateau, it is necessary to investigate novel device architectures and computing paradigms to sustain performance scaling and meet modern application demands. [1]. The major drawback of CMOS technology is the short-channel effects (SCEs). It is also known for secondary effects. In the ultra-nanoscale regime, SCEs increase and degrade performance.

The main secondary effects that alter transistors' performance are drain-induced barrier lowering (DIBL), sub-threshold voltage, punch-through, gate-induced barrier lowering (GIBL), threshold voltage roll-off, mobility degradation, and velocity saturation. Most of these secondary effects have less impact on circuits for higher technology nodes. However, technology node scaling produces a limitation for further minimizing the dimensions of a transistor. It is the biggest challenge for the circuit designers to tackle this problem. The rapid growth of portable systems requires area-efficient transistor architecture to be effectively utilized in small-scale applications [2]. The small-scale transistor consumes less power and is therefore more energy efficient. The response time of the small-sized transistor is also fast due to minimizing the gate size. Therefore, high speed, low area, and low energy dissipation are the most desirable features for today's portable electronic gadgets. The conventional MOSFET device deviates from its fundamental operation if the size of the material is too small. SCEs challenge the scaling down the size of the MOSFETs in the ultra-nanoscale region [3-5]. Figure 1 represents the evolution of microchips over time and the accuracy in predicting Moore's Law.

Scaling the power supply is needed for the scaled devices. The devices' supply and threshold voltages are scaled with the same factor to manage the same type of voltage scaling process. The scaling of the threshold voltage causes a

significant leakage power issue. It is a challenge for low-power circuit applications [6]. Beyond performance concerns, ultra-scaled transistors will also face serious reliability issues due to negative bias temperature instability (NBTI) and hot carrier injection (HCI), as well as manufacturing limits in lithography and yield. Hence, alternative methods need to be explored to further advance electronic systems. Various other transistor technologies, such as Fin Field-Effect Transistor (FinFET), Carbon Nanotube Field-Effect Transistors (CNTFET), and Graphene Nanoribbon Field-Effect Transistors (GNRFET), have been widely explored to overcome the device scaling challenge [7]. CNTFETs and GNRFETs are carbon-based transistor technologies that use carbon nanotubes and graphene nanoribbons as channel materials, respectively. CNTFETs and GNRFETs overcome silicon MOSFET scaling limitations through their one-dimensional channel geometry and superior electrical properties, particularly by mitigating short-channel effects and improving carrier mobility. The channel material used in CNTFETs is made up of carbon nanotubes, typically single-walled carbon nanotubes (SWCNTs), which are created by rolling up a sheet of graphene into a cylindrical shape. Graphene can also be manufactured as a nanostructure by etching to form nanoribbons (GNRs), which exhibit one-dimensional electronic transport. Even though there is limited research comparing quantum-dot cellular automata (QCA), CNTFETs, and GNRFETs, QCA performs better than CMOS equivalent for error-tolerant design in terms of power, area, and delay. QCA technology also reduces power dissipation because there is no current flow, unlike transistor-based approaches.

Moore's law: The number of transistors per microprocessor

Moore's law is the observation that the number of transistors in an integrated circuit doubles about every two years, thanks to improvements in production. It was first described by Gordon E. Moore, the co-founder of Intel, in 1965.

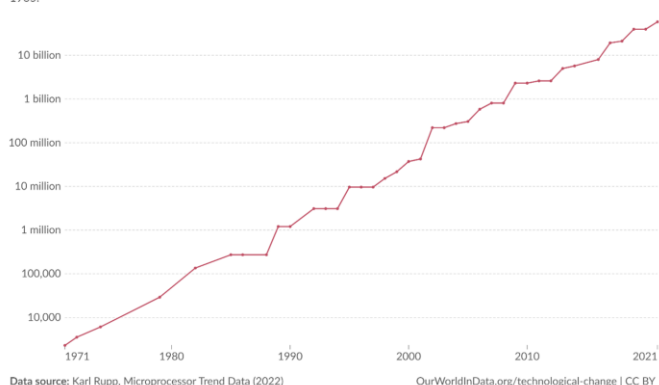


Figure 1. Evolution of microchips over time [8].

These alternative transistor technologies manage the scaling issue at specific nodes, but further scaling is also a tough job after a particular technology node. Therefore, researchers are exploring transistor-free concepts for the circuit's implementation. The transistor-free concept overcomes all the scaling-related issues in the nanoscale regime. In the future, various novel technologies, including transistor-free architectures, QCA, single-electron transistors (SET), and other beyond-CMOS concepts, show great potential. These new paradigms can help alleviate device limitations to build ultra-dense, energy-efficient, and high-speed systems for generations of computing in the future. The significant differences in CMOS and QCA technology are shown in Table 1.

Table 1. Difference between CMOS and QCA technology.

Feature	CMOS Technology	QCA Technology
Basic Element	Transistor (MOSFET)	QCA Cell (4 quantum dots, 2 electrons)
Information Encoding	Voltage levels (VDD, GND)	Electron position (polarization)
Signal Propagation	Current flow	Electron repulsion (Coulomb interaction)
Power Dissipation	Higher (due to leakage currents)	Lower (no current flow, only electron movement)
Size Scaling	Limited by short-channel effects	Better scaling potential in the nanoscale
Clocking Mechanism	No inherent clocking (needs external)	Intrinsic clocking (4-phase clocking)
Switching Speed	Limited by carrier mobility	Faster due to Coulombic interactions
Implementation Complexity	Established fabrication processes	Still under research, complex to fabricate

1.1. Overview of QCA

QCA nanotechnology is a transistor-free concept based on the atomic level [9, 10]. This concept is based on the movement of electrons in a lattice. The logic implementation depends on the actual position of the electrons in a structure [11]. QCA nanotechnology presents numerous advantages that are crucial for the advancement of future electronic systems. Compared to MOSFETs, QCA nanotechnology exhibits lower energy dissipation, a smaller physical footprint, and higher operational speeds. It also effectively mitigates secondary effects typically associated with conventional technologies [12, 13]. It means that QCA nanotechnology can be adopted for future system generation.

The QCA device fabrication process is critical, and different techniques can be employed, such as metal-dot QCA, Molecular QCA, and semiconductor QCA. Each technique has unique characteristics and challenges regarding precision, stability, scalability, and temperature requirements. QCA circuits are susceptible to temperature, and most QCA circuits, such as metal dot and semiconductor-based, require cryogenic temperature (nearly 0 kelvin) for stable operation, which dramatically limits any practical applications. However, molecular QCA has been suggested as a way to create QCA devices that work at room temperature, although this is still a new area of research.

Although QCA circuits do not necessarily conduct current, power will dissipate in circuits due to electron tunneling between quantum dots, operational clocks, and thermal noise. Power dissipation in QCA is notably less than in CMOS circuits. The energy expended on each event switch can be in the attojoule (aJ) range, allowing for ultra-low power uses, although the assessment and regulation of the power consumption is still a challenge. QCA nanotechnology has a far greater device density than conventional CMOS. The

distances between cells are on the order of tens of nanometers, and without the transistors and interconnect wire of CMOS, there is potential to pack more logic into a unit area. This gives QCA value for processors, memories, and signal processors, where the device needs to be small and fast.

In addition to logic circuits, QCA has also been investigated for the design of random access memory (RAM) and read only memory (ROM) architectures, flip-flops, latches, and registers. For QCA-based memory structures, the secondary advantages of potential non-volatility and lower power levels make them interesting, although implementing the writing operation at high speed remains an issue.

Several defects can occur in QCA circuits, including cell misalignment, cell displacement, missing or extra cells, thermal noise, and quantum decoherence. To guarantee circuit reliability, error tolerance strategies are being developed, including fault-tolerant majority gates, redundant layouts, and error correction circuits. Outside of ALUs and logic gates, QCA is being investigated for Quantum-dot-based sensors, Secure cryptographic hardware, Nano-scale Field-Programmable Gate Arrays (FPGAs), and Neuromorphic computing infrastructures. These applications all leverage the advantages of QCA, such as small sizes, fast operation, and low power dissipation.

1.2. QCA Cell Basics

The implementation of the QCA circuits is completed with the help of QCA cells [14, 15]. The QCA cell is the primary unit for QCA nanotechnology. The functionality of the QCA cell depends on the location of the electrons available in the quantum dots of a cell. There is the possibility of having two electrons in a cell due to the electrostatic force [16]. Binary equivalent logics are identified in QCA nanotechnology for designing digital logic circuits. The binary logic '0' or '1' is selected based on the position of electrons in a cell [17]. The representation of a cell is given in Figure 2, which shows binary logic '0' and '1'.

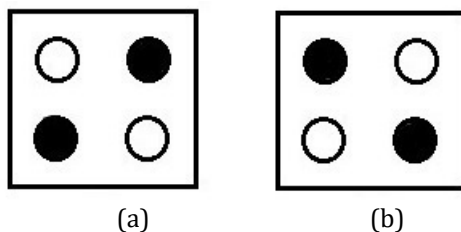


Figure 2. Cell representation as (a) binary '1' (b) binary '0'.

The logic formation requires QCA wires. The connection of QCA cells in a horizontal or vertical plane forms a wire for the QCA nanotechnology, which behaves similarly to the traditional electrical wire [18]. The locations of electrons in QCA wire depend on the overall impact of neighbouring cells, which determines a specific logic function [19]. A wiring system in QCA nanotechnology is depicted in Figure 3.

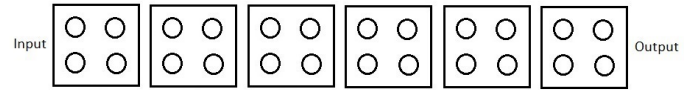


Figure 3. A wiring system in QCA nanotechnology

1.3. Clocking Mechanism

The clocking method is the other critical concept in QCA circuits [20]. QCA circuits do not need an external power supply; the clocking method must be applied to execute the function. QCA technology is energy-efficient due to its power supply-less operation [21]. This means the information flows from cell to cell using the electrostatic force between the neighbouring cells. The clocking method consists of four phases: switch, hold, release, and relax [22]. These phases are represented by the different coloured cells for easy understanding. The clocking method is applied in sequence, i.e., it starts from the switch and ends at the relaxation phase [23]. The clocking system in the QCA system is shown in Figure 4.

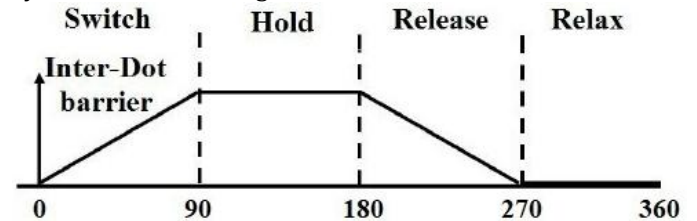


Figure 4. A clocking system in QCA nanotechnology

1.4. Crossing and Wire layout

The crossover is another essential operation in QCA circuits [24]. It is needed when crossing wires, similar to an electrical wire, is essential. A single-layer or multi-layer structure can be utilized for crossover purposes. A single-layer structure is always preferred. A multi-layer structure requires a minimum of three layers to flow signals properly. In a single-layer configuration, there are two scenarios when the cells lack a direct connection. The first possibility is between the switch and release phases, and the second is between the hold and relax phases [25]. These unique possibilities of clocking phases are the backbone for crossing the wires in logical crossover. Figure 5 depicts the single-layer crossing schemes.

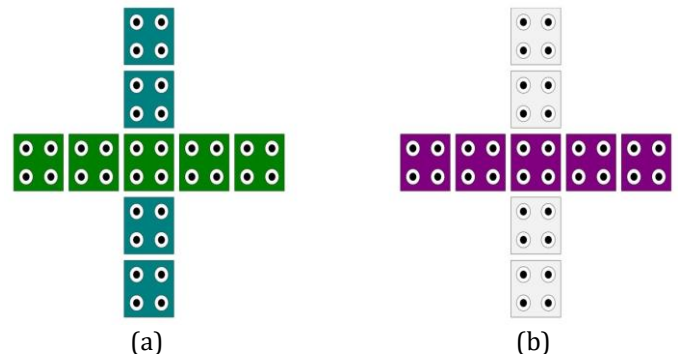


Figure 5. A single-layer crossing (a) first and third phases, (b) second and fourth phases.

Implementing circuits in a multi-layer design is difficult due to the physical structure of QCA-based circuits. The layers need to be correctly connected vertically. The external input-output ports can be assembled at the first or last layer. All the layers are defined individually, and connections are made sequentially [26]. The final layer contains the crossover connection, while the intermediate layers pass the logic values using the vertical values. Designing the multi-layer structures for the large circuits is complicated because the risk of improper connections is too high.

1.5. QCA Logic Gates

The digital logic circuit design in QCA nanotechnology is based on implementing fundamental gates [27]. The NOT gate is designed with the QCA cells' corner-to-corner connections. Input is provided to one cell, while the output is taken from the corner-connected cell. The other fundamental logic gates are designed with the help of a majority gate in QCA nanotechnology. Hence, a majority gate is sufficient to implement AND and OR logic gates in QCA nanotechnology. A three-input majority gate is required to design two-input AND and OR logic gates. One input of the majority gate is kept fixed polarized for generating two input AND and OR gates [28]. The logic functions of a NOT gate and a three-input majority gate are given in equations 1 and 2, respectively.

$$\text{Output} = \overline{IN1} \quad (1)$$

$$\text{Output} = IN1.IN2 + IN2.IN3 + IN1.IN3 \quad (2)$$

Here, IN1, IN2, and IN3 are the input 1, input 2, and input 3, respectively. In equation 2, if IN3 is zero, then it produces two input AND gates. If IN3 is one, then it produces two input OR gates. The QCA layouts for the NOT and a three-input majority gate are shown in Figure 6 [29].

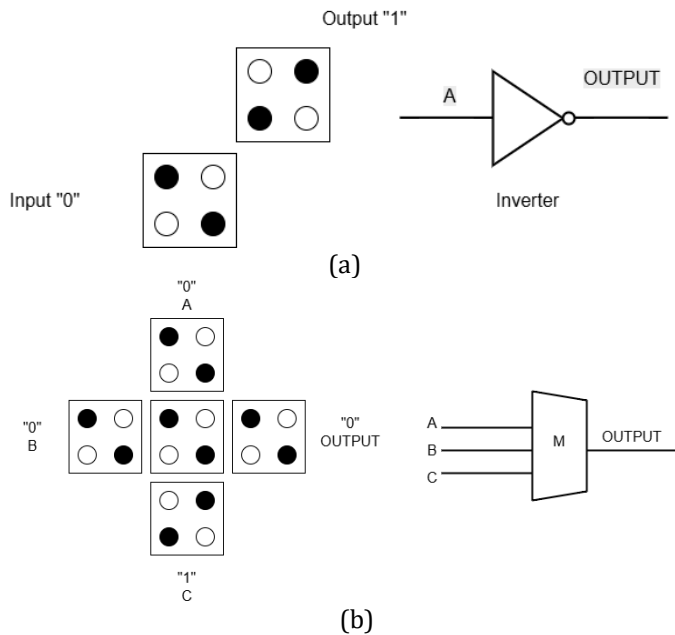


Figure 6. (a) NOT gate, (b) Three-input majority gate.

The three-input majority gate serves as a basic element in QCA and provides a foundation for universal logic design in

QCA circuits. The canonical Boolean expression of the three-input majority gate is given by Equation (3)

$$M(A, B, C) = AB + BC + AC \quad (3)$$

In Equation 3, the output of the majority gate is determined by the input values, and a high logic '1' in any two inputs will provide the high output value, and in other cases it remains low. In a majority gate, fixing one of the inputs to a constant logic value (1 or 0) will provide the conventional OR and AND logic operations, respectively.

Using a majority Gate for AND/OR shown in Equations (4) and (5):

$$\text{AND}(A, B) = M(A, B, 0) \quad (4)$$

$$\text{OR}(A, B) = M(A, B, 1) \quad (5)$$

This property illustrates the versatility and reconfigurability of the majority gate and is an effective substitute for multiple traditional logic gates. Further, using majority logic gates reduces circuit area, power dissipation, and complexity, which are beneficial in a QCA-based nanoelectronics design. In addition, researchers leverage the properties of the majority gate to build larger, more complex logic systems that include multiplexers, adders, and ALUs with minimal gate count and a compact layout.

The symmetric nature of the majority gate also creates design robustness, which is especially important in nanotechnology when fabrication tolerance specifications are needed. In addition, using majority logic can simplify clock zone alignment, and some designs developed with it also exhibit similar signal propagation paths.

1.6. Cell Polarization equation

The QCA cell schematic consists of four quantum dots, as shown in Figure 2. The QCA cell contains two highly free electrons, and according to the positions of these electrons, it determines the cell polarization. The cell polarization is represented by Equation (6) [12, 21],

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \quad (6)$$

where ρ_1 to ρ_4 = charge density at each quantum dot of the cell and polarization represented by $P=+1$ for logic '1', $P=-1$ for logic '0', this provides a quantum level basis to logic gates.

1.7. Circuit Level Delay and Area Estimation

In QCA, performance metrics such as delay and area estimations are essential for designing and optimization purposes.

1.7.1. Delay Estimation

Delay estimation (D_{total}): In QCA circuits, delay refers to the time taken for the output to appear, and it is measured in cycles or clock phases [9] as shown in Equation (7),

$$D_{total} = N_{stages} \times T_{clock} \quad (7)$$

where, N_{stages} is the number of QCA clock zones (phases) and T_{clock} is the time per clock phase. Factors that influence delay in QCA circuits are clock phases, circuit complexity, wire length, clocking scheme, and layout.

1.7.2. Area Estimation

In QCA circuits, the area is related to the 2D rectangular space occupied by the circuit layout, and factors that influence area are cell count, cell size and spacing, wiring and routing, multi-layer structure, and layout optimization. Equation (8) represents the area estimation of QCA circuits [15]

$$A_{total} = N_{cells} \times A_{cell} \quad (8)$$

Here, N_{cells} is total number of QCA cells and A_{cell} represents the area occupied by one QCA cell.

1.7.3. Power Dissipation Model

In QCA circuits, power dissipation is mainly caused by tunneling-based switching energy that happens due to the movement of electrons between quantum dots, unlike in CMOS, caused by current-based power dissipations. The parameters that influence power dissipation in QCA circuits are clocking, switching energy, leakage, and thermal effects. In the upcoming years, we are reaching the end of Moore's law, and Landauer's principle is becoming crucial in post-CMOS technologies such as reversible computing or QCA. Landauer's principle is mainly considered as a theoretical guide to design and optimize energy-efficient QCA circuits. Equation (9) represents Landauer's principle [17].

$$E \geq kT \ln(2) \quad (9)$$

Here, K is the Boltzmann constant, and T is absolute temperature (Kelvin).

1.7.4. QCA Latency

QCA design uses 4-phase clocking zones (switch-Hold-Release-Relax). Clock delay or latency can be calculated as Equation (10) [21].

$$D = N_z \times T_{clock} \quad (10)$$

Here D is clock delay, N_z is the number of clocking zones/stages, and T_{clock} represents the duration of one clock phase. In this paper the measurement of latency in QCA Designer is based on the number of clock phases. Thus, a single clock zone corresponds to 0.25 of a full cycle. The proposed ALU relies on three consecutive clock zones to propagate its signal; thus: Latency = $3 \times 0.25 = 0.75$ cycles (i.e., three times the number of clock zones) is used for simulation.

1.7.5. Area Delay Product (ADP)

ADP is a crucial performance metric that evaluates the trade-off between speed and circuit size. The lower the value of ADP, the better the performance of the QCA circuit,

indicating a compact and fast design. ADP is shown in Equation (11) [21, 26],

$$ADP = A_{Layout} \times D \quad (11)$$

where A_{Layout} is the layout area, and D is the total clocking delay in ns. This equation represents the trade-off between the circuit size and speed. In QCA circuits, lower ADP is preferred. This section provides the different crucial performance metrics that can evaluate the performance of QCA circuits, and this paper analyzes these performance metrics to assess the performance of the proposed ALU circuits. Even though QCA technology offers significant theoretical advantages over CMOS technology in terms of area, delay, and power consumption. However, in the real world, the fabrication of QCA faces critical challenges, including nanoscale lithographic precision, thermal limitations, and underground clock wire routing.

The structure of this paper is organized as follows: Section 2 outlines reported ALU design and their comparison, Section 3 presents a proposed ALU design, Section 4 discusses the simulation results and comparative analysis, and lastly, Section 5 provides a conclusion and future directions.

2. REPORTED WORK

The design of the ALU is a crucial element in computational devices. An effective ALU design is essential for achieving high performance in computing systems. Therefore, it is crucial to implement the ALU using QCA nanotechnology, which offers several advantageous features. This paper begins by evaluating various ALU designs in QCA nanotechnology to analyze their performance. Then, this paper suggests an energy-efficient, high-performance, and single-layer ALU design in QCA nanotechnology. The objective of the proposed ALU is to optimize the utilization of QCA cells, thereby minimizing the design area requirements. Additionally, the paper includes a comparative analysis of the proposed ALU design to evaluate its performance.

This section discusses the outcomes and challenges of similar designs in QCA nanotechnology. As an emerging technology, relatively few researchers have focused on designing the ALU using QCA. This paper includes the significant existing works that outline the key observational parameters of the ALU during its design and implementation. The cell count and total area requirement are key parameters to make the design area-efficient. The ALU circuit's operation speed is measured using applied clocking schemes. The minimum application of the clocking scheme shows a fast operating circuit. Energy efficiency is checked after calculating the energy dissipation values and deriving the power dissipation maps. Various researchers have developed different types of schematic arrangements of the QCA cells, which form an ALU design. The outcomes of these works, along with the QCA layouts of the ALUs, are detailed in this section.

A 1-bit ALU has been developed in recent literature using QCA technology [30]. This design leverages the concepts of a multiplexer and a full adder. The ALU can execute eight mathematical operations and four logical operations, demonstrating its effectiveness and versatility in computational applications. The ALU is implemented using multiplexers and a full adder. The designed ALU consists of two 2:1 multiplexers, one 4:1 multiplexer, and one full adder circuit. The authors first proposed a multiplexer and a full adder in QCA nanotechnology. The multi-layer option was utilized to make it operational, where three different layers are employed. This ALU contains 248 cells, 2.25 delay, and $0.15 \mu\text{m}^2$ area.

Another ALU in QCA technology was designed using 1010 cells and a 4.25 clock delay [31]. It occupies a $1.86 \mu\text{m}^2$ area. The concept of this ALU is based on the five-input majority gate. The developed five-input majority gate is further used to design logic circuits like AND, XOR, XNOR, and multiplexers. The five-input majority gate is compared for the fault analysis. Logical crossovers are used to complete the ALU operation.

A multi-layer-based ALU was developed using QCA technology [32]. The idea of ALU depends on two 4:1 multiplexers, one 2:1 multiplexer, and one full adder circuit. A full adder is designed using a three-input XOR gate and a three-input majority gate. A 4:1 multiplexer is designed using three input majority gates. For the design of a multi-layer system, five layers were used. The ALU design contains 324 cells, 2.25 clock delay, and covers $0.245 \mu\text{m}^2$ area. There are no energy dissipation and power maps for the ALU circuit.

A fault-tolerant ALU was discussed in [33]. The implementation idea of ALU depends on the rotated majority gate (RMG). RMG uses a multi-layer concept; hence, the designed ALU is multi-layer in configuration. Three layers are utilized for the ALU design in QCA nanotechnology. Stuck-at, missing, and addition faults were calculated for the few input vectors in the ALU design. ALU design consists of 3 clock cycles and $0.78 \mu\text{m}^2$ area. This paper concentrates on the topic of fault-tolerant ALU design in QCA, with emphasis on area and delay rather than cell count. As in previous studies, especially those with multilayer QCA structures, the number of cells associated with every component is not a focal point because of the complexity of the design and the use of other simulation programs like QCA Designer that emphasize functional verification. The authors do not consider the ALU design for energy dissipation and power map analysis.

Different logic circuits like AND, OR, XOR, and an adder were applied to make an ALU [34]. ALU design is single-layer. ALU consists of 257 cells, 2 clock cycle delay, and an area of $0.29 \mu\text{m}^2$. ALU is designed using a 2:1 multiplexer, a 2-input XOR gate, and full adder circuits in QCA nanotechnology. A 1-bit ALU is further extended to a 2-bit ALU in QCA nanotechnology. The authors have not analysed the energy dissipation and power maps to check the effectiveness of energy saving.

A fault-tolerant three-input majority gate was developed in [35]. A full adder and a 2:1 multiplexer circuit are developed using the fault-tolerant three-input majority gate. The developed full adder and multiplexer circuits are used to design a 1-bit ALU in QCA nanotechnology. A single-layered ALU consisting of 625 cells and a 3.75 clock cycle delay was mentioned in [35]. ALU covers an area of $1.34 \mu\text{m}^2$. The mentioned ALU uses NOT, OR, AND, a full adder, and a 4:1 multiplexer circuit inside its configuration. The logical crossover was applied to pass the different logic states.

A single-bit ALU in QCA technology was demonstrated in [36]. The idea behind ALU is to consist of the majority of gates and inverter circuits. The fault analysis is presented for the inverter and the majority gates. The idea also uses a multi-layer design of the ALU. The temperature effects of the circuits are provided in the paper. There is a requirement of 13 majority gates and four inverters. XOR and multiplexer circuits are generated through the fundamental logic gates in the method. ALU contains 231 cells, 3 clock cycle delay, and an area of $0.28 \mu\text{m}^2$. The QCA Designer-E tool is utilized to check the functionality of the circuits. The power dissipation maps are not available in the research, so it isn't easy to analyze the cell-to-cell energy dissipation level. Table 2 summarizes the literature review.

From the available works on ALU design in QCA nanotechnology, it is confirmed that most of the authors have selected a multi-layer implementation of the ALUs to produce many functions. However, multi-layer implementation is not a feasible solution for logic circuits. The designs, which utilize a single-layer implementation of the QCA cells, generate limited functionalities. Therefore, this paper also suggests a single-layer ALU design, which is more efficient regarding QCA cells, area, and latency than the existing ALUs. So, the proposed work targets implementing a single-layer, energy-efficient, area-efficient, and ALU in QCA nanotechnology. Most existing designs present a separate implementation of the fundamental elements, which ultimately increases the cell count, design area, and the application of clock cycles. A single configuration of QCA cells is needed to deliver the overall functionality of the ALU. Most of the existing QCA ALU designs aim to reduce the number of cells, area, latency, and area delay product, while fault-tolerance evaluations such as cell omissions, cell displacements, and thermal noise analyses remain an open research issue.

Table 2. Summary of literature review.

Ref. No.	Cells	Delay (Clock Phases)	Area (μm^2)	Layers Used	Fault Analysis
[30]	248	2.25	0.15	3 (Multi-layer)	×
[31]	1010	4.25	1.86	×	Cell omission, extra deposition, displacement
[32]	324	2.25	0.245	5 (Multi-layer)	×

[33]	Not specified	3	0.78	3 (Multi-layer)	Stuck-at, missing, and addition faults
[34]	257	2	0.29	Single-layer	×
[35]	625	3.75	1.34	Single-layer	×
[36]	231	3	0.28	Multi-layer	For inverters and majority gates

3. METHODOLOGY AND PROPOSED ALU DESIGN

The proposed ALU design consists of several logical operations and arithmetic functionalities. For logical functions, the proposed ALU design can perform the AND, XOR, XNOR, buffer, and NOT operations, while for the arithmetic functions, the ALU design generates adder and comparator outputs. The QCA layout of the proposed ALU is given in Figure 7. The QCA-based ALU circuit is simulated using QCA Designer with the default values. To obtain an estimate of the layout area, the maximum horizontal and vertical dimensions of the proposed layout were measured in the QCA Designer workspace. Using this metric, the layout area was calculated as the product of the maximum horizontal cell count, maximum vertical cell counts and the area of a single QCA cell (18nm x 18nm). This calculation follows conventional methodologies found in the QCA literature [22,24].

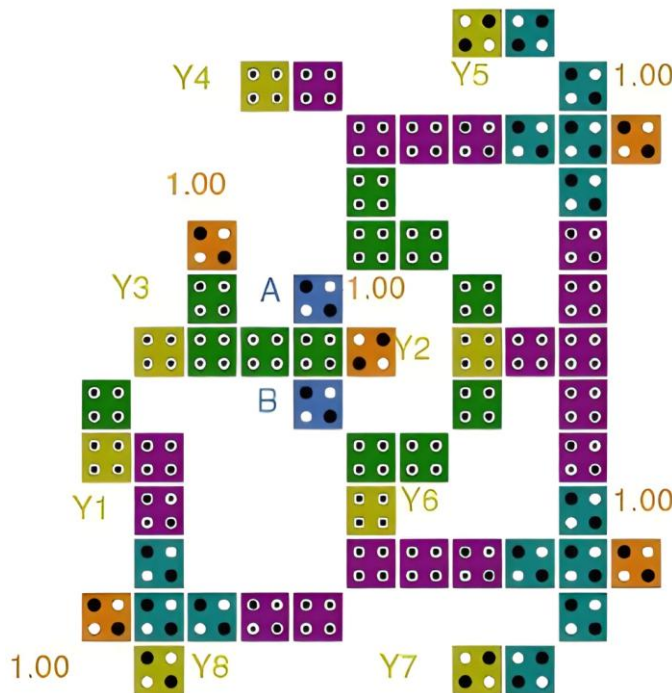


Figure 7. QCA layout of the ALU design

The proposed ALU design features a single layer without a crossing mechanism. It comprises the minimal number of cells required for the larger functions, necessitating only 57 QCA cells and three clocking phases to construct the ALU circuit. The design employs the fundamental principles of the majority gate for its implementation. Table 3 outlines the operations of the ALU design. To explicitly validate the

logic design, the truth tables are provided in Tables 5 and 6.

Table 3. The various operations of the ALU design

Operation	Circuit	Output
Arithmetic	Adder	Y1, (Sum), Y2(Carry)
	Comparator	Y3 (A=B), Y5 (A>B), Y7 (A<B)
Logical	AND	Y2
	OR	Y8
	NOT	Y6
	Propagation	Y4
	XOR	Y1
	XNOR	Y3

Table 3 shows that eight functions are generated for the ALU circuit. The output response of the ALU is provided in Figure 8 to check the input and output characteristics. The default settings of the bistable simulation engine within the QCA Designer tool are utilized for performance evaluation purposes. Table 4 represents the parameters used and energy dissipation.

Table 4. Parameters used and Energy dissipation.

Parameter	Description
Tool Used	QCA Designer-E
Simulation Engine	Coherence Vector
Energy Dissipation Mechanism	Occurs during polarization switching of QCA cells and environmental interaction
Total Energy Dissipation	2.58×10^{-2} eV
Average Energy Dissipation	2.35×10^{-3} eV per cycle
Energy Components	Input cell energy, output cell energy, and environmental energy

Table 5. Truth Table for XOR, AND, and XNOR Functions

A	B	Y1 (XOR/Sum)	Y2 (AND/Carry)	Y3 (XNOR/A=B)
0	0	0	0	1
0	1	1	0	0
1	0	1	0	0
1	1	0	1	1

Table 6. Truth Table for Buffer, Comparator, Inverter, and OR Functions

A	B	Y4 (Buffer A)	Y5 (A>B)	Y6 (NOT A)	Y7 (A<B)	Y8 (OR)
0	0	0	0	1	0	0
0	1	0	0	1	1	1
1	0	1	1	0	0	1
1	1	1	0	0	0	1

The energy dissipation is assessed to evaluate the energy-efficient operation of the proposed ALU circuit. The QCA Designer-E tool is employed for this purpose, utilizing the

coherence vector simulation engine. QCA cells dissipate energy during the transition of their polarization from one cell to another, and some energy is also lost to the environment during this process. Both total and average energy dissipation values are recorded. The total energy represents the aggregate of all energy components, including input cell energy, output cell energy, and environmental energy, among others. In the ALU depicted in Figure 7, the total energy dissipation measures $2.58\text{e-}002$ eV, while the average energy dissipation per cycle amounts to $2.35\text{e-}003$ eV for the ALU design.

4. SIMULATION RESULTS AND COMPARATIVE ANALYSIS

This paper employs a comparative analysis to identify the optimal QCA layouts designed for the ALU circuit. It examines various ALU circuit designs within QCA nanotechnology, with key features discussed in Section 2. A thorough comparative evaluation is essential to determine the most appropriate ALU design found in the existing literature across different criteria. Consequently, this section presents the comparative analysis and results of the diverse ALU designs. The comparison is based on the generalized key parameters like the number of QCA cells, clocking phase requirement, QCA cell area, QCA layout area, crossing requirement, nature of layer, number of function generations, and area delay product. The existing works are compared based on the available data in the published papers. Table 7 provides the comparative results of the ALU designs in QCA nanotechnology.

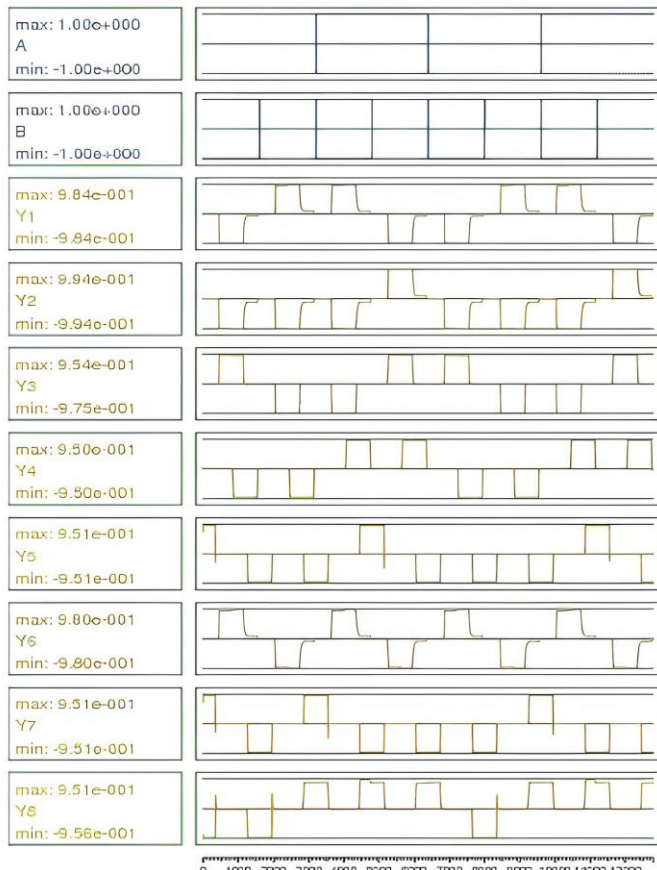


Figure 8. Output characteristics of the proposed ALU circuit

From Table 7, it can be seen that the proposed ALU provides better results than the existing ALU designs. The existing designs use a crossing mechanism to pass the signals, while the proposed ALU is free from any crossings by implementing an effective logic configuration. The proposed ALU consists of only 57 QCA cells and very few clocking phases that enhance the cell area, layout area, and area delay product. There is no requirement for a multilayer structure for the proposed ALU, so it made the physical implementation relatively simple.

Table 7 shows the QCA cells' requirements for building an ALU design. The effective selection of the logic formation causes a minimum cell requirement in the ALU design. The applied clocking system enables the estimation of speed in QCA circuits. A smaller number of clocking phases reflects a fast-operated circuit in QCA nanotechnology. A minimum cell in a circuit requires fewer clocking phases, producing a slight circuit delay. The QCA cells, utilized in the circuits, are assumed to be $18\text{ nm} \times 18\text{ nm}$ in size. Hence, the cell area is the multiplication of a cell size by the number of cells, utilized to meet the QCA design. The layout area is based on the area occupied by the QCA circuit on a real-time basis. It depends on the logic structure and the nature of horizontal and vertical connections of the cells in a QCA circuit.

The complexity of the design is reduced by avoiding the crossings of the wires in the proposed ALU. Many existing works employed a multilayer structure for the ALU designs. The multilayer structure faces the physical design implementation challenge. A single-layer structure provides easy access to the functions. The proposed ALU design is a single layer and overcomes the hurdles of multilayer design implementation. The figure of merit for the ALU design is measured in terms of the area delay product. The lower value of the area delay product is deemed more effective in terms of design utilization. The area delay product for the proposed ALU is minimal compared to the existing design. So, the figure of merit for the proposed ALU is improved.

The number of functions in an ALU causes the control of QCA cells. More QCA cells may be required to generate the targeted function and increase the functionality of the ALU. The design needs many QCA cells in a QCA layout if it is a single layer. However, a precise logic idea can be utilized to minimize the need for many QCA cells. This can be easily seen from Table 7, where the researchers implement different ideas to control the QCA cells and clocking phases. QCA cells and clocking phases in a QCA circuit are essential in observing the effectiveness of the logic circuits. A minimum QCA cell depicts an area-efficient design, while a minimum clocking phase requirement shows a fast logic circuit. Therefore, a competitive diagram for the QCA cells and clocking phases of the various ALU designs is needed to deliver effective output to the researchers. Hence, the graphical representation of the QCA cells and clocking phases is provided in Figure 9 for the different ALU designs for better comparative analysis. To calculate the improvement, in percentage terms, between an existing system and a system that has been proposed, the following Equation (12) is used:

$$\text{Improvement (\%)} = \left(\frac{\text{Benchmark Value} - \text{Proposed Value}}{\text{Benchmark Value}} \right) \times 100 \% \quad (12)$$

whereas the Proposed Value represents the metric obtained for the proposed ALU.

In Equation 12, the Benchmark Value represents the respective metric according to the reference design,

Table 7. Comparative results for various parameters of different ALU designs

ALU	QCA cells	Clocking phase	Cell area (μm^2)	Layout area (μm^2)	Crossing	Layer	# Function	Area delay product
[30]	248	2.25	0.080	0.15	yes	multi	12	0.3375
[31]	1010	4.25	0.327	1.86	yes	single	4	7.905
[32]	324	2.25	0.105	0.245	yes	multi	11	0.5513
[33]	NA	3.00	NA	0.78	yes	multi	4	2.34
[34]	257	2.00	0.083	0.29	yes	single	4	0.58
[35]	625	3.75	0.203	1.34	yes	single	4	5.025
[36]	231	3.00	0.075	0.28	yes	multi	4	0.84
Proposed	57	0.75	0.018	0.046	No	single	8	0.0345

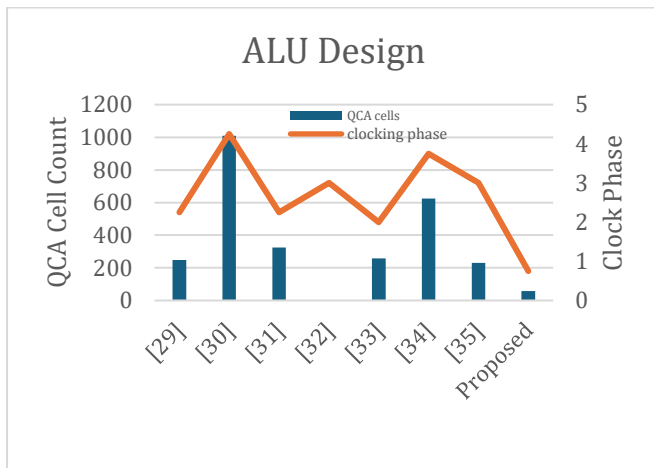


Figure 9. Graphical comparison of QCA cell count and clocking phases derived from Table 7.

The various operations of the presented ALUs are mentioned in Table 3. It helps identify the more valuable QCA-based ALU design in terms of functionality. The nature of functions is highlighted, and the key functions of the designed ALUs are provided. Few ALUs have generated additional type combinations, but these are counted as adders only because the basic function is addition. Therefore, the actual operations are mentioned in Table 8.

Table 8. Comparative analysis of the key functions generated by various ALUs

ALU	Function
[30]	XOR, AND, OR, NOT, Adder, Increment, Decrement, Propagation, Difference
[31]	XOR, XNOR, AND, Adder
[32]	XOR, NOT, Propagation, Increment, Decrement, Adder, Difference
[33]	AND, OR, XOR, Adder

[34]	AND, OR, XOR, Adder
[35]	AND, OR, NOT, Adder
[36]	AND, XOR, Adder
Proposed	Adder, Comparator, AND, OR, NOT, Propagation, XOR, XNOR

Table 8 presents adder as a common operation, a key element in the ALU system, and all the ALU designs implemented it. From Table 7, the functions of the ALU designed in [30] are high, and it can implement 12 functions. The proposed ALU has a minimum area delay product and is capable of executing a total of eight functions. The design in [30] also requires a multi-layer crossover. In summary, the QCA-based ALU architecture proposed here is a highly efficient, single-layer, with no wire crossings, and therefore very little complexity and implementation difficulties; by using just 57 QCA cells, the design has a large reduction of area ($0.046 \mu\text{m}^2$), with a very low (0.75 clocking phases) cost to producing 8 logic/adaptive functions (AND, OR, XOR, XNOR, NOT, propagation, adder, and comparator).

5. CONCLUSION

As the technology node is scaled down in the nanoscale regime, conventional MOSFET devices face the challenge of short-channel effects. The SCE limits the scalability and performance of the devices. Current MOSFET technology is being utilized to further optimize dimensions for area efficiency. To design effective digital circuits, it is essential to explore alternative device technologies. Among these, QCA technology is a trending computational method that benefits area-efficient, fast, and low-power logic implementation. It provides many advantages for digital circuit design compared to the MOSFET technology. The logic formation in QCA nanotechnology is based on the position of electrons in a QCA cell. ALU plays a critical role in computing architectures, making the design of efficient

QCA-based ALUs vital for practical nanocomputing applications. Therefore, this paper proposed a novel ALU design to mitigate QCA cell count and clock delay. It also comprehensively analyzes the various existing ALUs with proposed designs. The proposed ALU is more efficient regarding QCA cells, clock delay, nature of layer, area delay product, layout area, cell area, and crossing mechanism requirement. All the existing ALUs are using the crossing mechanism to pass the QCA wires, which shows the complexity of the designs. Due to large QCA cells and the nature of logic formation in the existing ALUs, the area delay product gets degraded. The area delay product of the proposed design is improved by 89.78% compared to the best existing design. Despite these advancements, opportunities for further research remain. Key areas for future work include developing fault-tolerant and noise-reducing QCA logic to enhance circuit reliability amid manufacturing imperfections. Additionally, exploring hybrid QCA with other nanotechnologies, like molecular or spintronic logic, is also a crucial direction for research.

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