

A novel analytical current model for hexagonal shaped double gate JLFET

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ABSTRACT

A fully analytical mathematical model for drain current for the junctionless field effect transistor (JLFET) with a hexagon-shaped body has been developed and reported in this work. The model is designed to be valid in the four modes of operation- Subthreshold, bulk current, flat band, and accumulation modes. The model is based on channel resistance. Resistance for each of the three-layer types—neutral, depletion, and accumulation layers is determined first, and then the equivalent channel resistance. The subthreshold region comprises only the depletion layer, while in the bulk current mode, the overall resistance will be the parallel combination of the neutral layer and depletion layer resistances. In accumulation mode, the total resistance is derived by combining the accumulation and neutral resistances in parallel, whereas in flat band mode, only the neutral layer is present. After calculating the body's equivalent resistance, the potential model and Ohm's law were used to generate the drain current expression. The model is appropriate for compact modeling and has a completely analytical nature. The analytical drain current model is validated with technology computer-aided design (TCAD) numerical simulator and experimental results by comparing the device's output and transfer characteristics acquired from the mathematical expressions with those computed by TCAD simulations and experimental results. The model seems to agree well with the results obtained from both TCAD simulations and experiments.

Keywords: Drain current, Subthreshold swing, Double gate, Hexagonal, JLFET

1. INTRODUCTION

Contemporary markets are primarily led by solid-state devices, particularly Metal Oxide Semiconductor (MOS) types, due to their superior controllability, minimal switching losses, and capacity for extreme miniaturization. Yet, in the very large scale integration (VLSI) era, the fundamental MOS configuration has become obsolete, and rapidly scaling down MOS field effect transistor (FET) presents significant challenges. In addition, MOSFETs are always getting smaller to improve performance, which leads to the development of short channel effect (SCE) techniques such as scattering of surface, modulation of channel length, and drain-induced barrier lowering (DIBL). SCE multigate MOSFETs were proposed to reduce all of the above; despite having many important advantages, it also has some significant switching limitations [1]. While showing strong gate control, near-ideal subthreshold slope, with minimal short-channel effects, and simple fabrication, the Junctionless Nanowire Transistor (JNT) is one of the most promising approaches for the realization of the integrated circuits of the near-future due to its superior electrical properties [2,3]. Various impacts of doping concentration levels (from $10^{10}/\text{cm}^3$ up to $10^{19}/\text{cm}^3$) on electrical figure-of-merits of a double gate (DG) JLFET, like the I-V characteristic parameters such as threshold voltage, on current, $I_{\text{on}}/I_{\text{off}}$, and subthreshold swing (SS), have been studied [4]. This device maintains a consistent doping level across the source, channel, and drain sections when there are no junctions. Junctionless Transistor (JLT) is easily fabricated and extremely scalable. The most critical

parameter of every MOS-based device is the current through it, and JLFET's turn-off state is a major limitation. So, for JLFET to effectively suppress the off-state current, it needs a small channel and a high work function gate. Due to its many advantages over traditional MOSFETs, such as its superior $I_{\text{on}}/I_{\text{off}}$ ratio, quick switching time, low power consumption, and exceptional gate controllability over channel potential, JLFETs are becoming more and more popular in the VLSI design field.

Due to the heavy doping of the substrate, the JLFET's device turn-on current is extremely high. In a JLFET, changing the gate voltage changes the depletion width, which changes the channel resistance. To determine the drain current, a channel resistance-based methodology is incorporated where channel resistance and channel potential models have been used. For long-channel DGJLFETs, the model for drain current was discussed by Duarte et al. in [5]. It is suitable for compact modelling since it consistently captures the bulk conduction mechanism phenomenon in all device operation regions, such as the saturation, linear, and subthreshold regions. Similarly, the drain current model for symmetric DGJLFET was discussed by Sarma et al. in [6], where each segment's equivalent resistance and potential difference are calculated, and current through each segment is then computed using Ohm's law. Also, a drain current model for triple-gate JLT was discussed in [7] by Trevisoli et al. For devices having a long channel, the effective surface potential is first determined using the 2-D Poisson equation. The novel contribution of the paper is higher on current compared to the conventional structure,

thereby giving better electrical characteristics compared to conventional DGJLFET. Moreover, it has a simplified manufacturing procedure with improved scalability and a lower leakage current.

2. LITERATURE REVIEW

Gola et al. in [8] introduced a drain current model for tri-gate JLT to investigate the influence of substrate bias voltage on the static surface potential, charge density, and drain current of the device. An excellent agreement between the drain current for triple gate JNT (3G JLNT) and its findings with different doping concentration and channel width values is shown by Paz et al. in [9]. Additionally, threshold voltage, V_{th} , subthreshold slope (SS), and DIBL calculations are performed. For short-channel symmetric JLFETs, the potential and drain current model was introduced by Baruah et al. [10]. The potential is determined using 2-D Poisson's equation, and this model is applicable in all operational zones, i.e., depletion to accumulation. Additionally, the V_{th} and DIBL values are taken from the potential model. The JLFET uses the depletion width, which comes from the different work functions of the body and gate, as explained in [11]. An internal electric field created by the work function difference between the semiconductor and gate layers forms the depletion range, as discussed in [12], which determines the depth and generation of the JLFET's operation.

The use of a double gate material in a JLFET was proposed in [13]. It acts as if the electric field given by the gate is less or more than that in the gate. In [14], the four operating regimes of JLFET are discussed, which are based on the mechanism of current conduction: accumulation, bulk current, flat band, and subthreshold. The depletion width and threshold voltage, V_{th} , of the parallel double gate JLFET are explained in [15]. When the gate voltage drops below V_{th} , the carriers in the channel get depleted, causing a high resistance in the channel. Additionally, the channel resistance and the drain current in a JLFET are directly connected to the thickness of the depletion region.

The work in [16] discusses the unified analytical model for the drain current of a symmetric DGJLFET. The work in this paper mainly focuses on the accumulation mode. Additionally, reference [17] demonstrates that placing an insulator within the channel substantially lowers the I_{off} . Nevertheless, this method might also lower the ON current. Employing high-K spacers offers an alternative to this limitation, improving analog device performance by leveraging the fringing-field effect to significantly reduce off-state leakage current [18]. For JLT to work, the device's body area needs to be completely discharged for total shutdown. In this instance, the depletion layer will be maintained as long as the substrate's and gate material's work functions diverge sufficiently to produce an electric field that maintains the device in a fully depleted state, as discussed in [19]. If requirements are not met, then turning off the device is not possible. Bora et al. in [20] have developed an analytical model to describe the surface potential and drain current of an ultra-short channel Double Gate Asymmetric JLT (DG AJLT). After obtaining the

potential, electrical properties such as drain current were extracted, which are applicable in all areas of operation. The introduction of another method for controlling leakage current by utilizing high-k gate dielectrics is analyzed in [21-22]. N. Bora in [23] examines how quantum confinement influences the surface potential, threshold voltage, drain current, transconductance, and drain conductance of dual material (DM) DGJNT. Because the channel thickness falls under 10 nm due to quantum mechanical effect (QME), the V_{th} shift serves as a quantum correction term for JLFET compact modeling. Gnudi et al. in [25] discuss the channel potential model, threshold roll-off, DIBL, and inverse subthreshold slope for symmetric DG JLFET, thereby simplifying the current, making the circuit model easy for simulation. S. Kumar et al. in [26] discuss the Recessed Double Gate JLFET, where, in comparison to Conventional DG JLFET, the device exhibits lower I_{off} , improved I_{on}/I_{off} , better SS, and lower DIBL. In [27], A. Kumari et al. discuss the drain current model for gate all around (GAA) MOSFET. The methodology incorporates the S/D series resistance (RSD), which decreases the drain current effect due to the reduction in terminal voltages. A Baro in [28] discusses Symmetric DGJLFET with a triangle-shaped spacer, and the drain current is obtained.

3. DESIGN OVERVIEW

The hexagonal-shaped junctionless field-effect transistor (HDG JLFET) is a proposed structure where drain current (I_d) and overall device performance are enhanced through geometry engineering. This new design for a hexagonal DG JLFET with a triangular S-D region is suggested in order to improve performance characteristics over the traditional DG JLFET structures. Due to this hexagon-shaped structure, the cross-section channel offers an increased ratio of surface area to volume, improved gate management throughout the channel, and a more consistent electric field by making the channel wider.

3.1. Proposed Work

In [26], the electrical characteristics of the proposed JLFET with a hexagonal shape is demonstrated. Therefore, by depleting the channel under the gate, the HDG JLFET can be turned off. The device is off when a complete depletion layer forms at the channel region, preventing current from flowing through it. Applying a gate voltage, V_{gs} , reduces the depletion layer and weakens the internal electric field, thereby making the channel conductive. When in this mode, the device is powered on. Current begins to flow, and the depletion region narrows when the applied gate voltage reaches the device's threshold. The work function (w.f) of the gate material determines its on-off operation. If the gate's w.f is greater than the channel's, an N-channel JLFET generates a depletion area that can stretch across the channel's thickness if the channel is thin. When voltage is applied above the threshold, the device goes from standby to activated because the resulting electric field is unable to keep the channel completely depleted. If the V_{gs} is gradually raised, the device will eventually experience a massive surge in current, and when the electric field is zero, this particular point is known as the flat band voltage. The applied gate voltage causes charges to accumulate at the

surface above this point. The new hexagonal-based double-gate junctionless FET (HDG JLFET) design consists of a semiconductor substrate with a practically uniform doping profile in the source, drain, and channel, high-k gate dielectric over the channel, and a high work function metal gate structure over the gate dielectric. This hexagonal arrangement maximizes the effective channel length close to the middle and decreases it near the gate since the channel length is longer. The DIBL is controlled in the Off-state near the gate, but because the channel length is longer near the center, the DIBL is already lower, leading to a stronger ON current and a maintained OFF current, which increases the I_{on}/I_{off} ratio.

The device's enhanced performance is largely attributed to the high-k gate dielectric, which improves gate control and minimizes leakage current. The model encompasses every operational mode of the device. This work presents an analytical model for the drain current, which is determined using the channel resistance and channel potential model. Results from TCAD simulations are used to verify the model at the simulation level.

3.2. Contribution

The main contributions in this work include a novel hexagonal double-gate JLFET structure with a triangular source-drain (S-D) structure is presented. This results in higher drain current in the ON-state. The hexagon's multiple faces enable the gate to regulate the channel from several directions. Lessens leakage and improves channel formation, leading to increased transconductance (g_m). The hexagonal shape mitigates DIBL and threshold voltage roll-off while enhancing the I_{on}/I_{off} ratio. In this hexagonal-shaped JLFET, the ON-state drain current increases because the effective channel width is bigger, which gives better control of the gate, making the current more efficient and lessening SCEs. Hexagonal geometry greatly enhances drain current performance while preserving little leakage, rendering it appropriate for next-generation nanoscale devices.

4. MATHEMATICAL MODELLING

In order to establish the drain current, the study employs the channel's resistance. The method used to compute the resistance is based on the charge density in the different sections of the channel since the channel is composed of neutral semiconductors that can accumulate, deplete, or combine in different modes of operation.

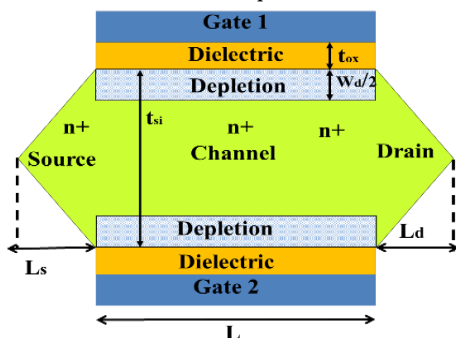


Figure 1. 2-D view of Hexagonal Double gate JLFET [24]

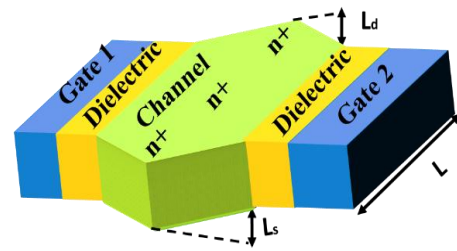


Figure 2. 3-D schematic view of Hexagonal Double gate JLFET

A cross-sectional view of a hexagon-shaped double-gate JLFET is displayed in Figures 1 and 2. Drain, source, and channel are the three sections that make up the device's body, where L represents gate length, and L_s and L_d denote source and drain length, respectively. After determining the resistances of each region independently, the equivalent resistance of the entire body is finally found. The four different modes of operation of JLFET are as-

- Subthreshold mode ($V_{gs} \leq V_{th}$)
- Bulk current mode ($V_{fb} \leq V_{gs} \leq V_{th}$)
- Flat band mode ($V_{gs} = V_{fb}$)
- Accumulation mode ($V_{gs} \geq V_{fb}$)

where V_{gs} , V_{ds} , V_{th} , and V_{fb} stand for gate-to-source voltage, drain-to-source voltage, threshold voltage, and flat-band voltage, respectively.

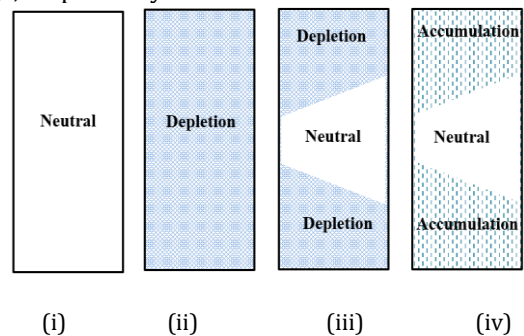


Figure 3. Different modes of operation of DGJLFET in (i) Flat band (ii) Subthreshold (iii) Bulk current and (iv) Accumulation

Figures 3(i), (ii), (iii), and (iv) depict the device's resistance equivalent circuits for various modes of operation. The device operates in four modes—cutoff, bulk current, flatband, and accumulation—each represented by distinct resistance equivalent circuits. When operating in cutoff mode, a substantial work function disparity generates a strong internal electric field that completely depletes the channel, leading to high resistance and zero current. When the gate voltage exceeds the threshold, partial depletion enables current flow in bulk current mode. Raising the gate voltage further neutralizes the channel in flat band mode, significantly lowering resistance and allowing high current to flow. At even higher gate voltages, accumulation mode occurs, where additional charge carriers near the surface boost the drain current.

Each area comprises of-

- Depletion resistance $R_d(x, y, V_{gs}, V_{ds})$
- Flat band resistance $R_{nd}(x, y, V_{gs}, V_{ds})$
- Combination of both neutral semiconductor region and depletion region (Bulk mode)
- A combination of neutral semiconductor and accumulation resistance (Accumulation mode)

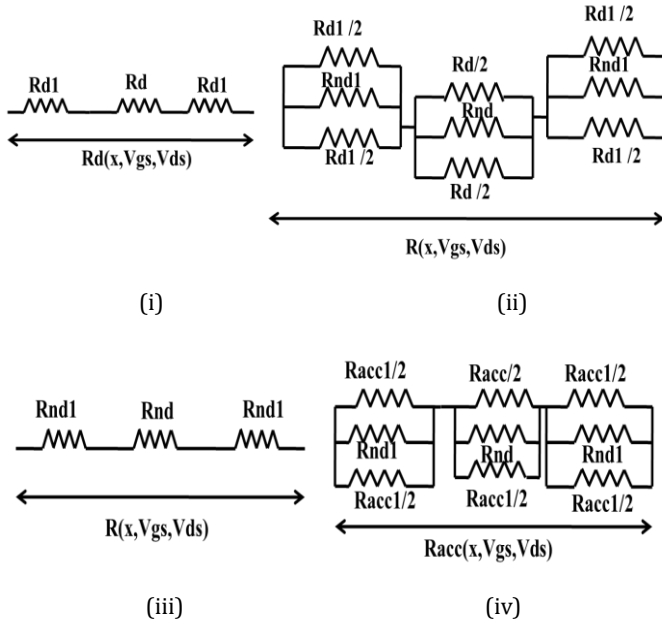


Figure 4. (i) Subthreshold mode (ii) Bulk current mode (iii) Flat band mode (iv) Accumulation mode

In the subthreshold mode, only the depletion layer is present, as seen in Figure 4(i). Therefore, the equivalent resistance of the channel in the subthreshold mode is given as Equation (1),

$$R_{eq} = 2R_{d1} + R_d \quad (1)$$

where R_{d1} , R_{nd1} and R_{acc1} represents S-D region depletion resistance, flat band resistance and accumulation resistance, respectively. On considering the depleted region where the variation of resistances are expressed as Equation (2) [6],

$$R_d = \frac{1}{q\mu p} \frac{\Delta L}{WW_d} \quad (2)$$

where the depletion width of n-channel DG JLFET's, W_d can be expressed using Equation (3) [15],

$$W_d = t_{si} - \sqrt{\frac{4qN_d t_{si} \epsilon_{si} t_{ox} + t_{si}^2 \epsilon_{ox} qN_d - 8 \epsilon_{si} \epsilon_{ox} (\phi_0 - \phi_{gs})}{qN_d \epsilon_{ox}}} \quad (3)$$

Therefore, resistance of the depleted regions can be obtained as Equations (4) and (5),

$$R_d = \frac{1}{q\mu p} \frac{\Delta L}{W \left(t_{si} - \sqrt{\frac{4qN_d t_{si} \epsilon_{si} t_{ox} + t_{si}^2 \epsilon_{ox} qN_d - 8 \epsilon_{si} \epsilon_{ox} (\phi_0 - \phi_{gs})}{qN_d \epsilon_{ox}}} \right)} \quad (4)$$

$$R_{d1} = \frac{1}{q\mu p} \frac{\Delta L}{W \left(t_{sieff} - \sqrt{\frac{4qN_d t_{sieff} \epsilon_{si} t_{ox} + t_{sieff}^2 \epsilon_{ox} qN_d - 8 \epsilon_{si} \epsilon_{ox} (\phi_0 - \phi_{gs})}{qN_d \epsilon_{ox}}} \right)} \quad (5)$$

where, W indicates device width, ϵ_{ox} , and t_{ox} indicates permittivity and thickness of gate dielectric, respectively, ΔL is the single segment length, mobility is denoted by μ , charge carrier concentration by n , and single electron charge by q , t_{si} represents channel thickness, ϵ_{si} and t_{sieff} denotes permittivity and effective channel thickness, respectively and N_d is donor doping concentration. The depleted region's carrier density is provided as Equation (6) [6]

$$P = \frac{n_i^2}{\sqrt{\left(n_i^2 + \frac{N_d^2}{4} \right)} + \frac{N_d}{2}} \quad (6)$$

where, intrinsic carrier concentration is denoted by n_i , the effective channel thickness, t_{sieff} can be obtained in following way Equations (7) and (8),

$$\tan \theta(x) = \frac{t_{si}}{L_s} \quad (7)$$

$$\text{As } \frac{t_{sieff}}{x} = \frac{t_{si}}{L_s} \quad (8)$$

then

$$t_{sieff} = \frac{x t_{si}}{L_s} \quad \text{for } x = -L_s \text{ to } 0 \text{ and}$$

$$t_{sieff} = \frac{x t_{si}}{L_d} \quad \text{for } x = 0 \text{ to } L_d$$

The bulk current mode's body is a neutral semiconductor layer with depletion layers on either side, as seen in Figure. 4(ii). Consequently, in this mode, the channel's resistance will be Equation (9).

$$R_{eq} = R_1 + R_2 + R_3 \quad (9)$$

$$\text{where, } R_1 = \frac{R_{d1}}{2} \left| R_{nd1} \right| \frac{R_{d1}}{2} = \frac{R_{d1}}{4} \left| R_{nd1} \right|, R_2 = \frac{R_d}{4} \left| R_{nd} \right|$$

$$R_3 = \frac{R_{d1}}{4} \left| R_{nd1} \right|$$

For each segment, the resistance of the non-depleted area is provided as Equations (10), (11) and (12)[6],

$$R_{nd} = \frac{1}{qn\mu} \left(\frac{\Delta L}{W(t_{si} - W_d)} \right) \quad (10)$$

$$R_{nd} = \frac{1}{q\mu n} \left(\frac{\Delta L}{W \sqrt{\frac{4qN_d \epsilon_{si} t_{ox} t_{si} + t_{si}^2 \epsilon_{ox} qN_d - 8 \epsilon_{si} \epsilon_{ox} (\phi_0 - \phi_{gs})}{qN_d \epsilon_{ox}}}} \right) \quad (11)$$

$$R_{nd1} = \frac{1}{q\mu n} \left(\frac{\Delta L}{W \sqrt{\frac{4qN_d \epsilon_{si} t_{ox} t_{sieff} + t_{sieff}^2 \epsilon_{ox} qN_d - 8 \epsilon_{si} \epsilon_{ox} (\phi_0 - \phi_{gs})}{qN_d \epsilon_{ox}}}} \right) \quad (12)$$

The non-depleted region's carrier density is provided as Equation (13) [6],

$$n = \sqrt{\left(n_i^2 + \frac{N_d^2}{4} \right)} + \frac{N_d}{2} \quad (13)$$

The channel or entire body is a neutral semiconductor in the flatband mode. Thus, the channel resistance can be expressed as Equation (14),

$$R_{eq} = 2R_{nd1} + R_{nd} \quad (14)$$

In the accumulation mode, the channel is composed of two accumulation layers on top and bottom of a neutral semiconductor layer in the middle. Consequently, the channel's resistance in this mode is determined similar to Equation (9) but here,

$$R_1 = \frac{R_{acc1}}{2} || R_{nd1} || \frac{R_{acc1}}{2} = \frac{R_{acc1}}{4} || R_{nd1} ||, \quad R_2 = \frac{R_{acc}}{4} || R_{nd}$$

$$R_3 = \frac{R_{acc1}}{4} || R_{nd1}$$

Let us consider the value of resistances of the channel and S-D region in the accumulation mode given as Equations (15) and (16),

$$R_{acc} = \left(\frac{L}{WW_{acc}} \rho_{acc} \right) \quad (15)$$

$$R_{acc1} = \left(\frac{L_{seff}}{WW_{acc1}} \rho_{acc1} \right) \quad (16)$$

where charge in the accumulation mode is given by Equations (17) and (18) [29],

$$Q_{acc} = \epsilon_{si} \frac{\sqrt{2}}{L} \frac{kT}{q} \sqrt{\exp\left(-\frac{q\phi_{Sch}(x)}{2kT}\right) - 1} \quad (17)$$

$$Q_{acc1} = \epsilon_{si} \frac{\sqrt{2}}{L} \frac{kT}{q} \sqrt{\exp\left(-\frac{q\phi_{Ssd}(x)}{2kT}\right) - 1} \quad (18)$$

The resistivity of accumulation mode can be given as Equation (19) and (20),

$$\rho_{acc} = \frac{1}{\mu_{eff} Q_{acc}} \quad (19)$$

$$\rho_{acc1} = \frac{1}{\mu_{eff} Q_{acc1}} \quad (20)$$

When the velocity saturation effect is taken into account, effective mobility can be expressed as Equation (21) [28],

$$\mu_{eff} = \frac{\mu}{\left[1 + \left(\frac{\mu V_{ds,eff}}{v_{sat} L} \right)^\beta \right]^{\frac{1}{\beta}}} \quad (21)$$

Where L is the gate length, $V_{ds,eff}$ and v_{sat} denotes the effective drain-to-source voltage and carrier's saturation velocity, respectively. The thickness of accumulation layer can be given as Equations (22) and (23) using Debye length, where L_D as Equation (24) [28],

$$W_{acc} = \sqrt{2} L_d \left[\frac{t_{si}}{2\sqrt{2} L_d} + \cos^{-1} \left\{ \exp\left(\frac{q\phi_{Sch}(x)}{2kT}\right) \right\} \right] \quad (22)$$

$$W_{acc1} = \sqrt{2} L_d \left[\frac{t_{sieff}}{2\sqrt{2} L_d} + \cos^{-1} \left\{ \exp\left(\frac{q\phi_{Ssd}(x)}{2kT}\right) \right\} \right] \quad (23)$$

$$\text{Where, } L_D = \sqrt{\frac{\epsilon_{si} kT}{q^2 N_d}} \quad (24)$$

where T is temperature k is Boltzman's constant, and $\phi_s(x)$ is the surface potential which can be obtained as follows. The electrostatic channel potential expression for DGJLFET is obtained as Equation (25) [29],

$$\phi(x, y) = \phi_0(x) + \frac{\epsilon_{ox}}{t_{sieff} \epsilon_{si} t_{ox}} (\phi_{gs} - \phi_s) y^2 \quad (25)$$

At $y = t_{sieff}/2$

$$\phi(x, y) = \phi_s(x) = \phi_0(x) + \frac{t_{sieff} \epsilon_{ox}}{4 \epsilon_{si} t_{ox}} (\phi_{gs} - \phi_s(x)) \quad (26)$$

On substituting Equations (26) in (25) we get Equation (27),

$$\phi(x, y) = \phi_s \left(1 + \frac{t_{sieff} \epsilon_{ox}}{4 \epsilon_{si} t_{ox}} \right) - \frac{t_{sieff} \epsilon_{ox}}{4 \epsilon_{si} t_{ox}} \phi_{gs} + \frac{\epsilon_{ox}}{t_{si} \epsilon_{si} t_{ox}} (\phi_{gs} - \phi_s(x)) y^2 \quad (27)$$

Inserting $\phi(x, y)$ in Poisson's equation and considering, $y = t_{si}/2$ forms Equation (28),

$$\frac{d^2 \phi_s(x)}{(1\phi)^2} + \frac{1}{\lambda^2} \{ \phi_{gs} - \phi_s(x) \} = - \frac{qN_d}{\epsilon_{si}} \quad (28)$$

Solving Equation (28), the surface potential in the channel and source-drain region can be obtained as Equations (29) and (32), respectively, where,

$$\frac{L_s}{t_{si}} \left(\frac{t_{si}}{2} - y \right) = L_{seff} \quad \text{for } 0 \text{ to } -t_{si}/2,$$

$$\frac{L_s}{t_{si}} \left(\frac{t_{si}}{2} + y \right) = L_{seff} \quad \text{for } 0 \text{ to } t_{si}/2,$$

As $L_{seff} = L_{deff}$ consequently equations of L_{deff} is analogous to L_{seff} , therefore,

$$\phi_{Sch}(x) = \frac{\left[(V_{ds} + C\lambda^2) e^{\frac{L+L_{deff}}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_{deff}}{\lambda}}} \right] e^{\frac{x}{\lambda}}}{\left(e^{\frac{2(L+L_{deff})}{\lambda}} - e^{-\frac{2L_{deff}}{\lambda}} \right)} - \left[\frac{\left\{ (V_{ds} + C\lambda^2) e^{\frac{L+L_{deff}}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_{deff}}{\lambda}}} \right\} e^{-\frac{2L_{deff}}{\lambda}} - \left\{ C\lambda^2 (e^{\frac{2(L+L_{deff})}{\lambda}} - e^{-\frac{2L_{deff}}{\lambda}}) e^{\frac{L_{deff}}{\lambda}} \right\}}{e^{\frac{2(L+L_{deff})}{\lambda}} - e^{-\frac{2L_{deff}}{\lambda}}} \right] e^{-\frac{x}{\lambda}} - C\lambda^2 \quad (29)$$

$$\text{Where } \lambda = \sqrt{\frac{t_{si} \epsilon_{si} t_{ox}}{2 \epsilon_{ox}}} \quad (30)$$

$$\lambda_1 = \sqrt{\frac{t_{sieff} \epsilon_{si} t_{ox}}{2 \epsilon_{ox}}} \quad (31)$$

$$\begin{aligned}
 \phi_{ssd}(x) = & -\frac{qN_d}{2\epsilon_{si}}x^2 + \\
 & \left[\frac{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_{deff}}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_{seff}}{\lambda_1}}}}{(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}})} \left(e^{\frac{L}{\lambda_1}} - 1 \right) - \frac{\left\{ (V_{ds} + C\lambda_1^2)e^{\frac{L+L_{deff}}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_{seff}}{\lambda_1}}} \right\} e^{-\frac{L_{seff}}{\lambda_1}} - C\lambda_1^2 \left(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}} \right) e^{\frac{L_{seff}}{\lambda_1}}}{(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}})} \left(e^{\frac{L}{\lambda_1}} - 1 \right) + \frac{qN_d}{2\epsilon_{si}}L^2} \right] \frac{x}{L} \\
 & + \left[\frac{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_{deff}}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_{seff}}{\lambda_1}}}}{(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}})} \right] - \left[\frac{\left\{ (V_{ds} + C\lambda_1^2)e^{\frac{L+L_{deff}}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_{seff}}{\lambda_1}}} \right\} e^{-\frac{L_{seff}}{\lambda_1}} - C\lambda_1^2 \left(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}} \right) e^{\frac{L_{seff}}{\lambda_1}}}{(e^{\frac{L+L_{deff}}{\lambda_1}} - e^{-\frac{L_{seff}}{\lambda_1}})} \right] - C\lambda_1^2 \quad (32)
 \end{aligned}$$

Considering quantum confinement effect, ϕ_{gs} is replaced with ϕ_{gs}' as Equation (33),

$$\phi_{gs}' = \phi_{gs} - \Delta V_{th} \quad (33)$$

Here the threshold voltage shift, ΔV_{th} results from quantum mechanical phenomena, which is expressed as Equation. (34) [19],

$$\Delta V_{th} = \frac{kT}{q} \ln \frac{\alpha \text{Erf}\left(\frac{t_{si}}{2} \sqrt{\frac{N_d q^2}{2\epsilon_{si} kT}}\right)}{\frac{N_d}{N_c} \frac{4\pi kT}{h^2} [2m_{d,1}^* \sum_n e^{-E_{1,n}/kT} + 4m_{d,2}^* \sum_n e^{-E_{2,n}/kT}]} \quad (34)$$

The expression for the drain current when considering the full channel is given as Equation (35),

$$I_d = \frac{\phi(L + L_{deff}) - \phi(-L_{seff})}{R_{eq}} \quad (35)$$

The applied potential along the channel can therefore be expressed as Equation (36)

$$\begin{aligned}
 \phi(x) = & \frac{V_{ds} + \frac{qN_d}{2\epsilon_{si}}[(L + L_{deff})^2 - L_{seff}^2]}{(L + L_{deff} + L_{seff})} L_{seff} + \frac{qN_d}{2\epsilon_{si}} L_{seff}^2 \\
 & + \frac{V_{ds} + \frac{qN_d}{2\epsilon_{si}}[(L + L_{deff})^2 - L_{seff}^2]}{(L + L_{deff} + L_{seff})} x - \frac{qN_d}{2\epsilon_{si}} x^2 \quad (36)
 \end{aligned}$$

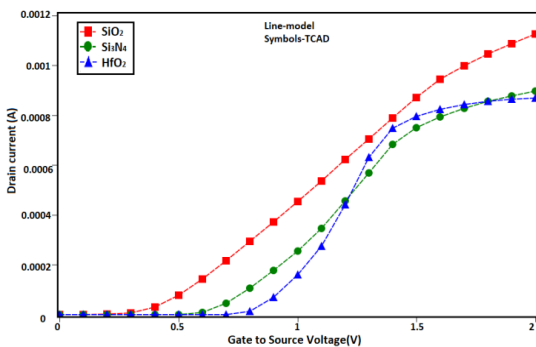


Figure 5. Transfer characteristics plot of hexagonal DGJLFET for various gate dielectric constants

5. RESULTS AND DISCUSSIONS

Using the TCAD device simulator, the model thus obtained is validated by contrasting the device's transfer and output characteristics derived from the mathematical expressions with those derived from simulating the device on TCAD. The transfer and output characteristics are displayed in Figure 5 and Figure 6 for various gate dielectric constant values (K for SiO_2 , Si_3N_4 , and HfO_2 are 3.9, 6.9, and 22, respectively) for hexagonal DG JLFET. The gate capacitance rises in tandem with the gate dielectric constant. Consequently, the features show improved controllability with lower DIBL. Nevertheless, a stronger depletion layer might result from a higher K dielectric, which would lower ON current. Also, the transfer and output characteristics are displayed in Figures 7 and 8 for different value of doping concentration ($N_d = 10^{18}/\text{cm}^3$, $5 \times 10^{18}/\text{cm}^3$ and $10^{19}/\text{cm}^3$). Charge density increases with doping concentration. The threshold voltage will therefore be lower, and the current will be higher in both the on and off states with higher doping concentrations. The transfer and output characteristics are displayed in Figures 9 and 10 for different values of channel length ($L = 20 \text{ nm}$, 25 nm and 30 nm) for a hexagonal DG JLFET. A higher drain current flows when the channel resistance decreases with decreasing channel length.

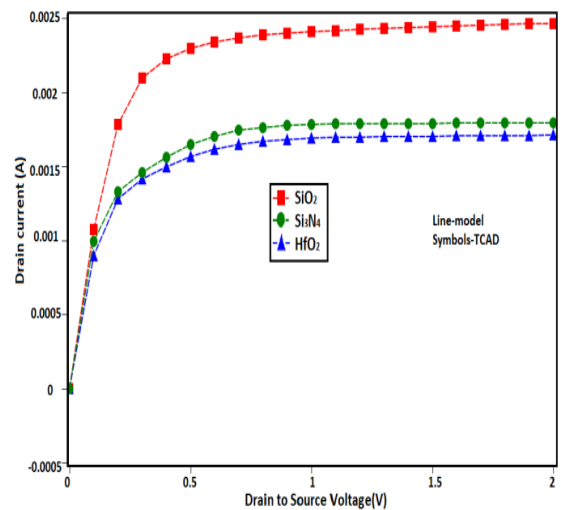


Figure 6. Output characteristics plot of hexagonal DGJLFET for various gate dielectric constants.

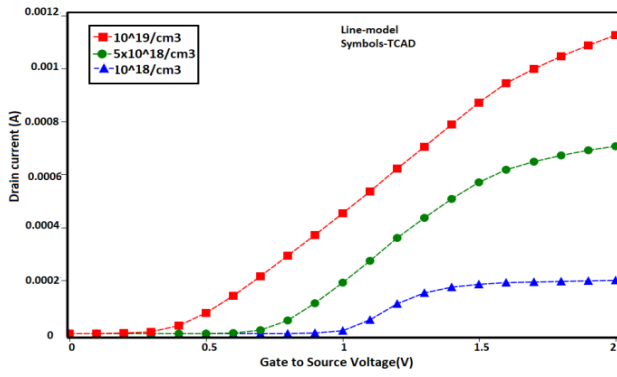


Figure 7. Transfer characteristics plot of hexagonal DGJLFET for various doping concentration.

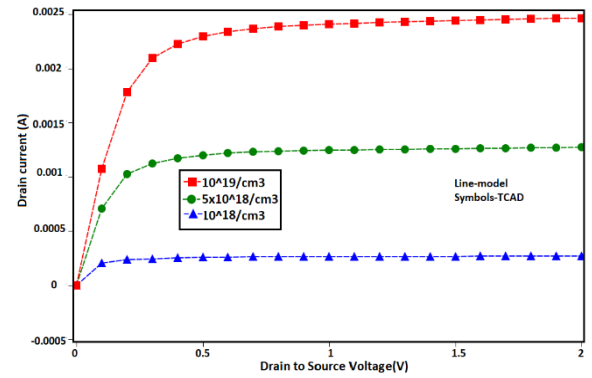


Figure 8. Output characteristics plot of hexagonal DGJLFET for various doping concentration.

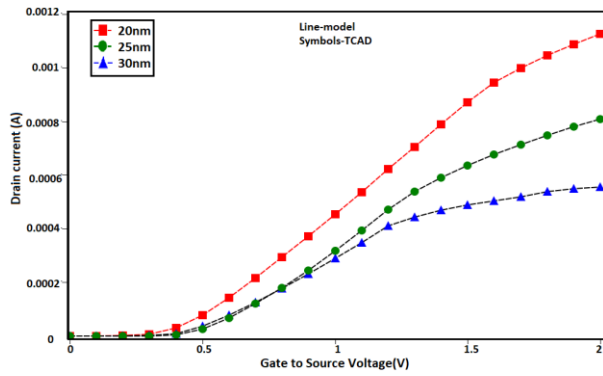


Figure 9. Transfer characteristics plot of hexagonal DGJLFET for various channel length.

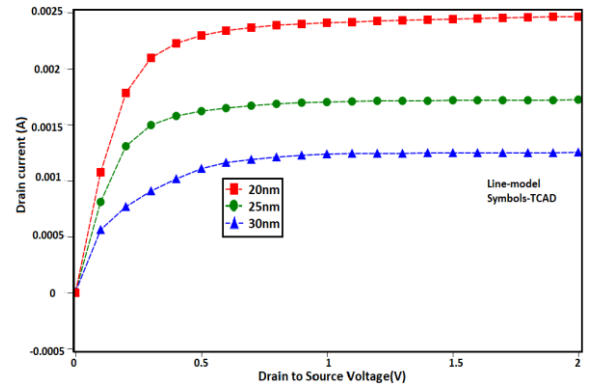


Figure 10. Output characteristics plot of hexagonal DGJLFET for various channel length.

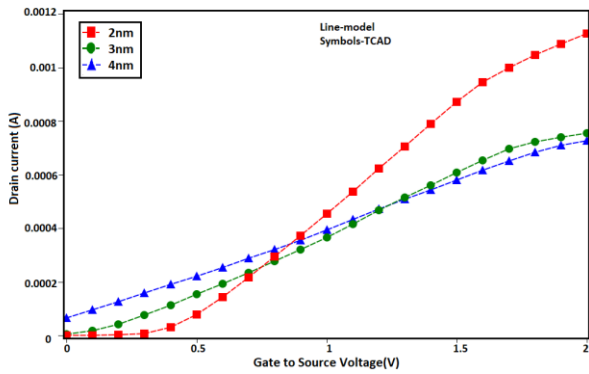


Figure 11. Transfer characteristics plot of hexagonal DGJLFET for various gate dielectric thickness.

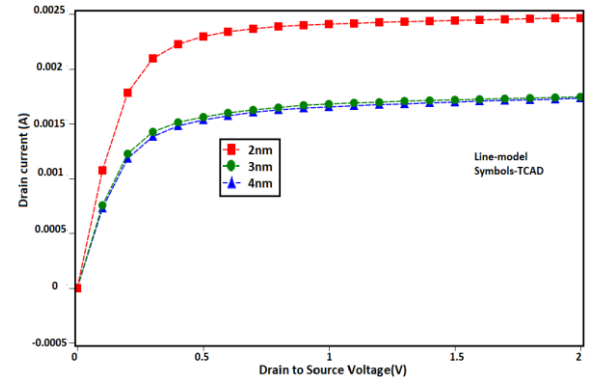


Figure 12. Output characteristics plot of hexagonal DGJLFET for various gate dielectric thickness.

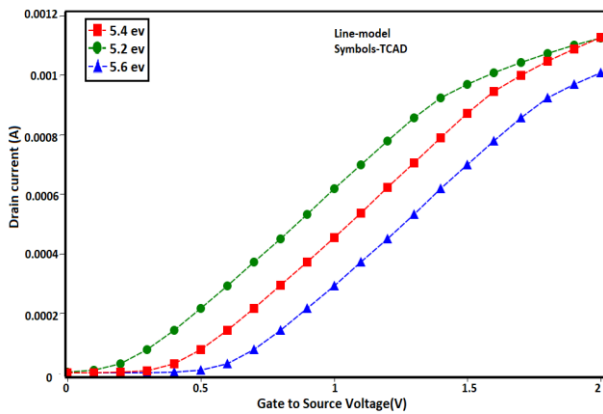


Figure 13. Transfer characteristics plot of hexagonal DGJLFET for various gate work function.

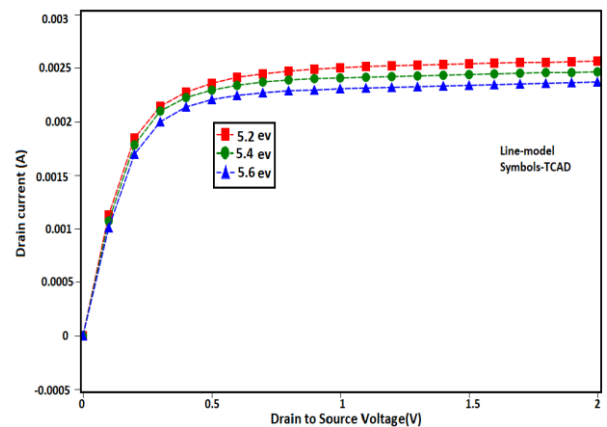


Figure 14. Output characteristics plot of hexagonal DGJLFET for various gate work function.

Again, the transfer and output characteristics are displayed in Figure 11 and Figure 12 for various gate dielectric thickness values ($t_{ox} = 2 \text{ nm}, 3 \text{ nm}, 4 \text{ nm}$). As oxide thickness increases, gate capacitance falls because gate controllability diminishes, increasing off-state current and decreasing on-state current. The transfer and output characteristics are displayed in Figures 13 and 14 for different values of work function ($\Psi = 5.2 \text{ eV}, 5.4 \text{ eV}, \text{ and } 5.6 \text{ eV}$) for hexagonal DG JLFET. Because the gate and substrate have different work functions, a drop in work function reduces the internally induced electric field, which lowers channel resistance and increases drain current. The transfer characteristics for various drain-to-source voltages ($V_{ds} = 0.1 \text{ V}, 0.3 \text{ V}, \text{ and } 0.5 \text{ V}$) are displayed in Figures 15 and 16 displays the output

characteristics for various gate to source voltages ($V_{gs} = 0 \text{ V}, 1 \text{ V}, 2 \text{ V} \text{ and } 3 \text{ V}$) for hexagonal DG JLFET. Higher drain voltage results in higher DIBL, which in turn improves the current due to larger biasing voltage. According to the output characteristics, a thicker depletion layer and lower current are implied by a lower gate voltage. Figure 17 shows that with a high-k dielectric constant, the capacitive coupling increases, thereby increasing gate capacitance, resulting in less DIBL, which reduces subthreshold swing. Figure 18 shows that with a lower dielectric constant, higher is the ON-state current and as the dielectric constant increases the ON-state current decreases. Figures 19 and 20 show a comparison of the mathematical model with experimental results for the validity of the model.

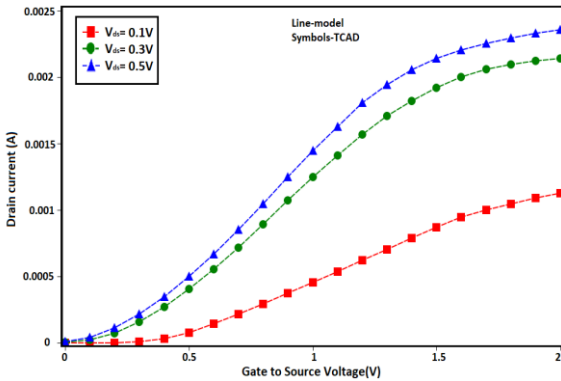


Figure15. Transfer characteristics plot of hexagonal DGJLFET for various drain to source voltages

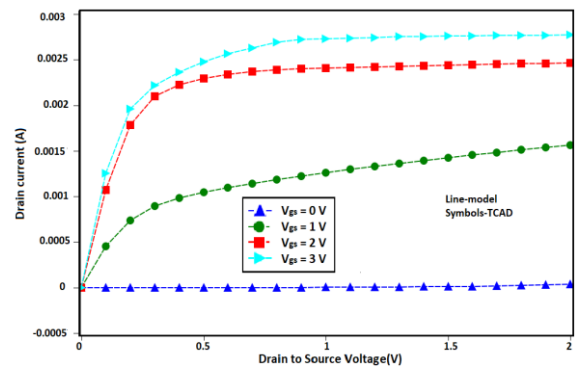


Figure 16. Output characteristics plot of hexagonal DGJLFET for various gate to source voltages

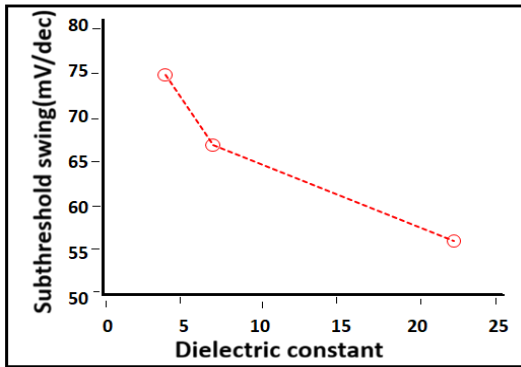


Figure 17. Subthreshold swing plot of hexagonal DGJLFET for various dielectric constant

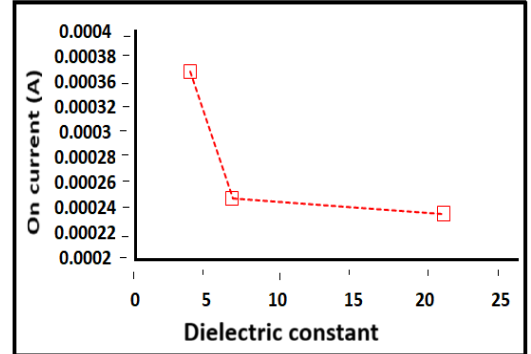


Figure18. On current plot of hexagonal DGJLFET for various dielectric constant.

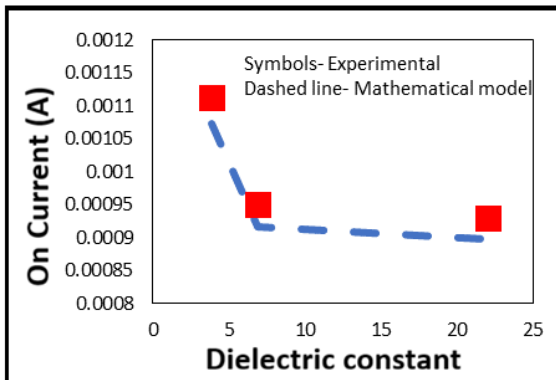


Figure 19. On current plot of hexagonal DGJLFET for various dielectric constant

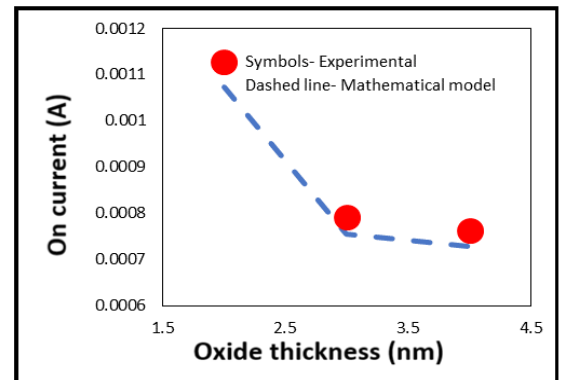


Figure 20. On current plot of hexagonal DGJLFET for various oxide thickness

6. CONCLUSIONS

This study presents an analytical model for drain current in the channel area of a double-gated junctionless field effect transistor with a hexagonal structure that is valid in all four operating regions of the device. Finally, the mathematical model for computing the drain current of a hexagonal-based double-gate JLFET is presented, which consists of both simulation and experimental validation. The model produced is totally analytical, which reduces the calculation time in designing. The device's channel resistance serves as

the basis for the model. The proposed device's transfer and output characteristics indicate the dependence of drain current on many factors such as gate oxide thickness, gate dielectrics, doping concentration, channel length, and work function. The model's output is compared with the numerical simulation results from TCAD and experimental results. The model agrees closely with both simulation (average 2% deviation) and experimental (average 3.6% deviation) results.

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