

A novel technique for designing ternary logic arithmetic circuits using GNRFETs to enhance energy efficiency and circuit performance

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ABSTRACT

Ternary logic systems provide many benefits over typical binary logic, including faster logic and arithmetic operations, lower connection complexity, and a smaller footprint. This study describes ternary logic circuit designs. A novel design strategy is presented for developing ternary logic circuits using graphene nanoribbon field-effect transistors (GNRFETs). The GNR dimer line controls the GNRFET's threshold voltage and width. Designs such as half adder and multiplier circuits are presented using fewer transistors. The adder and multiplier schematics are created utilizing a variety of ternary unary operators. The Synopsys HSPICE tool is used to build and simulate the proposed circuitry. The proposed designs' performance parameters, including delay, power dissipation, and power delay product (PDP), are studied and compared with typical CNTFET circuits. The proposed schematics enhanced overall performance by up to 42.12% over CNTFET devices. Furthermore, the PDP of the proposed designs is compared to previous literature. The suggested circuits enhance the PDP by up to 69.64% compared to the current works. In addition, the effect of process, voltage, and temperature (PVT) variations on the proposed adder and multiplier designs is examined. It was discovered that adder and multiplier circuits exhibited the fewest differences in performance for PVT fluctuations. The ternary full adder circuit is then developed as a complex circuit and compared to a CNTFET-based circuit to determine its performance.

Keywords: Ternary, Graphene, GNRFET, Adders, Multiplier and HSPICE.

1. INTRODUCTION

Recently, the two-valued logic states are inadequate for developing digital circuits because of large interconnections, large occupied area and high energy-dissipation, respectively [1-5]. Alternatively, multiple-valued logic (MVL) consists of more than two logic levels that reduce the interconnection [6], reduce the area by 70% [7] and improve the energy-dissipation by 50% [8]. In [9], it is discussed that the utilization of ternary logic in design of digital circuit improves the design complexity and cost over the other MVL logics. Ternary logic consists of logic levels 0, 1 and 2 that correspond to 0, $V_{DD}/2$, and V_{DD} , respectively.

Ternary circuit designs utilizing silicon technology have challenges such as short-channel effects and large leakage currents [1-3]. Hence, researchers have proposed various alternative technologies such as Fin-transistors [10], single-electron transistors [11], quantum-dot transistors [12], carbon nanotube FETs (CNTFETs) [13-15] and graphene nanoribbon FETs (GNRFETs) [16-20], respectively. Out of these techniques, GNRFETs provide a promising approach for digital circuits because they offer energy-efficient and high-speed circuits. Compared to traditional bulk-silicon technologies, GNRFETs offer exceptional carrier mobility and near-ballistic transport capabilities, which translate to significantly higher switching speeds and enhanced circuit performance. Furthermore, the atomically thin, one-dimensional nature of graphene nanoribbons provides superior electrostatic control over the conductive channel.

This strong gate control drastically mitigates SCEs and minimizes subthreshold leakage currents. By leveraging the tunable bandgap of GNRFETs which can be precisely engineered via the nanoribbon width and edge geometry designers can optimize the threshold voltage to balance power and performance. Consequently, employing GNRFETs plays a pivotal role in achieving ultra-energy-efficient and high-speed digital architectures, making them exceptionally well-suited for realizing the advanced ternary arithmetic circuits proposed in this work.

Using GNRFETs, various ternary schematics are designed in [16-18]. The basic gates, universal gates, decoder, half adder and full adder are implemented in [16]. The ternary adder and multiplexer using decoders are discussed in [17]. In [18], the adder, subtractor and multiplier schematics are presented. However, all these existing literature uses single supply and decoder circuits in the designs. Using the single supply and decoders in the circuits, increases the heat, there is a direct connection among large and small possible voltages, increases transistors and increases power dissipation [19]. Moreover, limitations of existing papers [16-18] are provided in Table I.

Hence, in this work, new designs of unary operators, half adder and multiplier circuits using GNRFET technology are presented. The delay, power, PDP, and the effects of PVT variations on the performance of the proposed circuits are also investigated. Moreover, proposed GNRFET schematics

are also compared with CNTFET circuits and existing GNRFET designs [16-18]. The ternary full adder circuit is designed as a complex circuit as an extension, and its performance is compared with the CNTFET based circuit. All the proposed circuit schematics are built in HSPICE for transient verification and performance evaluation. The primary contributions of the proposed work are: the GNRFET ternary complex circuits are designed without

using the decoders and encoders that helps to reduce the transistor count, two voltage supplies i.e., V_{DD} and $0.5V_{DD}$ are used that removes the direct connection from V_{DD} to GND, the additional ternary operators are used to develop the adder and multiplier that reduce the transistor count and improve the overall performance and the PVT variations are also investigated and compared to existing CNTFETs and GNRFETs based circuits.

Table I. Limitations of existing designs [16-18].

Method	Refs.	Year	Details	No. of Transistors		Limitations
				Adder	Multiplier	
Traditional Design	[16]	2020	▪ Uses Ternary Decoders	284	-	▪ Large Transistor Count ▪ High PDP ▪ High EDP ▪ Large Circuit Area
	[17]	2020	▪ Uses Single supply	90	-	
	[18]	2023	▪ Uses basic gates	100	76	

The remainder of the work is arranged as follows: Section 2 describes GNRFET background. The discussion on ternary unary operator is presented in Section 3. The design of ternary adder and multiplier schematics are discussed in Section 4. The comparative study with the existing works and PVT variation effect on performance are also discussed in Section 5. Finally, the conclusion is presented in Section 6

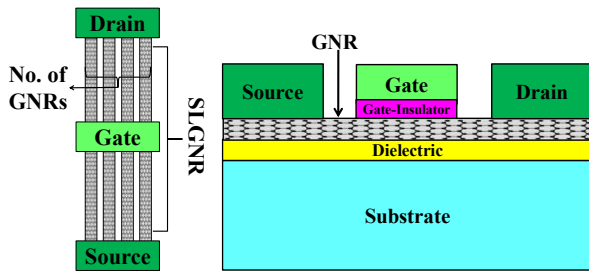


Figure 1. GNRFET structure.

2. GNRFET TRANSISTOR

In this work, the University of Illinois GNRFET model presented in [21-23] is used. The GNRFET structure is shown in Figure 1. GNRFETs utilize the semi-conductive armchair single-layer GNR (SLGNR) sheets as a channel. The carbon atom arrangement across the sheet of SLGNR is dimer line and it is represented by (n) . The dimer line value of SLGNR determines whether the SLGNR is a conductor or a semiconductor. If $n = 3i$ or $3i+1$, then the SLGNR is semiconductor and it is conductor for $n = 3i+2$, (i is a positive integer). The GNR width is stated as

$$W_{SLGNR} = \frac{\sqrt{3}(1+n)a_0}{2} \quad (1)$$

where n is a dimer line value and a_0 is the distance between the carbon atoms, respectively. The GNRFET threshold voltage (V_{GT}) is defined as

$$V_{GT} = \frac{E_{gp}}{3e} \quad (2)$$

$$E_{gp} = \frac{2 \cdot |\Phi| \cdot h_{pc} \cdot V_{fr} \cdot \pi}{W_{SLGNR}} \quad (3)$$

where E_{gp} is the bandgap, e is charge of electron, h_{pc} is Planck's value and V_{fr} is fermi velocity, respectively. The detailed on the $|\Phi|$ is given in [16-19]. The characteristics of GNRFETs look similar to the MOSFET. The current and voltage curves of GNRFETs are given in Figure 2. It is found that high drain current for large dimer line value. In the proposed work, we have used only two dimer line GNRs $n = 6$ and 12 , respectively. The relation of these dimer lines with the width and threshold values is given in Table .

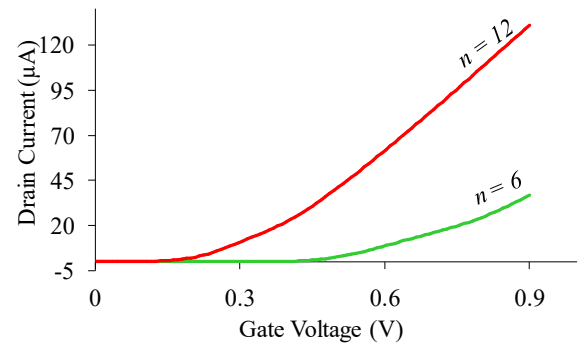


Figure 2. Current and Voltage curves of GNRFET.

Table 2. The relation of dimer line, width and threshold voltage of GNRFETs

Dimer Line (n)	Width (W_{SLGNR})	Threshold Voltage (V_{GT})	
		N-GNRFET	P-GNRFET
6	0.86nm	0.43V	-0.43V
12	1.60nm	0.23V	-0.23V

3. TERNARY LOGIC UNARY OPERATORS

The logic gate which consists of single input and output is called a unary operator. In conventional binary logic, there are four unary operators (i.e., 00, 11, 01, 10). Whereas, in ternary logic, there are 27 unary operators (i.e., 000, 001,....., 222). In this work, we have focused on 8 unary operators are X_p , X_n , X_1 , X^1 , X^2 , $\overline{X^2}$, $1 \cdot \overline{X_p}$ and $1 \cdot \overline{X_n}$, respectively. The 1st and 2nd operators X_p and X_n represent

positive (PTI) and negative (NTI) inverters, respectively. The 3rd operator X_I is known as decisive lateral. The 4th and 5th operators are called as cycle operators, X^1 and X^2 are the single and dual shift operators. The 6th operator $\overline{X^2}$ is complement of X^2 and last unary operators are $1 \cdot \overline{X_p}$ and $1 \cdot \overline{X_n}$, respectively. The circuit diagrams of the 8 unary operators and truth tables are given in Figure 3 and Table 3. Moreover, the operations of unary operators X^2 , X_I and X^1 are presented in Table 4. The eight proposed unary operators are developed and simulated in HSPICE tool to verify functionality. The obtained simulations result of the operators given in Figure 4. The input signal, X , is subjected

to a comprehensive step sequence, transitioning through the defined ternary logic levels: logic 0 (0 V), logic 1 (0.45V), and logic 2 (0.9V). The corresponding output waveforms demonstrate the correct logical evaluations for the respective unary operations. The waveforms exhibit full voltage swings with sharp transition edges, indicating robust drive strength and minimized propagation delay. Notably, the intermediate voltage level (0.45V) remains stable without significant degradation or voltage drop, which confirms that the resistive voltage division and threshold voltage parameters of the proposed transistor network are optimally sized to preserve noise margins.

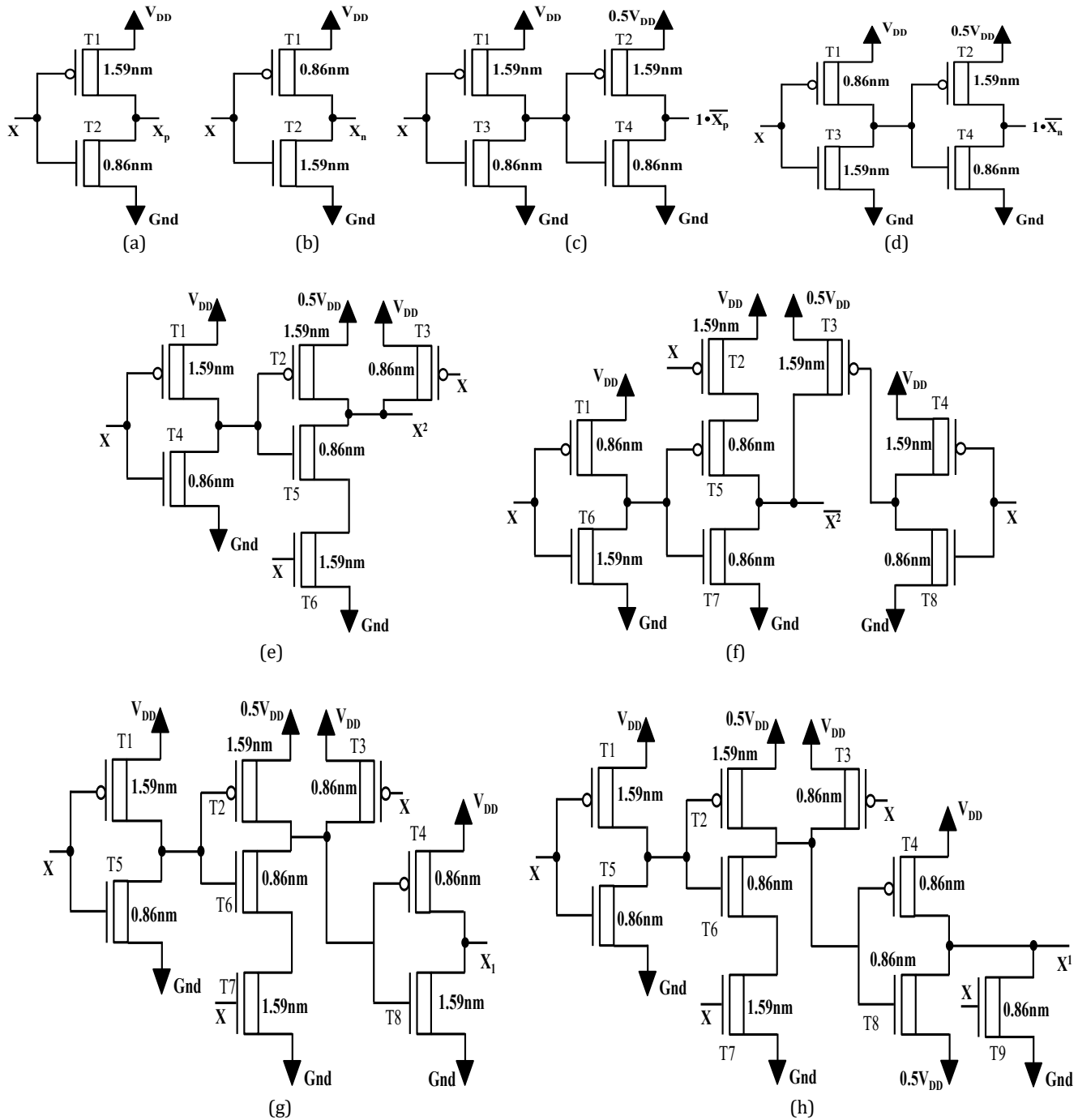


Figure 3. Ternary logic unary operators (a) X_p , (b) X_n , (c) $1 \cdot \overline{X_p}$, (d) $1 \cdot \overline{X_n}$, (e) X^2 , (f) $\overline{X^2}$, (g) X_I and (h) X^1 , respectively.

Table 3. Unary Operators Truth table

X	X_p	X_n	$1 \cdot \overline{X_p}$	$1 \cdot \overline{X_n}$	X^2	$\overline{X^2}$	X_I	X^I
0	2	2	0	0	2	0	0	1
1	2	0	0	1	0	2	2	2
2	0	0	1	1	1	1	0	0

Table 4. Operations of X^2 , X_I and X^I unary operators

X	X_p	Transistor State						Output		
		X^2		X_I		X^I		X^2	X_I	X^I
		ON	OFF	ON	OFF	ON	OFF			
0	2	T5 T3	T2 T6	T8	T4	T8	T4 T9	2	1	0
1	2	T5 T6	T2 T3	T4	T8	T4	T8 T9	0	2	2
2	0	T2 T6	T5 T3	T8	T4	T9	T4 T8	1	0	0

Table 5. Half Adder and Multiplier Truth table

X	Y	Half Adder		Multiplier	
		Sum	Carry	Product	Carry
0	0	0	0	0	0
0	1	1	0	0	0
0	2	2	0	0	0
1	0	1	0	0	0
1	1	2	0	1	0
1	2	0	1	2	0
2	0	2	0	0	0
2	1	0	1	2	0
2	2	1	1	1	1

4. PROPOSED ADDER AND MULTIPLIER DESIGNS

In this work, we propose a ternary half adder with 36 GNRFETs and multiplier with 23 GNRFETs. The proposed

adder and multiplier schematics are developed using the unary operators discussed above functions, transmission gates and two voltage-supplies (V_{DD} and $V_{DD}/2$), respectively.

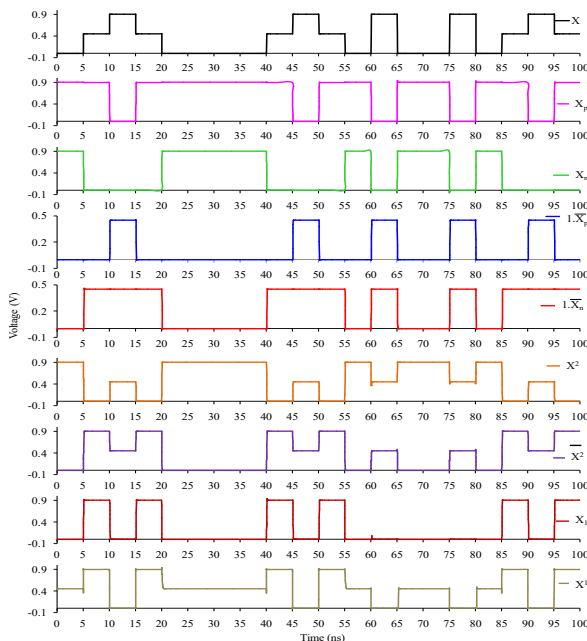


Figure 4. Output responses of unary operators.

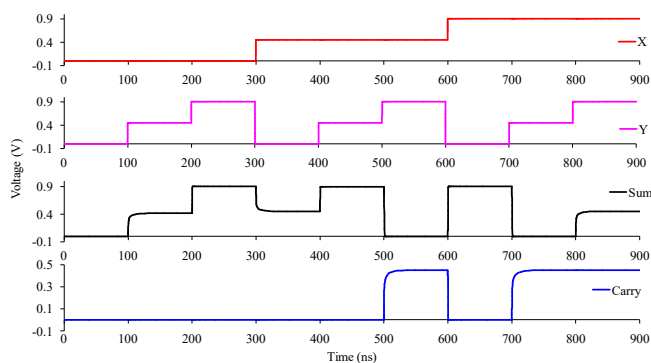


Figure 6. Waveform of Half Adder.

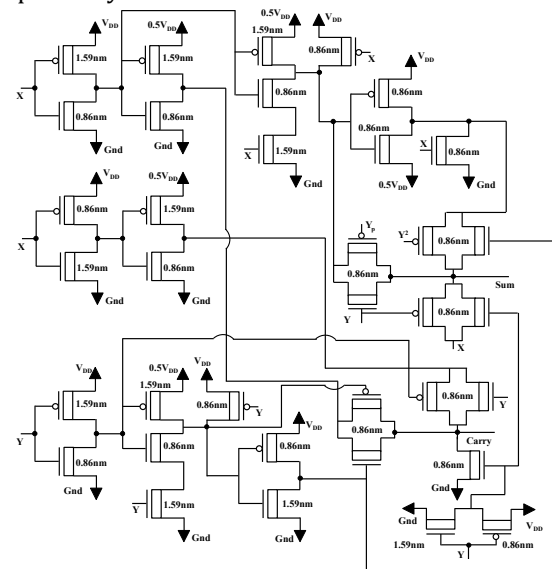


Figure 5. Circuit diagram of Half Adder.

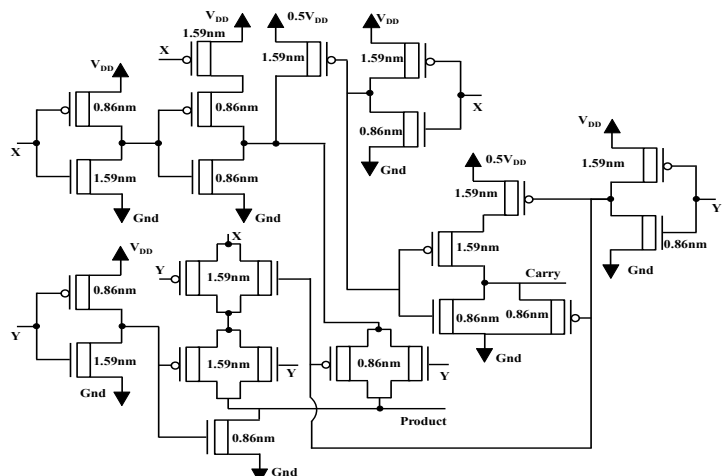


Figure 7. Circuit diagram of Multiplier.

4.1. Half Adder

The one-trit adder that adds two inputs and produces the two outputs (i.e., Sum and Carry) is presented. The truth table and expressions of Sum and Carry are provided in Table 5 and equ. (4).

$$\begin{aligned} Sum &= X \cdot Y_0 + X^1 Y_1 + X^2 Y_2 \\ Carry &= 0 \cdot Y_0 + (1 \cdot \overline{X_p}) \cdot Y_1 + (1 \cdot \overline{X_n}) \cdot Y_2 \end{aligned} \quad (4)$$

Using the equation (4), the adder is developed and illustrated in Figure 5. The proposed half adder is developed and simulated in HSPICE to acquire the

transient response and performances. The transient response is illustrated in Figure 6. To validate the design across all possible states, inputs X and Y are stimulated with waveforms that cycle through all nine distinct input combinations for a 2-input ternary gate. The temporal simulation confirms that the Sum and Carry outputs strictly adhere to the ternary addition truth table. For instance, during the time interval where $X = 2$ (0.9V) and $Y = 2$ (0.9V), the circuit correctly computes a decimal 4, resulting in a ternary 11₃. This is accurately reflected in the waveforms as both the Sum and Carry outputs transition to logic 1 (0.45V).

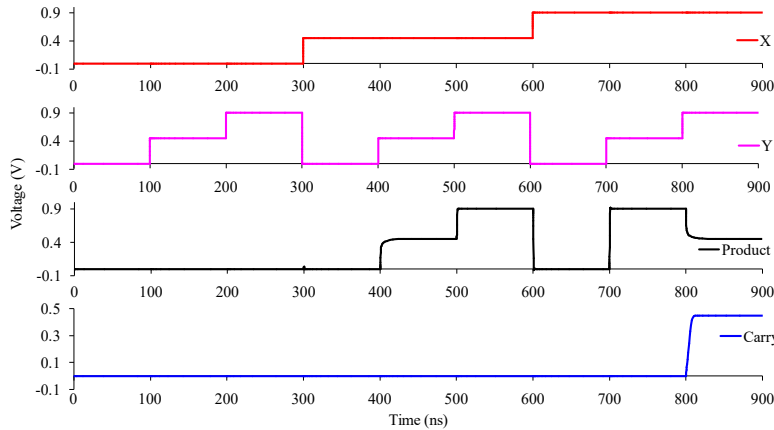


Figure 8. Waveform of Multiplier.

The transient analysis further reveals that the outputs settle rapidly to their steady-state logic levels without observable glitches, ringing, or dynamic hazards, demonstrating the dynamic stability and low contention of the internal nodes. Moreover, the delay, power and PDP are analyzed and obtained as 208.8ns, 4.25μW and 0.88pJ, respectively.

4.2. Multiplier

The one-trit multiplier that multiplies the two inputs and produces the two outputs (i.e., Product and Carry) is presented. The truth table and numerical equations of Product and Carry are given in Table 5 and equ. (5). Using the equation (5), the multiplier is developed and illustrated in Figure 7. The transient response of multiplier is illustrated in Figure 8. Similar to the adder verification, the inputs X and Y are varied to exhaustively test all nine multiplier states. The output waveforms for the Product and Carry accurately map to theoretical ternary multiplication. For example, the critical worst-case transition occurs when $X = 2$ and $Y = 2$, yielding a decimal product of 4 (ternary 11₃). The simulation accurately captures this, with both Product and Carry settling at 0.45V (logic 1). The technical analysis of these waveforms highlights the circuit's excellent transient characteristics; the transition from logic 0 to logic 2 and particularly the transitions involving the intermediate logic 1 state, maintain high signal integrity. The absence of severe voltage spikes during input switching transitions indicates that the design minimizes short-circuit power dissipation while maintaining reliable data computation. Moreover,

the delay, power and PDP are analyzed and obtained as 229.3ns, 3.738μW and 0.857pJ, respectively.

$$\begin{aligned} Product &= 0 \cdot Y_0 + X \cdot Y_1 + \overline{X^2} Y_2 \\ Carry &= 1 \cdot (X_p + Y_p) \end{aligned} \quad (5)$$

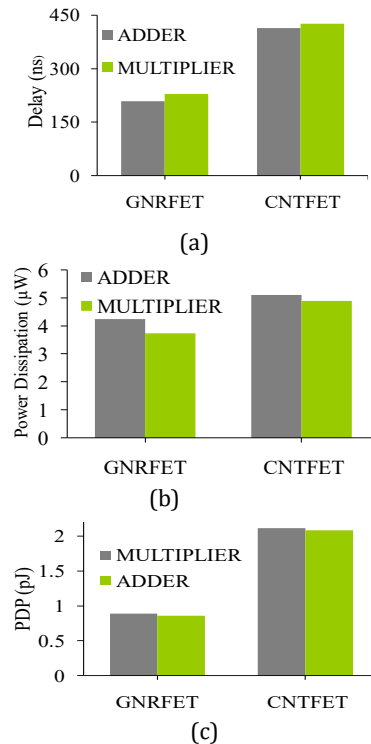


Figure 9. Performance of Adder and Multiplier (a) Delay, (b) Power and (c) PDP.

Table 6. Performance of Proposed and CNTFET Circuits

Half Adder					
Delay (ns)		Power (μ W)		PDP (pJ)	
GNRFET	CNTFET	GNRFET	CNTFET	GNRFET	CNTFET
208.80	413.48	4.25	5.10	0.88	2.11
Multiplier					
Delay (ns)	Power (μ W)	PDP (pJ)	Delay (ns)	Power (μ W)	PDP (pJ)
GNRFET	CNTFET	GNRFET	GNRFET	CNTFET	GNRFET
229.30	425.60	3.73	4.89	0.85	2.08

4.3. Comparative Study

The performance of the proposed designs is examined with CNTFET designs. For CNTFET circuits, CNT-diameters 1.48 and 0.78 nanometers are utilized. The SPICE model of CNTFET discussed in [24, 25] is utilized to develop CNTFET ternary designs. Figure 9 and Table 6 provides performances comparability's of GNRFET and CNTFET based ternary designs. The proposed GNRFET based adder and multiplier circuits show high performance over the CNTFET circuits. In addition, PDP of proposed GNRFET schematics are examined with traditional GNRFET circuits presented in [16-18]. Fig. 10 and Table 7 shows the comparison of proposed circuits with the [16-18]. It is worth noting that the same load and switching patterns of proposed circuits is used for designs of [16-18]. The proposed design shows degraded transistor count and PDP than the existing circuits.

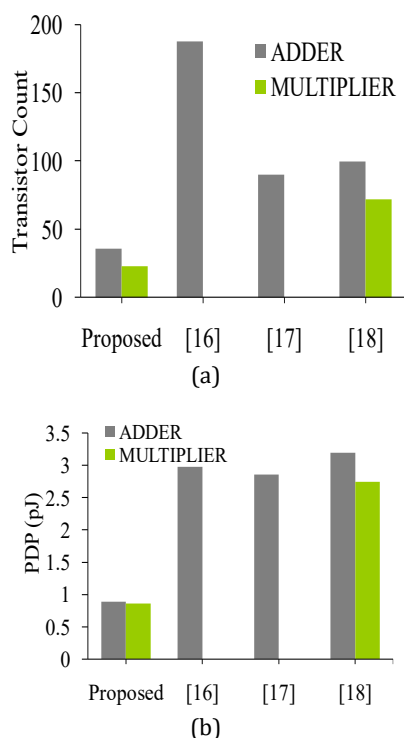


Figure 10. Adder and Multiplier Circuits (a) Transistor Count and (b) PDP.

Table 7. Transistor Count and PDP of proposed and existing works.

Performance	Half Adder				Multiplier	
	[16]	[17]	[18]	Proposed	[18]	Proposed
Transistor Count	188	90	100	36	72	23
PDP (pJ)	2.98	2.86	3.20	0.88	2.75	0.85

4.4. PVT Variations impact on Adder and Multiplier Performance

The ternary circuits are highly sensible to PVT variations. Hence, PDP investigations are carried out for the different PVT variations for adder and multiplier circuits. For the process, the PDP circuits are analyzed by varying the oxide thickness. The obtained PDP results for different oxide thickness are given in Figure 11 and Table 8. The PDP of adder and multiplier circuits is also analyzed by varying the different power supplied and temperature values. The obtained PDP values for adder and multiplier circuits are shown in Figure 12, Table 9, Figure 13 and Table 10, respectively. It worth noting that the PVT variations of proposed circuits are than the existing circuit designs. The PDP of the proposed circuits is improved compared to the existing works. The minimal deviation in PDP can be attributed to the following analytical factors:

In GNRFETs, the total gate capacitance is a series combination of oxide capacitance (C_{ox}) and the quantum capacitance (C_Q) of the channel. Because C_Q is relatively small and often dominates the equivalent capacitance, the total gate capacitance becomes highly insensitive to physical variations in T_{ox} . Consequently, the charging and discharging times of the load capacitance remain stable, preserving the propagation delay and dynamic power dissipation.

The PDP demonstrates strong stability across supply voltage scaling. This is fundamentally due to the near-ballistic carrier transport properties of the channel material. At typical operating voltages, the carriers rapidly reach velocity saturation. Therefore, minor fluctuations in the lateral electric field (caused by V_{DD} noise) do not drastically alter the on-current (I_{ON}). Because the drive current remains relatively bounded, the delay variations are constrained. Simultaneously, the steep subthreshold swing intrinsic to the proposed device structure effectively suppresses exponential increases in static leakage power when V_{DD} fluctuates, keeping the overall PDP tightly controlled.

The proposed logic designs exhibit minimal PDP degradation across varying operating temperatures. Unlike conventional silicon, where elevated temperatures cause severe carrier mobility degradation (due to acoustic phonon scattering) and significant threshold voltage roll-off, the band structure and density of states in the proposed channel technology offer higher thermal stability. The variation in the off-state leakage current is significantly less temperature-dependent. This means that at higher temperatures, the static power dissipation does not dominate the dynamic power, allowing the total energy metric (PDP) to remain stable across the simulated thermal range.

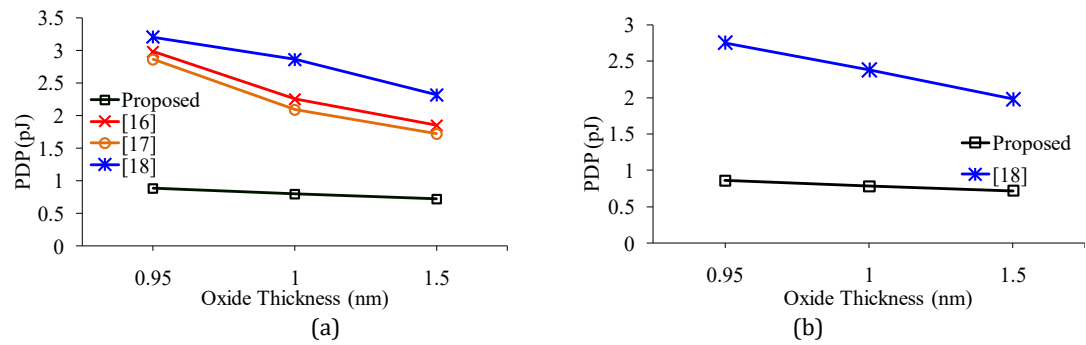


Figure 11. Process variation effect on PDP (a) Adder and (b) Multiplier.

Table 8. PDP values of proposed and existing works.

T _{ox} (nm)	PDP (pJ)					
	Half Adder			Multiplier		
	[16]	[17]	[18]	Proposed	[18]	Proposed
0.95	2.98	2.86	3.2	0.88	2.75	0.85
1	2.25	2.09	2.86	0.79	2.38	0.78
1.5	1.85	1.72	2.32	0.72	1.98	0.71

Table 9. PDP values of proposed and existing works.

Supply (V)	PDP (pJ)					
	Half Adder			Multiplier		
	[16]	[17]	[18]	Proposed	[18]	Proposed
0.8	2.76	2.63	3.02	0.78	2.58	0.76
0.9	2.98	2.86	3.2	0.88	2.75	0.85
1	3.10	2.95	3.39	1.20	2.98	1.10

Table 10. PDP values of proposed and existing works.

Temperature (°C)	PDP (pJ)					
	Half Adder			Multiplier		
	[16]	[17]	[18]	Proposed	[18]	Proposed
50	2.98	2.86	3.2	0.88	0.85	2.75
60	3.0236	2.945	3.365	0.94	0.95	2.86
70	3.125	3.005	3.458	1.10	1.0	2.95

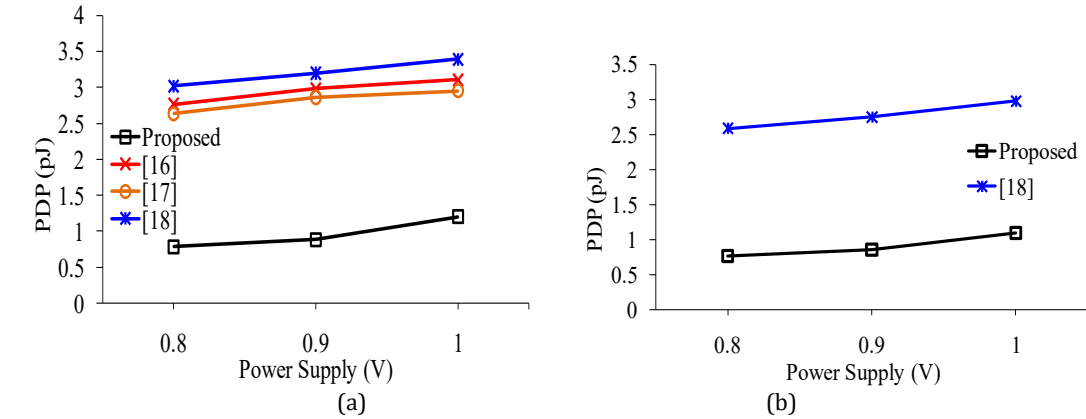


Figure 12. Power supply variation effect on PDP (a) Adder and (b) Multiplier.

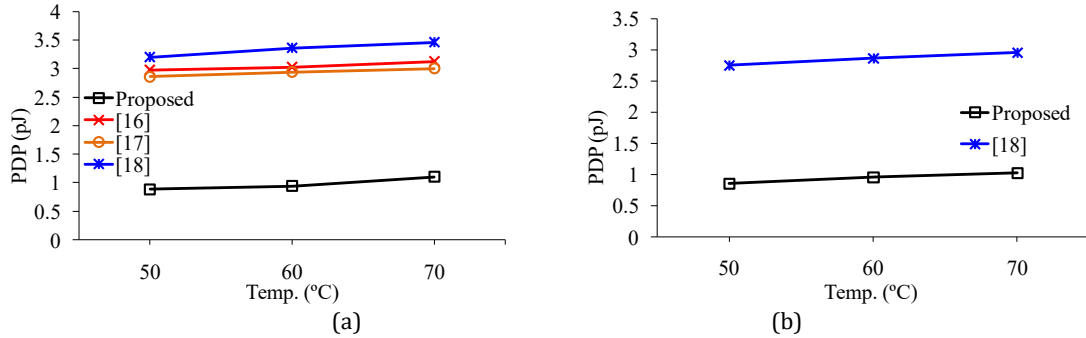


Figure 13. Temperature variation effect on PDP (a) Adder and (b) Multiplier.

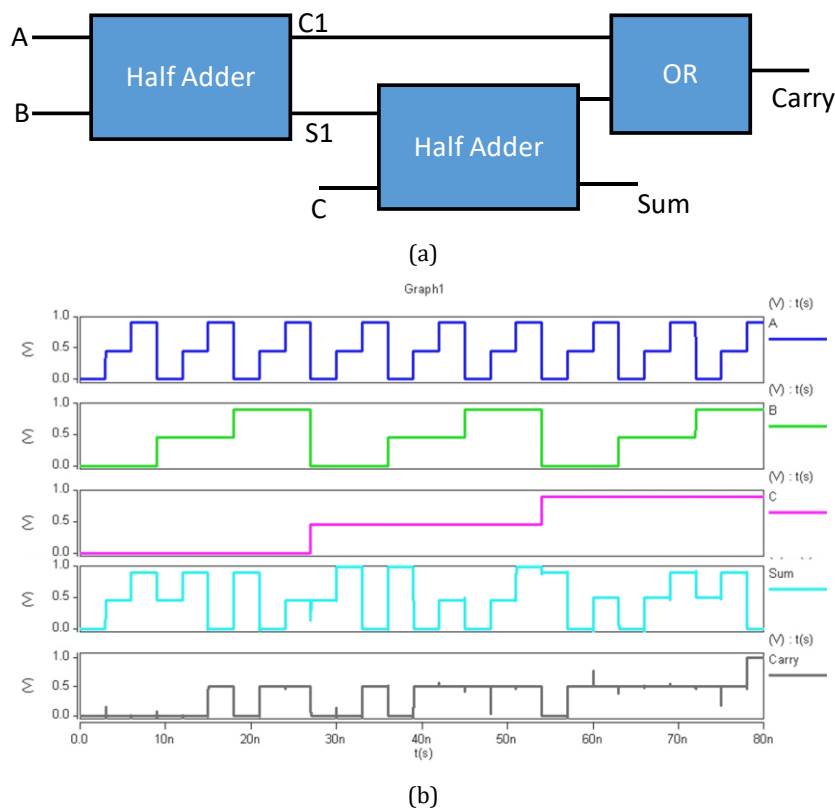


Figure 14. Full Adder (a) Circuit and (b) Output Response.

Table 11. Performance of Proposed and CNTFET Full Adder Circuit

Delay (ns)		Power (μW)		PDP (pJ)	
GNRFET	CNTFET	GNRFET	CNTFET	GNRFET	CNTFET
418.65	863.99	15.43	35.34	6.45	30.58

It is worth noting that the full adder circuit can be designed using the two half adders and one OR gate. Hence, we have extended this work to design the ternary full adder circuit as complex design. The circuit diagram of full adder is shown in Fig. 14a. The output response obtained from the HSPICE simulator is shown in Fig. 14b. Furthermore, the performances for the proposed GNRFET based full adder is compared with the CNTFET based full adder circuit. Table 11 shows the comparative study of proposed and CNTFET full adders. It is noticed that the GNRFET based full adder shows high performance over the CNTFET based full adder.

5. Conclusion

A new design technique is proposed to develop ternary adder and multiplier schematics using unary operators. The proposed circuits are designed in the HSPICE simulator for functional verification and performance evaluation. Moreover, simulation results of proposed designs are compared to conventional CNTFET and GNRFET based designs. It is noted that the proposed designs improved the performances over the conventional designs. Moreover, the PVT variations on the performance of the proposed adder and multiplier designs are carried out and noted that the proposed circuits showed minimal variations. Then, the ternary full adder circuit is designed as a complex circuit and compared its performance with the CNTFET based circuit. The proposed full adder shows high performance

compared to existing CNTFET full adder. Because of the betterment in performance than existing designs, the proposed design technique plays an important role in future integrated circuits to achieve high performance.

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