

Modeling and design of an InP/InGaAs HBT for microwave transimpedance amplifiers in 20 Gb/s optical links

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ABSTRACT

This paper presents the design and simulation of an InP/InGaAs heterojunction bipolar transistor (HBT) fabricated on a 6H-SiC substrate for microwave applications. The device is modeled using the Silvaco TCAD simulation tool to analyze its electrical and physical characteristics. The heterojunction structure enables efficient carrier confinement and enhanced electron injection, leading to improved current gain and high-frequency performance. Key simulation results, including the energy band diagram, Gummel characteristics, output characteristics, recombination profile, and potential distribution, demonstrate the high quality of the device and its suitability for high-speed operation. The transistor exhibits a high current gain of $\beta = 250$, a transition frequency of $f_T = 66$ GHz, and a maximum oscillation frequency of $f_{max} = 70$ GHz confirming its potential for microwave circuit applications. The parameters extracted using Silvaco are subsequently imported into Keysight Advanced Design System (ADS) to implement a two-stage shunt-series feedback transimpedance amplifier (TIA) targeting 20 Gb/s optical links. The TIA achieves a transimpedance gain of 45 dB Ω , a -3 dB bandwidth of 14.5 GHz, and a supported data rate of approximately 20 Gb/s. The amplifier demonstrates unconditional stability across the entire 0–20 GHz frequency range, a noise figure in the range of 6.25–7.8 dB, and a group delay variation of 10 ps within the passband. Overall, the proposed InP/InGaAs HBT on a 6H-SiC substrate offers promising performance for high-frequency and microwave circuit integration, and the Silvaco-to-ADS design flow provides a rigorous and physically grounded methodology for device-to-circuit performance prediction.

Keywords: Heterojunction bipolar transistors; InP/InGaAs; TCAD; ADS; microwave; transimpedance amplifiers; optical receivers.

1. INTRODUCTION

Heterojunction bipolar transistors (HBTs) are bipolar devices in which the emitter, base, and collector are formed from different semiconductor materials, creating bandgap and band-offset engineering that improves carrier injection, transit time, and breakdown compared with homojunction bipolar transistors [1]. In III–V technology, HBTs based on indium phosphide (InP) and indium gallium arsenide (InGaAs) have become key devices for high-speed, low-power analog and digital integrated circuits, particularly in the millimeter-wave and terahertz (THz) range and in fiber-optic communication systems [2], [3]. InP-based HBTs exploit the combination of a wide-bandgap InP emitter/collector and a narrow-bandgap InGaAs base to obtain high emitter injection efficiency, low base resistance, and very short minority-carrier transit times [4]. These material properties, including the high electron mobility and high thermal conductivity of InP, enable operation at very high cutoff frequencies with relatively low supply voltages and low DC power consumption compared with Si, SiGe, or GaAs bipolar technologies [2]. Continuous scaling and refinement of InP/InGaAs single and double HBT (DHBT) structures have pushed unity-current-gain cutoff

frequencies (f_T) and maximum oscillation frequencies (f_{max}) into the sub-THz and THz regimes [5], [6], [7].

A central research direction has been substrate and epitaxial-stack engineering to reconcile conflicting requirements of high thermal conductivity, electrical isolation, and lattice matching. Traditional InP/InGaAs HBTs grown lattice-matched on semi-insulating InP substrates offer low defect densities and good RF performance but suffer from limited wafer size and relatively high cost [8]. Metamorphic buffer layers on GaAs allow the growth of InP/InGaAs DHBTs with excellent DC and RF performance while leveraging cheaper, larger-diameter GaAs substrates [9]. High-thermal-conductivity substrates such as SiC, accessed through wafer-bonding transfer of InP-based DHBT epitaxy, reduce device thermal resistance and enable higher current-density operation and record f_T values approaching or exceeding 700–800 GHz [10], [11]. In parallel, advanced device geometries and process optimizations such as emitter-fin architectures, vertical scaling, and base-collector undercut techniques further reduce parasitic resistances and capacitances, enabling simultaneous realization of very high f_T , f_{max} , and breakdown voltage [12], [13]. For system-level

applications, InP/InGaAs-based HBT processes support monolithic integration of high-speed analog front-ends, including photoreceivers operating at tens of gigabits per second, RF power amplifiers, and mixed-signal ICs for millimeter-wave communications [14]. Ongoing work on transferring or bonding III-V HBT epitaxial layers onto insulating or high-thermal-conductivity substrates (e.g., sapphire, SiC) aims to combine superior device performance with improved thermal management and compatibility with large-diameter wafers [15], [16].

Advanced Design System (ADS; Keysight Technologies) is a widely adopted RF and microwave electronic design automation platform that provides unified tools for schematic capture, physical layout, and multi-domain circuit simulation, including DC, AC, S-parameter, harmonic balance, transient, noise, and electromagnetic co-simulation, tailored to the analysis of high-frequency bipolar and FET-based circuits [17], [18], [19]. In typical III-V HBT design flows, physics-based Technology Computer-Aided Design (TCAD) simulations (e.g., Silvaco Atlas) are first used to generate accurate DC characteristics and small-signal S-parameters, from which compact models and equivalent circuit parameters such as saturation current, current gain, transit time, series resistances, and junction capacitances are extracted and mapped onto the HBT macro-models available in ADS [20], [21].

Once parameterized in this way, the ADS environment enables the inclusion of the HBT in complete front-end architectures and its evaluation under realistic source, load, and interconnect conditions, allowing reliable prediction of gain, bandwidth, linearity, noise, and stability over the targeted microwave frequency range. In the context of optoelectronic front-ends, ADS is extensively used for the design of transimpedance amplifiers (TIAs), where co-simulation of the photodiode, HBT-based preamplifier, and subsequent limiting stages provides quantitative assessment of transimpedance gain, -3 dB bandwidth, and input-referred noise, and has been successfully employed in CMOS and InP HBT receiver ICs operating at multi-gigabit data rates [22], [23], [24], [25].

2. HBT DEVICE STRUCTURES

The proposed device is a vertically structured NPN InP/InGaAs heterojunction bipolar transistor realized on an electrically insulating wide-bandgap substrate and summarized schematically in Fig. 1. From bottom to top, the structure consists of a thick semi-insulating 6H-SiC equivalent substrate, whose large bandgap and moderate permittivity, as reported in Table 1, ensure excellent RF isolation and efficient heat extraction under high-current-density operation. On this handle wafer, a heavily doped n^+ InP sub-collector and a moderately doped n -type InP collector are successively grown, providing a low-resistance current path and sustaining the collector-emitter voltage while exploiting the high electron mobility and breakdown strength of InP. The active base region is formed by a thin, heavily doped p^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer lattice-matched to InP; its narrower bandgap and higher electron mobility, highlighted by the material parameters in Table 1, yield a strong conduction-band offset at the InP/InGaAs interface,

which confines injected electrons in the base, suppresses hole back-injection, and simultaneously minimizes base resistance and transit time. Above the base, an n -type InP emitter and an n^+ InP emitter cap complete the double heterojunction, the wide-bandgap emitter ensuring high emitter injection efficiency and low base current, while the heavily doped cap enables the formation of low-ohmic emitter contacts without perturbing the underlying band alignment. Ohmic terminals are then defined lithographically, with the collector contact connected to the n^+ InP sub-collector, lateral base contacts accessing the p^+ InGaAs base, and a top emitter pad on the n^+ InP cap, such that the emitter stripe geometry and access regions are optimized to minimize parasitic resistances and capacitances in view of microwave operation. This carefully engineered InP/InGaAs/InP heterostructure on a wide-bandgap insulating substrate, as depicted in Fig. 1 and parameterized in Table 1, provides the combination of high current gain, low recombination, reduced thermal resistance, and low RF parasitics that underpins the excellent DC and high-frequency characteristics demonstrated in the subsequent Silvaco and ADS simulations.

The simulated HBT consists of an InP emitter and emitter-cap, an InGaAs base, an InP step-graded layer and pulse-doping region, followed by a 6H-SiC subcollector. The emitter has a width of $1.2\ \mu\text{m}$ and a thickness of $0.15\ \mu\text{m}$. The InGaAs base has a width of $3.6\ \mu\text{m}$ and a thickness of $0.055\ \mu\text{m}$. The step-graded layer has a width of $3.6\ \mu\text{m}$, while the pulse-doping region has a width of $2.0\ \mu\text{m}$. Finally, the SiC subcollector has a width of $3.6\ \mu\text{m}$, and the InP emitter cap is defined with a width of $1.2\ \mu\text{m}$ and a thickness of $0.05\ \mu\text{m}$.

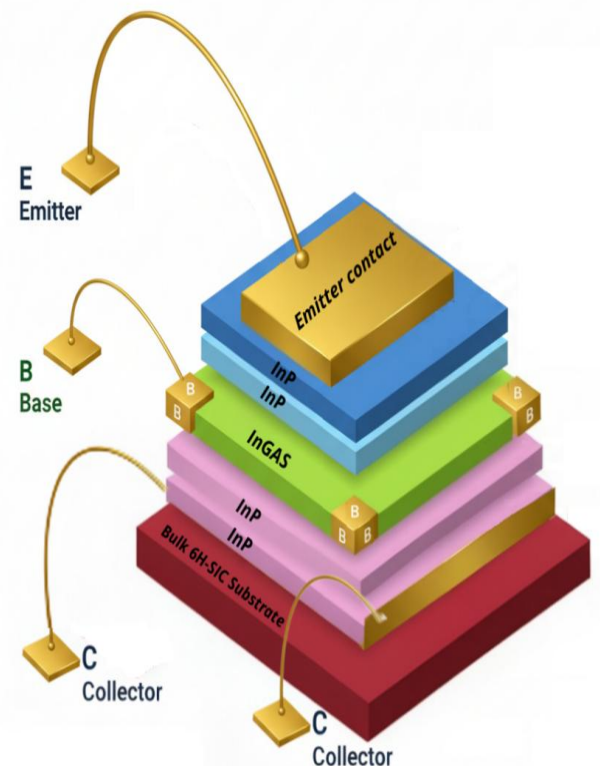


Figure 1. Schematic structure of the proposed InP/InGaAs HBT on a 6H-SiC insulating substrate.

Table 1. Key material parameters of InP, In_{0.53}Ga_{0.47}As, and 6H-SiC at 300 K (literature-based values for TCAD modeling).

Parameter	InP	InGaAs	6H-SiC
Bandgap E_g (eV)	1.34 [1]	0.74 [1]	3.0 [26]
Electron affinity χ (eV)	4.38 [27]	4.5 [28]	3.7 [29]
Permittivity ϵ_r	12.5 [30]	13.9 [28]	9.7 [29]
N_c (cm ⁻³)	5.7×10^{17} [30]	1.0×10^{17} [28]	1.6×10^{19} [29]
N_v (cm ⁻³)	1.1×10^{19} [30]	7.0×10^{18} [28]	2.5×10^{19} [29]
Electron mobility μ_n (cm ² /V·s)	5400 [30]	8500 [28]	800 [29]
Hole mobility μ_p (cm ² /V·s)	150 [30]	400 [28]	115 [29]
τ_n (s)	1×10^{-9} – 1×10^{-7}	1×10^{-9} – 1×10^{-7}	1×10^{-7}
τ_p (s)	1×10^{-9} – 1×10^{-7}	1×10^{-9} – 1×10^{-7}	1×10^{-7}
Doping type	n/p	n/p	n-type

3. ANALYTICAL MODELING

The analytical model is employed to provide a physical interpretation of the TCAD simulation results and the RF behavior of the proposed InP/InGaAs HBT. It is based on a one-dimensional drift-diffusion and charge-control approach using the heterojunction-adapted Ebers-Moll/Gummel-Poon model [31], [32]. The analysis assumes one-dimensional carrier transport, uniform doping in each region, abrupt InP/InGaAs heterojunctions, steady-state operation, and the thin-base approximation ($W_B \ll L_n$). [33][34].

3.1. Minority Electron Transport in the Base

In forward-active operation, electrons are injected from the n-type InP emitter into the p⁺ InGaAs base across the forward-biased emitter-base junction. In the quasi-neutral base $0 < x < W_B$, the steady-state continuity equation for electrons reduces to the diffusion-recombination equation

$$D_n \frac{d^2 \Delta n(x)}{dx^2} - \frac{\Delta n(x)}{\tau_n} = 0 \quad (1)$$

where D_n is the electron diffusion coefficient, τ_n is the minority-carrier lifetime, and $\Delta n(x)$ is the excess electron concentration in the base. Applying the thin-base approximation ($W_B \ll L_n$) yields:

$$J_n(0) \approx q \frac{D_n}{W_B} n_{B0} (e^{V_{BE}/V_T} - 1) \quad (2)$$

Showing that the collector current is primarily controlled by the base width, carrier diffusion, and the equilibrium minority-electron concentration. The equilibrium minority-electron concentration is expressed as:

$$n_{B0} = \frac{n_i^2}{N_B}, n_i^2 = N_C N_V \exp\left(\frac{-E_{g,eff}}{V_T}\right) \quad (3)$$

where N_B is the base doping concentration, n_i is the intrinsic carrier concentration, N_C and N_V are the effective densities of states in the conduction and valence bands, respectively, and $E_{g,eff}$ is the effective bandgap including the InP/InGaAs heterojunction band-offset effects. The wide-bandgap InP emitter suppresses hole back-injection from the base into the emitter, thereby reducing the base saturation current and improving the emitter injection efficiency, which results in a higher current gain than that of conventional homojunction BJTs [31], [33].

3.2. Collector Current and DC Gain

The collector current in forward-active operation is obtained from the minority-electron current density at the emitter-base junction and is expressed as:

$$I_C = A_E J_n(0) \approx A_E q \frac{D_n n_{B0}}{W_B} e^{V_{BE}/V_T} \equiv I_{S,E} e^{V_{BE}/V_T} \quad (4)$$

where A_E is the emitter area and $I_{S,E}$ is the emitter saturation current. The base current is represented by an effective base saturation current,

$$I_B \approx I_{S,B} e^{V_{BE}/V_T} \quad (5)$$

where $I_{S,B}$ accounts for the dominant hole injection and recombination mechanisms in the device. Consequently, the forward common-emitter current gain is

$$\beta_F = \frac{I_C}{I_B} \approx \frac{I_{S,E}}{I_{S,B}} \quad (6)$$

For the proposed InP/InGaAs HBT, the wide-bandgap InP emitter suppresses hole back-injection, while the thin, highly doped InGaAs base reduces carrier recombination. These heterojunction characteristics increase the emitter injection efficiency and result in the high current gain observed in the simulated Gummel characteristics [31][32][33][35].

3.3. Base Transit Time and Intrinsic Capacitances

The high-frequency performance of the proposed InP/InGaAs HBT is primarily determined by the carrier transit time through the base and the intrinsic junction capacitances. Under the thin-base approximation, the base transit time is expressed as:

$$\tau_B = \frac{Q_B}{I_C} \approx \frac{W_B^2}{2D_n} \quad (7)$$

where W_B is the base width and D_n is the electron diffusion coefficient. This relationship shows that reducing the base width and exploiting the high electron mobility of the InGaAs base minimizes the carrier transit time, thereby enhancing the high-speed performance of the proposed HBT. The corresponding base-emitter diffusion capacitance is given by:

$$C_{BE,diff} = \frac{\partial Q_B}{\partial V_{BE}} \approx \frac{Q_B}{V_T} \approx \frac{I_C \tau_B}{V_T} \quad (8)$$

While the total small-signal input capacitance is

$$C_\pi \approx C_{BE,diff} + C_{BE,dep} \quad (9)$$

where $C_{BE,dep}$ is the depletion capacitance of the emitter-base junction. Together with the collector-base capacitance, these intrinsic capacitances govern the frequency response of the device and are incorporated into the ADS small-signal equivalent circuit used for RF performance evaluation [32], [36].

3.4. High-Frequency Figures of Merit

The RF performance of the proposed InP/InGaAs HBT is characterized by the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}). Under the charge-control model, the cutoff frequency is related to the total forward transit time by:

$$f_T \approx \frac{1}{2\pi\tau_F}, \tau_F = \tau_E + \tau_B + \tau_C \quad (10)$$

Where τ_E , τ_B , and τ_C denote the emitter, base, and collector transit times, respectively. Reducing the base transit time and minimizing parasitic capacitances are therefore essential for improving the high-frequency performance of the proposed HBT. Alternatively, the cutoff frequency can be expressed as:

$$f_T \approx \frac{g_m}{2\pi(C_\pi + C_\mu)} \quad (11)$$

where g_m is the transconductance ($g_m \approx I_C/V_T$), and C_π and C_μ are the intrinsic base-emitter and collector-base capacitances, respectively. The maximum oscillation frequency is approximated by:

$$f_{max} \approx \frac{f_T}{2} \sqrt{\frac{1}{g_m R_B (R_C + R_E) + 2\pi f_T R_B C_\mu}} \quad (12)$$

showing that f_{max} is mainly limited by the base resistance and collector-base capacitance. Consequently, the thin InGaAs base, reduced parasitic capacitances, and optimized device geometry adopted in the proposed HBT contribute to the enhanced RF performance demonstrated by the TCAD and ADS simulations [34], [36], [37].

4. RESULTS AND DISCUSSION

4.1. Silvaco TCAD Simulation of InP/InGaAs HBT on 6H-SiC Substrate

The HBT device was simulated using the Silvaco ATLAS simulator. Fermi-Dirac statistics were considered to account for carrier degeneracy, while the field-dependent mobility model was activated using FLDMOB with EVSATMOD=1 to describe carrier velocity saturation under high electric fields. The SRH and Auger recombination mechanisms, together with the optical recombination model, were included. The lattice temperature was fixed at 300 K. To improve the description of high-field electron transport, the hydrodynamic transport model HCTE.EL was applied to electrons with KSN=1.5.

The coupled electron and hole transport equations were solved using the Newton iterative method with a block solution scheme and two carrier types (CARRIERS=2). The bipolar model was activated to account for the coupled transport processes in the HBT. Conduction- and valence-band parameters were also extracted to analyze the energy-band profiles of the device. The selected physical and numerical models were verified using the corresponding PRINT commands.

Figure 2 depicts the energy band profile along the device, showing a clear heterojunction between the InP emitter and InGaAs base. The conduction and valence band discontinuities confirm efficient carrier confinement in the base region, which enhances electron injection from the emitter while reducing hole back-injection. This band alignment is essential for achieving high current gain and high-frequency performance.

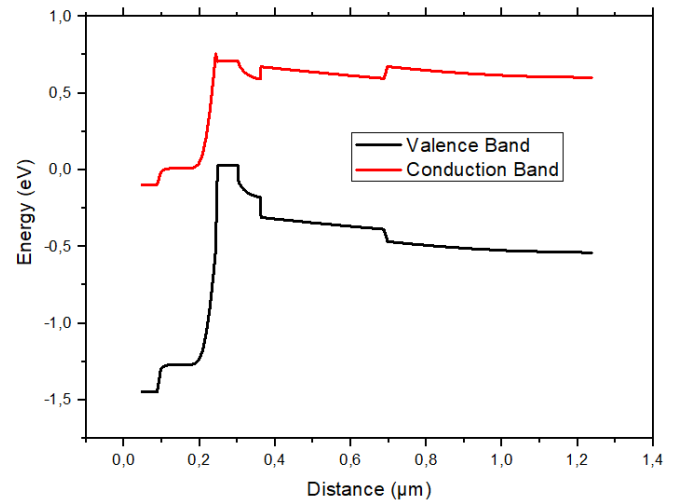


Figure 2. Energy band diagram of the InP/InGaAs HBT on 6H-SiC substrate.

Figure 3 shows the Gummel plot of the proposed InP/InGaAs HBT fabricated on a 6H-SiC substrate. Both the collector current (I_C) and base current (I_B) increase exponentially with the base-emitter voltage (V_{BE}), confirming the excellent bipolar behavior of the device. The collector current rises from approximately 10^{-13} A at $V_{BE} \approx 0.1$ V to about 4×10^{-3} A at $V_{BE} = 1.0$ V, while the base current increases from approximately 10^{-14} A to nearly 1×10^{-2} A over the same voltage range. A significant increase in current is observed between 0.6 V and 0.8 V, corresponding to the transistor turn-on region. The separation between the I_C and I_B curves indicates efficient carrier injection and

a high current gain. The nearly linear behavior on the semi-logarithmic scale suggests diffusion-dominated carrier transport with limited recombination losses. At higher bias voltages ($V_{BE} > 0.8$ V), slight deviations from ideal exponential behavior appear due to high-injection effects and series resistance. These results demonstrate the excellent electrical performance of the proposed InP/InGaAs HBT for microwave and other high-frequency applications.

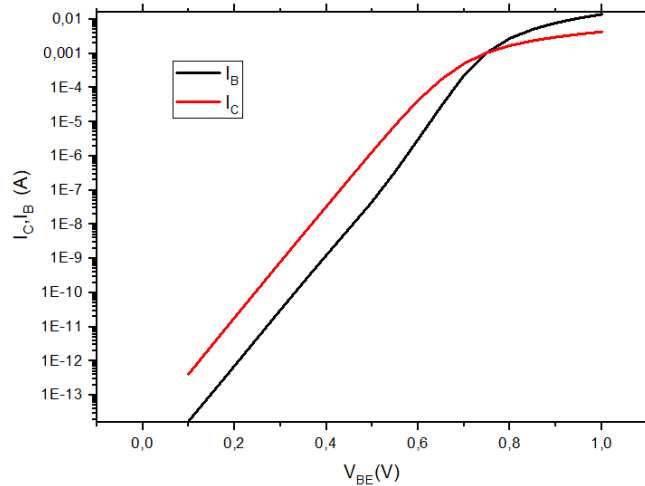


Figure 3. Gummel plot (I_C and I_B vs V_{BE}) of the InP/InGaAs HBT on 6H-SiC substrate.

From Figure 4, we can observe the output characteristics of the InP/InGaAs HBT on a 6H-SiC substrate for base currents ranging from 10 μ A to 40 μ A. The collector current increases rapidly between $V_{CE} = 0.6$ V and 0.8 V, then gradually approaches saturation in the active region. At $V_{CE} = 2.0$ V, the collector current increases from approximately 5.0 mA for $I_B = 10$ μ A to about 9.8 mA for $I_B = 40$ μ A, demonstrating effective current control by the base current. The nearly flat output curves at higher voltages indicate high output resistance and good transistor performance. These characteristics confirm the excellent potential of the proposed InP/InGaAs HBT for microwave and high-frequency applications.

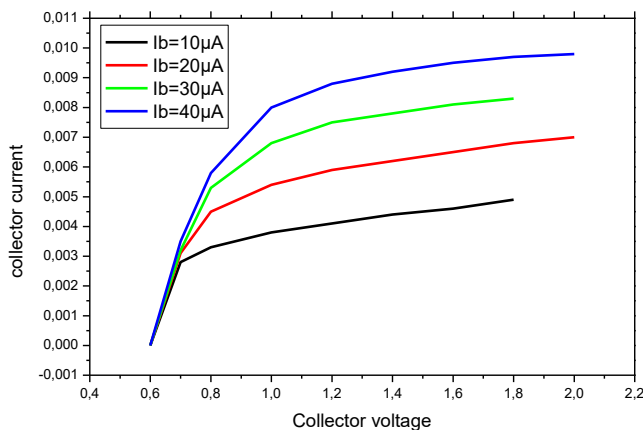


Figure 4. Output characteristics (I_C vs V_{CE}) of the InP/InGaAs HBT on 6H-SiC substrate for different base currents.

The $I_C - V_{BE}$ characteristic of the InGaAs/InP HBT exhibits the expected forward-active behavior. For $V_{BE} < 0.6$ V, the collector current remains almost zero, indicating negligible carrier injection. As V_{BE} increases beyond 0.6 V, I_C rises rapidly, reaching approximately 0.2 mA at 0.65 V, 1.3 mA at 0.8 V, and 4.3 mA at 1.0 V. This strong increase demonstrates efficient carrier transport across the heterojunction and good transistor operation.

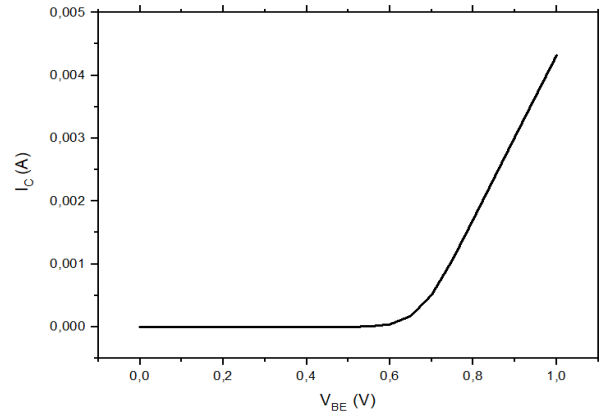


Figure 5. $I_C - V_{BE}$ characteristic of the InP/InGaAs HBT on 6H-SiC substrate.

The current gain β was evaluated from the ratio between the collector and base currents, in the forward-active region. From the output characteristics, at $V_{CE} = 2.0$ V and $I_B = 40$ mA, the collector current reaches approximately 9.8 mA, resulting in $\beta \approx 245$, which is consistent with the nominal value of approximately 250. This result confirms the high current-gain capability of the proposed InP/InGaAs HBT.

Figure 6 shows the recombination rate distribution of the InP/InGaAs HBT on a 6H-SiC substrate. The maximum recombination occurs near the emitter-base and collector-base junctions due to the high carrier concentration in these regions. The recombination rate decreases significantly inside the bulk semiconductor layers, indicating efficient carrier transport and low carrier losses. This behavior reflects the high quality of the InP/InGaAs heterostructure and contributes to improved current gain and high-frequency performance, making the device suitable for microwave applications.

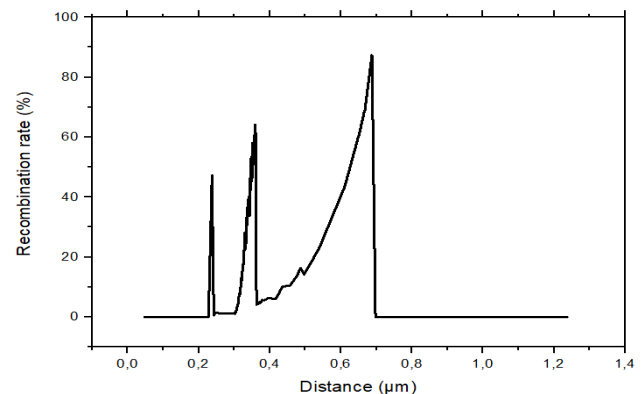


Figure 6. Recombination rate distribution across the InP/InGaAs HBT on 6H-SiC substrate.

The gain (both power gain and current gain H21) decreases with increasing frequency, as expected for high-frequency transistors. However, the device maintains significant gain in the microwave frequency range (tens of GHz), confirming its suitability for microwave amplifier applications. The cutoff frequency (f_T) of 66 GHz and maximum oscillation frequency (f_{max}) 70 GHz, demonstrating excellent high-speed performance.

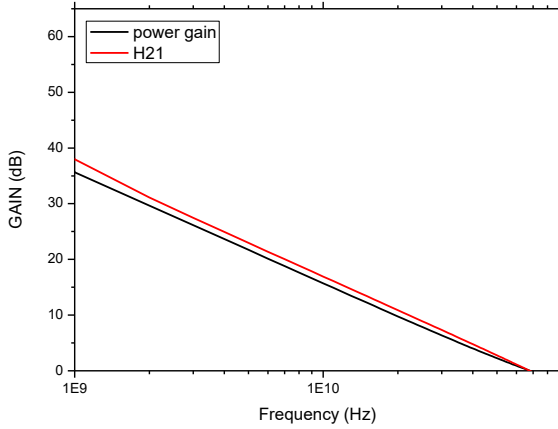


Figure 7. Frequency Response (Gain vs Frequency) of the InP/InGaAs HBT on 6H-SiC substrate.

4.2. Transimpedance Amplifier Design and Simulation in ADS

To transition from device-level simulation in Silvaco to circuit-level design in Keysight ADS, the small-signal S-parameters extracted from the Silvaco simulations are used to populate the ADSHBT model. The key transistor parameters, including saturation current, forward current gain, forward transit time, base resistance, and junction capacitances C_{JE} and C_{JC} , are calculated from the simulated S-parameters and then imported into ADS, ensuring that the simulated transistor in ADS faithfully reproduces the DC and high-frequency behavior established in Silvaco. This methodology provides a direct, physically grounded link between the device-level simulation and the circuit-level performance predictions.

4.2.1. Circuit Topology and Operating Principle

The TIA topology adopted in this work is a two-stage shunt-series feedback amplifier, comprising a common-emitter (CE) gain stage (Q1) followed by a common-collector emitter-follower buffer stage (Q2), with a global feedback resistor R_F closing the loop from the emitter of Q2 back to the base of Q1. This architecture combines the voltage gain of the CE stage with the low output impedance and current drive capability of the emitter follower, while the global shunt-series feedback simultaneously stabilizes the gain, sets the input impedance, and extends the bandwidth.

The TIA schematic shown in Figure 8 consists of a two-stage shunt-series feedback amplifier. Q1 (common-emitter stage) provides the voltage gain, with its collector directly driving the base of Q2 (emitter follower), which acts as an output buffer and ensures low output impedance for 50 Ω

matching. The input node at the base of Q1 includes C_{pd} (15 fF), modeling the photodiode capacitance and dominating the bandwidth limitation. Feedback is provided by R_F (100 Ω), connected from the emitter of Q2 to the base of Q1; It sets the transimpedance gain, controls the feedback depth, and governs the bandwidth–gain tradeoff. R_1 (500 Ω) sets the open-loop voltage gain together with the transconductance of Q1, thereby determining the bandwidth and minimum noise figure. R_2 (250 Ω) is the emitter load of Q2, setting its quiescent current and defining the feedback fraction in the shunt-series loop.

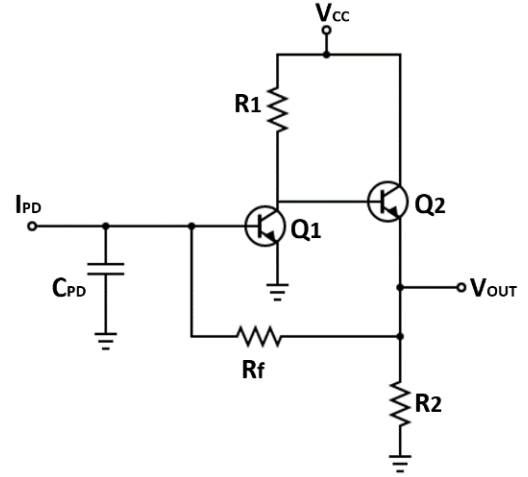


Figure 8. Schematic circuit of the Transimpedance Amplifier

The input current I_{pd} (delivered by a photodiode modeled as C_{pd} in parallel with a current source) is injected at the base of Q1. Q1 converts this current to a voltage at its collector with gain. The emitter follower Q2 reproduces this voltage at its emitter with unity gain and low impedance. The feedback resistor R_F senses the output voltage and returns a fraction of it to the input, creating a negative feedback loop that stabilizes gain, broadens bandwidth, and lowers the input impedance seen by C_{pd} . The overall transimpedance gain is given by:

$$Z_T = \frac{V_{out}}{I_{PD}} \approx \frac{R_F \cdot A}{1+A} \approx R_F \text{ for } A \gg 1 \quad (22)$$

The DC bias network of the TIA consists of a single supply voltage $V_{CC} = 3$ V applied to the collector of Q1 through R_1 and to the collector of Q2 directly. The base of Q1 is biased through the feedback resistor R_F , which self-establishes the DC operating point by sensing the output voltage at the emitter of Q2 and feeding a fraction of it back to the input node, eliminating the need for a separate base bias resistor divider. Unlike amplifiers requiring separate DC and AC feedback paths, the shunt-feedback resistor R_F in this design simultaneously establishes the DC bias point of Q1 and provides the AC negative feedback, simplifying the biasing network to a single supply rail. The resulting quiescent operating point, verified through DC simulation in ADS, is $V_{CE1} = 1.575$ V and $V_{BE1} = 784$ mV for Q1, and $V_{CE2} = 3$ V and $V_{BE2} = 1.575$ V for Q2, with both transistors remaining well within the forward-active region across the simulated frequency range. The emitter of Q2 is biased through R_2 , which sets the buffer stage quiescent current and defines the DC reference for the feedback loop.

The photodiode is modeled as a current source in parallel with Cpd, connected at the base of Q1 through a DC-blocking capacitor to isolate the photodiode's reverse-bias condition (typically $V_{PD} = -3$ to -5 V in a practical receiver) from the base bias of Q1. For small-signal S-parameter simulation, the input port is driven with the standard $50\ \Omega$ source, while a representative input photocurrent amplitude of 10 – $100\ \mu\text{A}$ is assumed for large-signal considerations, consistent with typical InGaAs PIN photodiode responsivity under low-to-moderate optical input power. The output is terminated in a $50\ \Omega$ load, representing the standard measurement and interconnect impedance used for microwave characterization.

All simulations are performed using the ADS S-parameter engine with a frequency sweep from $100\ \text{MHz}$ to $20\ \text{GHz}$. The ADShBT Gummel-Poon model is biased at $V_{CE} = 1.5\ \text{V}$ and a collector current density $J_c = 1.10^4\ \text{A}/\text{cm}^2$. Results are presented in order from gain and bandwidth, to impedance matching, to transimpedance, to stability, and finally to noise and signal integrity.

4.2.2. Forward Gain: S_{21}

The forward transmission parameter S_{21} , shown in Figure 9, exhibits a flat passband gain of approximately $+4.5\ \text{dB}$ at low frequencies, rolling off smoothly to $+0.5\ \text{dB}$ at $20\ \text{GHz}$. The $-3\ \text{dB}$ bandwidth is $14.5\ \text{GHz}$, confirming that the feedback topology has extended the bandwidth well beyond the intrinsic pole of the CE stage. Using the standard NRZ conversion rule $R_{bit} \approx BW/0.7$, this bandwidth corresponds to a supported data rate of approximately $20\ \text{Gb/s}$, which is the target of this design.

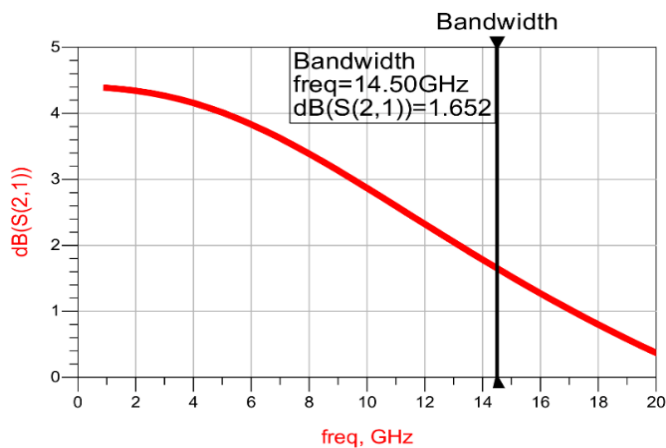


Figure 9. Forward transmission parameter S_{21} versus frequency.

4.2.3. Input and Output Matching: S_{11} and S_{22}

The return loss parameters are presented in Figure 10. The output reflection coefficient S_{22} decreases monotonically from $-10.5\ \text{dB}$ at low frequency to $-12\ \text{dB}$ at $20\ \text{GHz}$, remaining below the $-10\ \text{dB}$ threshold across the entire band. This confirms that the emitter follower output stage provides a well-matched $50\ \Omega$ termination, consistent with the low output impedance characteristic of the common-collector configuration.

The input reflection coefficient S_{11} exhibits a more complex behavior: it decreases from $-12.5\ \text{dB}$ at low frequency to a minimum of $-15.5\ \text{dB}$ near mid-band, before rising back to $-11.5\ \text{dB}$ at $20\ \text{GHz}$. The slight rise at high frequency is attributed to the increasing reactance of C_{be} of Q1 and the decreasing effectiveness of R_f as a shunt feedback element as frequency approaches f_T . Throughout the band, S_{11} remains below $-10\ \text{dB}$, confirming acceptable input matching for a TIA front-end application.

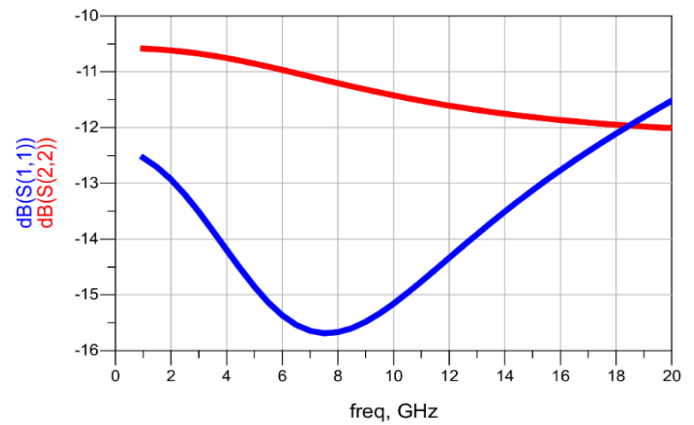


Figure 10. Return loss parameters S_{11} and S_{22} versus frequency.

4.2.4. Transimpedance Gain: Z_T

The transimpedance Z_T in $\text{dB}\Omega$, computed from the S-parameter results as:

$$Z_T(\text{dB}\Omega) = S_{21}(\text{dB}) + 20\log_{10}(2 \times 50) \quad (23)$$

The curve shown in Figure 11 is essentially flat, ranging from $45\ \text{dB}\Omega$ ($\sim 178\ \Omega$) at low frequencies to $40\ \text{dB}\Omega$ ($\sim 100\ \Omega$) at $20\ \text{GHz}$, yielding a flat in-band transimpedance with gradual roll-off toward the band edge. A peak transimpedance of $45\ \text{dB}\Omega$ indicates an effective feedback resistance close to the designed R_f value, confirming that the DC and small-signal operating point is correctly established. The smooth, monotonic roll-off without peaking demonstrates that the feedback is well-damped, which is critical for low inter-symbol interference in the time domain.

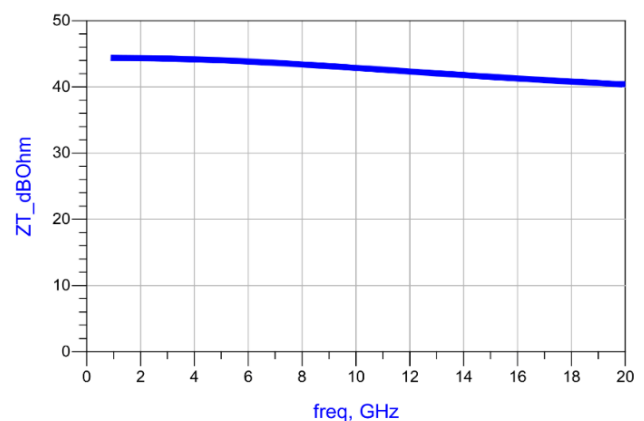


Figure 11. Transimpedance Z_T ($\text{dB}\Omega$) vs frequency

4.2.5. Stability: Rollett Factor (K) and μ -Factor

The Rollett stability factor K and the single-parameter μ -factor are plotted in Figure 12. Both metrics are greater than unity across the entire 0–20 GHz frequency range and exhibit an increasing slope with frequency, indicating that stability margin improves at higher frequencies. Since $\mu > 1$ is a sufficient condition for unconditional stability on its own, the TIA is confirmed to be unconditionally stable under any passive source and load termination at any simulated frequency.

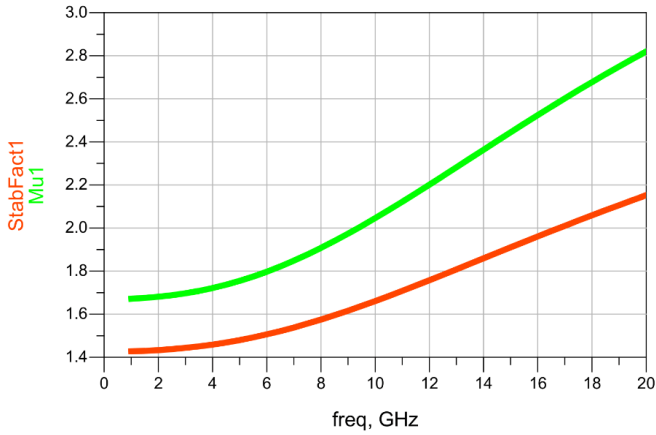


Figure 12. Stability factors K and μ versus frequency.

4.2.6. Noise Performance: NF_{min} and NF

The minimum noise figure NF_{min} and the circuit noise figure NF, both simulated with a 50 Ω source impedance, are shown in Figure 13. NF_{min} increases from 6.25 dB at low frequency to 7.25 dB at 20 GHz, while NF increases from 6.25 dB to 7.8 dB over the same range. The two curves diverge slightly with frequency, reflecting a growing noise mismatch penalty as the optimum noise impedance of Q1 moves further from 50 Ω at higher frequencies. For a TIA in an optical receiver front-end, the noise figure is a secondary figure of merit after bandwidth and transimpedance; however, the relatively small gap between NF_{min} and NF (below 0.6 dB at low frequency) indicates that the input matching provided by the feedback network is close to the optimum noise match at the most sensitive part of the band. The frequency dependence of NF is dominated by the shot noise of the collector current of Q1 and the thermal noise of R_F , both of which increase in relative importance as frequency rises.

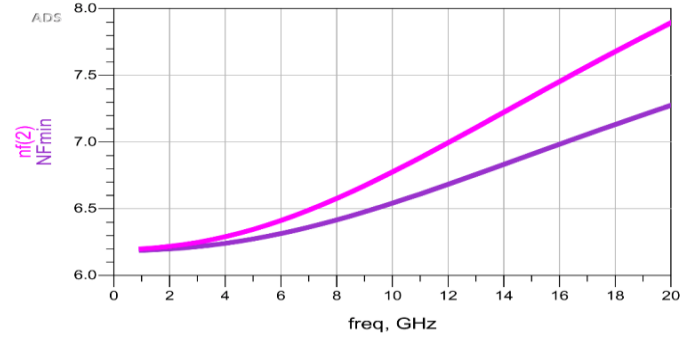


Figure 13. Noise performance of the simulated TIA versus frequency.

4.2.7. Group Delay

The group delay, computed from the derivative of the S21 phase response, is presented in Figure 14. It decreases from 18 ps at low frequency to 8 ps near 20 GHz, corresponding to a total variation of 10 ps across the passband. For a 20 Gb/s NRZ signal with a bit period of 50 ps, this variation represents 20% of the bit period, which is within the acceptable range for low inter-symbol interference operation. The monotonically decreasing group delay rather than a peaked response near the band edge, reflects the absence of resonant poles in the feedback network and confirms that the circuit phase response is well-behaved across the simulated range.

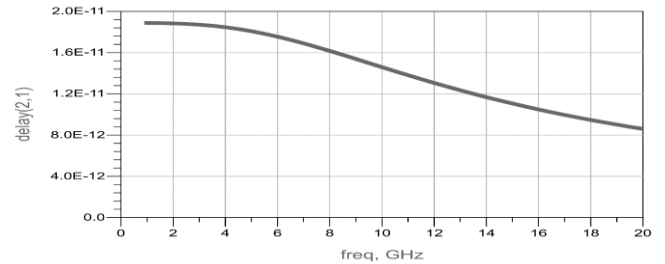


Figure 14. Group delay plot vs frequency

The comparison table shows that the proposed TIA occupies a middle ground between very high-bandwidth research receivers and more conventional 20 Gb/s-class TIAs. Its main strength is not record-breaking bandwidth, but a balanced combination of 14.5 GHz bandwidth, 45 dB Ω transimpedance, unconditional stability, and acceptable noise performance in a topology derived directly from the Silvaco-extracted HBT model

Table 2. Performance comparison of different TIA circuits

Parameter	InP HBT TIA, 2010 [39]	InP PIN/DHBT TIA, 2022 [40]	CMOS TIA, 2022 [41]	CMOS TIA, 2023 [42]	This work
Technology	0.25 μ m InP HBT	1.55 μ m InP PIN + DHBT	0.18 μ m CMOS	28 nm CMOS	InP/InGaAs HBT (Silvaco $\rightarrow$ ADS)
Topology	Distributed TIA	DHBT TIA front end	Single-stage TIA	Shunt-feedback TIA example	CE + emitter follower, shunt-series feedback
Supply voltage	- 4.0 V	N/R	1.8 V	0.95 V	3 V
Power consumption	304 mW	N/R	4.6 mW	N/R	15 mW
Bandwidth	>110 GHz	27 GHz	$\sim$ 22 GHz	19 GHz	14.5 GHz

Data-rate relevance	100 GbE class	20 Gb/s NRZ	~20 Gb/s	40 Gb/s	~20 Gb/s NRZ capability
Transimpedance gain	50 dB Ω	36 dB	40 dB Ω	58 dB Ω	45 dB Ω
Gain-bandwidth product	>35000 Ω ·GHz	~970 Ω ·GHz	~1,940 Ω ·GHz	~14,000 Ω ·GHz	~2,580 Ω ·GHz
Group delay	N/R	N/R	8–15.6 ps	N/R	8–18 ps
Input-referred noise	N/R	N/R	9.7 pA/ $\sqrt{\text{Hz}}$	8 pA/ $\sqrt{\text{Hz}}$	NF = 6.25 dB

CONCLUSION

This work presents the design and simulation of an InP/InGaAs heterojunction bipolar transistor implemented on a 6H-SiC substrate for microwave and high-speed applications. The device was modeled using Silvaco TCAD to investigate its electrical and physical behavior. The heterojunction structure ensures efficient carrier confinement and improved electron injection, resulting in enhanced device performance. Simulation results, including energy band diagrams, Gummel plots, output characteristics, recombination profiles, and potential distribution, confirm the good quality of the device. The transistor exhibits a high current gain of $\beta = 250$, a cut-off frequency $f_T = 66$ GHz, and a maximum oscillation frequency $f_{max} = 70$ GHz, demonstrating strong suitability for high-frequency operation. These results highlight the effectiveness of the proposed device structure for microwave applications. Furthermore, the extracted parameters from Silvaco TCAD were implemented in Keysight ADS to design a two-stage shunt-series feedback transimpedance amplifier (TIA) for 20 Gb/s optical communication systems. The TIA achieves a transimpedance gain of 45 dB Ω and a –3 dB bandwidth of 14.5 GHz. It also supports a data rate close to 20 Gb/s with stable operation. The circuit remains unconditionally stable over the entire 0–20 GHz frequency range. In addition, it presents a low noise figure between 6.25 and 7.8 dB, with limited group delay variation. Overall, the proposed InP/InGaAs HBT on 6H-SiC substrate shows excellent potential for microwave and high-speed integrated circuits. The Silvaco-to-ADS design methodology provides a reliable approach for accurate device-to-circuit performance prediction. These results indicate that the proposed device and circuit are well suited for applications in high-speed optical communication systems, microwave amplifiers, radar front-ends, millimeter-wave circuits, and broadband high-frequency integrated systems.

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