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Investigation on Geometrical Effects of FinFET Electronic Device Properties Using TCAD Simulations and Taguchi Optimization

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ABSTRACT

Accurate determination of transistor size parameters is necessary to provide ideal operating conditions and performance. Using Design of Experiments (DoE) techniques to enhance device performance and efficiency, this work explores the Taguchi strategy for optimizing device parameters in a 7 nm Silicon FinFET. This study examines how geometric scaling influences FinFET performance, focusing on the ratio of on-state current (ION) to off-state current (IOFF), threshold voltage (VTH), subthreshold swing (SS), and drain-induced barrier lowering (DIBL). The Taguchi method is used to improve the FinFET model, leading to better performance. In addition, the study of the impact of improved FinFETs on the performance of logic circuits, especially regarding delay and power requirements. Silvaco TCAD Simulator is used in this work for simulation and analysis. The Taguchi method was used to identify the optimal factor combination for robust device performance, with orthogonal arrays and Signal-to-Noise Ratio (SNR) as the selected quality parameter. The parameters considered in the Design of Experiments (DoE) include Length (LG), Fin Height (HFIN), and Fin Width (WFIN) in the top region. The parameters for the ION/IOFF ratio, VTH, DIBL, and SS were identified using Taguchi's robust performance signal-to-noise ratio (SNR). The VTH value is 0.7461V for the FinFET, with LG, WFIN, and HFIN ranging 13 nm, 7 nm, and 35 nm, respectively. FinFET yielded a current ratio of 262.072 and SS of 72 mV/dec when LG was 13 nm, WFIN was 5 nm, and HFIN was 40 nm. When the FinFET has LG, WFIN, and HFIN of 10 nm, 10 nm, and 35 nm, respectively, it produces the optimum DIBL of 232 mV/V. Overall, the analysis demonstrates that FinFET performance can be substantially enhanced by dimension optimization. Additionally, the Taguchi approach effectively identified the optimal parameter combinations, which were then employed in logic circuits to create low-power FinFETs.

Keywords: *Design of experiments (DoE), SiO2, off-current (IOFF), on-current (ION), SN ratio, Taguchi method, TCAD simulation, fin length (LG), fin height (HFIN), fin width (WFIN), threshold voltage (VTH), subthreshold swing (SS), drain-induced barrier lowering (DIBL)*

1. INTRODUCTION

FinFET is a potential successor to CMOS device architectures in the nanometer range. It provides great control over Short Channel Effects (SCEs) such as leakage current, Drain-Induced Barrier Lowering (DIBL), and perfect sub-threshold slope. Compared to earlier FinFET nodes, including 14 nm and 22 nm, 7 nm FinFETs feature reduced critical dimensions, such as channel Length (LG) and fin pitch, resulting in enhanced electrostatic gate control and improved device performance. In semiconductor design, critical dimensions refer to key physical parameters that impact performance and manufacturability, including gate LG, Fin Width (WFIN), and Fin Height (HFIN). According to the International Technology Roadmap for Semiconductors (ITRS), FinFET will propel technology from the sub-nanometer range up to the 5 nm node [1], [2]. Various manufacturers, including Samsung, GlobalFoundries, and Intel, are working at the 14 nm node. Broadwell-y, an Intel Core M processor, is built on 14 nm technology. Intel is primarily focused on increasing HFIN to optimize FinFETs. In particular, FinFET VTH properties are determined by HFIN and WFIN. In this work, the design optimization of FinFET performance focuses on device dimensions consisting of channel LG, WFIN, and HFIN. The electrical characteristics of a 7 nm FinFET, including VTH, ION/IOFF ratio, SS, and DIBL, are optimized using the Taguchi method and Design of Experiments (DoE) approach. Thus, to understand the performance characteristics, the effects of varying fin LG, WFIN, and HFIN on VTH, ION/IOFF ratio, SS, and DIBL are studied.

2. LITERATURE REVIEW

The SCE occurs when the conductive channel LG of a FinFET is less than 20 nm, or even 10 nm. Notably, the impacts of decreasing channel LG include a lower Threshold Voltage (VTH) and a reduced leakage-induced barrier. In particular, shorter-gate LGs in FinFETs reduce channel control capacity [3]. This makes it challenging for the gate voltage (VG) to displace the channel, leading to subthreshold leakage. Furthermore, the short-channel effect is more

likely to occur [4]. Generally, LG should be more than or equal to WFIN for better DIBL control and a current ratio.

Additionally, DIBL is a unique method for assessing SCEs in electronics. Notably, DIBL tends to increase as LG scales down, with LG determined by the devices' scaling LG [5]. Moreover, the FinFET structure was developed to address scaling issues, which limited device scalability. High leakage current in short-channel transistors reduces switching performance by lowering the ION/IOFF ratio. In line with this, ION and IOFF are key electrical characteristics for evaluating device performance, particularly switching speed and standby time [6]. Accordingly, to obtain reliable switching performance, ION should be higher and IOFF as close to zero as possible, resulting in a high ION/IOFF ratio. Off-state leakage current is also reduced through technological advancements. However, the older MOSFETs have surpassed their key scalability and performance limits. One major downside of this device is its extremely low threshold potential, which allows for prompt device startup [7], [8]. Note that the reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the Gate-to-Source Voltage (VGS) is lower than the VTH [9]. In FinFETs, the VTH can be reduced to improve device performance while also decreasing leakage current significantly [9], [10].

Meanwhile, the SS increases significantly when the gate LG is shortened. In particular, the SS increases with increasing Drain-to-Source voltage (VDS). It is caused by an enhancement of subthreshold current due to the drain effect, which lowers the potential barrier height [11]. Conclude that it aims to optimize the electrical characteristics of a 7 nm FinFET using the Taguchi method and DoE. Additionally, it examines how various fin LG, WFIN, and HFIN impact electrical characteristics such as VTH, ION/IOFF ratio, SS, and DIBL.

Key geometrical parameters include gate LG, WFIN, and HFIN, which impact FinFET performance under aggressive scaling. These variables—VTH roll-off, DIBL, Subthreshold Swing (SS), and current ratios (ION/IOFF)—are essential to lowering SCEs. Investigations show that accurate tuning of LG, WFIN, and HFIN is needed to maintain electrostatic integrity in devices scaled below 14 nm. [12]. Reducing WFIN and HFIN in 14 nm SOI FinFETs increases SS and reduces leakage; however, this affects the RF cutoff frequency, as demonstrated by Boukortt et al. [13]. On the contrary, previous studies have shown that non-uniform doping, together with small fins (WFIN = 4 nm, HFIN = 20 nm), can result in ultra-low leakage and a small DIBL [14]. Furthermore, it has been shown that when WFIN decreases from 10 nm to 5 nm, the ON current increases. However, this reduction also results in a 50% increase in DIBL and a 14% increase in SS, highlighting the sensitive trade-off between drive strength and electrostatic degradation [15].

Further caution is warranted, as quantum confinement effects at the 5 nm scale fundamentally limit the benefits of aggressive fin narrowing [16]. Despite the depth of existing work, few studies attempt to co-optimize all three parameters (LG, WFIN, HFIN) within a unified experimental design.

To address the challenge of balancing multiple design variables, researchers have increasingly employed the Taguchi DoE method to optimize FinFET geometry systematically. For instance, Karimi et al. [12] emphasized that at 32 nm nodes, SCEs can be effectively mitigated via precise dimensional tuning. It has been confirmed that aggressive WFIN scaling significantly influences SS and DIBL [16]. Meanwhile, Vijaya and Lorenzo [17] asserted that WFIN has the greatest impact on ION/IOFF, as well as on HFIN and LG. Similarly, Ansari et al. [18] applied the Taguchi method to a 22 nm TG FinFET. They achieved low leakage (10^{-10} A) and excellent SS of around 60 mV/decade and 78.1 mV/decade, respectively, with optimized geometries. Further studies on 7 nm strained Germanium FinFETs [19] and 16 nm DG-FinFETs [20] confirmed that orthogonal arrays such as L25 can yield designs with high ION/IOFF ratios. Notably, the ION and IOFF values of 1726.88 μA/μm and 503.41 pA/μm, respectively, meet the ITRS predictions. At the same time, Afifah Maheran et al. [21] reported 18 nm Double Gate MOSFETs, confirming their applicability to high-k gate material such as a gate structure made of Titanium Dioxide (TiO_2). However, despite these advancements, a research gap persists. Additionally, there is limited work that applies the Taguchi method for multi-variable optimization followed by circuit-level validation using predictive models.

To evaluate the circuit-level impact of optimized FinFET designs, researchers commonly implement the electrical parameters obtained from Taguchi-based optimization into HSPICE simulations using Predictive Technology Models (PTM). The Taguchi method, widely used for optimizing device-level parameters such as VTH, SS, DIBL, and ION/IOFF, enables the identification of optimal combinations of geometrical variables such as gate LG, WFIN, and HFIN [22], [23], [24]. Once optimized via TCAD simulations, these parameters are used in PTM FinFET libraries, which are freely available in HSPICE for technology nodes such as 7 nm, 10 nm, and 14 nm. This approach allows researchers to simulate fundamental logic circuits, such as inverters and gates, and evaluate key performance metrics, including delay and power dissipation. In previous work, a 16 nm DG-FinFET was optimized using a Taguchi L25 orthogonal array, and the resulting optimized values were then imported into SPICE for circuit analysis [20]. Similarly, the results for delay and power dissipation were 0.685 ns and 2.35 μW, respectively, when a heterojunction P-type FinFET at the 14 nm node was implemented in HSPICE using PTM models [25]. Another comparative study, employing optimal geometries with PTM FinFET models at 14 nm and 22 nm, demonstrated significant improvements in delay and energy efficiency [26].

3. METHODOLOGY

Figure 1 shows the flowchart of the project's technique. First, it will design FinFET technology based on the factors that will be used. Progressing technology involves evaluating the device's attributes, capabilities, performance, and other areas. Subsequently, all collected research data will be optimized and utilized by the TCAD simulation. The process begins with the design of a FinFET structure by selecting critical geometrical factors such as gate LG, WFIN, and HFIN. These dimensions—such as electrostatic control and current-driving capability—were selected because they are known to influence device performance. The electrical properties of the device, including VTH, ION/IOFF ratio, SS, and DIBL, are then evaluated through TCAD simulations. We analyze performance and examine the effects of reducing specific geometric parameters using simulation results. The research aims to determine the optimum dimensional structure for FinFET performance under a 7 nm technology node. Therefore, using this data, the settings that yield the device's best performance characteristics can be identified.

3.1 Silvaco TCAD

The research was conducted using simulation in the Silvaco TCAD software. The source and drain lengths (LS/LD) and gate LGs in nanometers are the parameters utilized in the FinFETs. WFIN is the width, and HFIN is the height of the vertical silicon fin. The source and drain areas are doped with a donor concentration of 1.20×10^{21} cm^{-3}, whereas the channel is evenly doped with acceptor dopant of 1.45×10^{18} cm^{-3} [23], [24]. Figure 1 shows the flowchart of the Silvaco TCAD simulation. The 3D structure of the FinFETs employed in this work is illustrated in Figure 2. It emphasizes the device's functional areas and structural aspects. The source and drain terminals serve as charge injection and collection points, respectively, and are situated on opposite ends of the fin. The channel formed beneath the fin is controlled by the gate positioned above it. The channel length (LG), which defines the separation between the source and drain beneath the gate, is one of three essential geometrical features. The fin height (HFIN) represents the vertical dimension of the silicon fin, while the fin width (WFIN) corresponds to the lateral thickness of the fin [23], [24]. The parameters LG, HFIN, and WFIN influence the electrical characteristics of the FinFET, including VTH tuning, current driving performance, and suppression of short-channel effects (SCEs). Additionally, Figure 2 exhibits the effect of geometric scaling on the electrostatic performance and reliability of modern FinFET devices.

The simulation employed a 2D Schrödinger-Poisson model, and the quantization inside the channel is nearly two-dimensional. Equations 1 and 2 are used in the simulation to extract the values of SS and DIBL, respectively [5].

The SS and DIBL are key parameters for evaluating SCEs in FinFET devices. Equation 1 defines the SS as the inverse slope of the logarithmic Drain Current (IDS) versus VGS curve in the subthreshold region:

$$SS = \frac{dV_{GS}}{d(log_{10}I_{DS})}, \quad (1)$$

where VGS is the Gate-Source Voltage (in volts), and IDS is the Drain Current (in amperes). A lower SS indicates better switching behavior and improved energy efficiency.

Meanwhile, Equation 2 defines DIBL as the change in ΔVTH with respect to a change in ΔVDS:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}}, \quad (2)$$

where VTH is the Threshold Voltage, and VDS is the Drain-Source Voltage (in volts). Higher DIBL values indicate the influence of drain voltage on VTH. Ideally, only the voltage that would affect the barrier. However, as the channel becomes shorter, a higher VD widens the drain depletion and reduces the potential barrier.

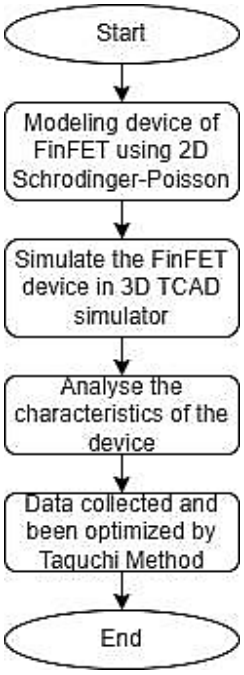

Figure 1. Flowchart of Silvaco TCAD simulati

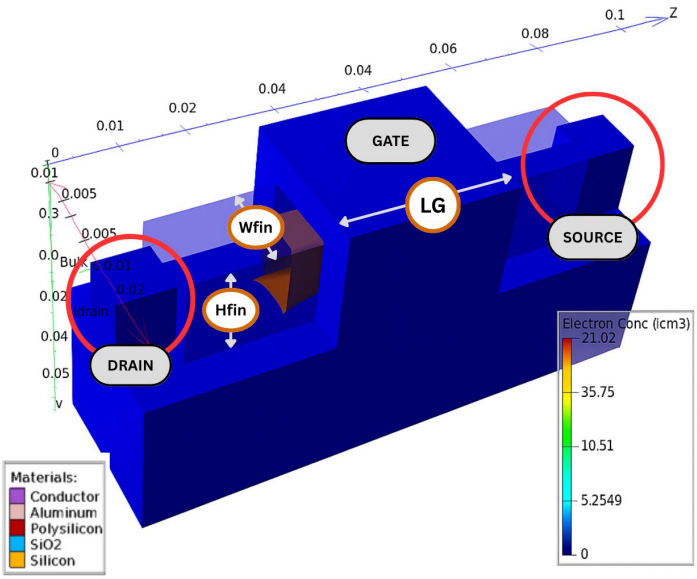

Figure 2. 3D structure of the FinFETs from the Silvaco TCAD Simulation.

3.2 Taguchi Method

The Taguchi method is one of several statistical strategies that are highly beneficial for addressing complex problems with the fewest variables and tests [27]. The Taguchi approach seeks to identify the parameters or factors that have a substantial impact on performance. Hence, it employs orthogonal arrays to vary simulation parameters and analyze their influence on target performance metrics. In this study, the Taguchi method was used to optimize the FinFET device geometry by exploring the impact of three key factors, such as channel LG, WFIN, and HFIN, on VTH, ION/IOFF ratio, SS, and DIBL.

To study the effects of each parameter variation. Table 1 summarizes the three-level DoE, with each factor assigned levels 0, 1, and 2. The L27 orthogonal array (3^3 design) was selected to balance design comprehensiveness with computational efficiency. Note that each simulation scenario corresponds to one combination of parameter levels [24].

Table 1 Factors and levels used in the parameters

Symbol	Factors	Level		
		0	1	2
A	Channel Length	10	13	15
B	Fin Width	5	7	10
C	Fin Height	30	35	40

The parameters that have been varied are outlined in Table 1, which includes LG, WFIN, and HFIN, assigned as A, B, and C, respectively. These factors are set at three levels each, where '0' represents the lowest value and '2' the highest. Meanwhile, the responses or desired output measures are VTH, ION/IOFF, SS, and DIBL, using the Smaller The Better (STB), Larger The Better (LTB), and Nominal The Better (NTB), respectively [24].

The three-level standard orthogonal arrays used in this work are L27(33) [24]. In this work, the factor level is varied based on previous work in which researchers have optimized the FinFET [23], [28]. Additionally, all design parameters and electrical characteristics of the structure were calibrated in accordance with ITRS guidelines.

3.3 Synopsis HSPICE

The FinFET library from PTM is utilized in this work. These predictive files were selected because they are compatible with the HSPICE simulator and can account for a wide range of process changes. Following that, a simulation will be run using Taguchi method data, with the primary goal of optimizing both delay and power consumption in the circuit. In line with this, inverter circuits are used in this work to study delay and power consumption. Figure 3 displays the flowchart of the simulation on HSPICE.

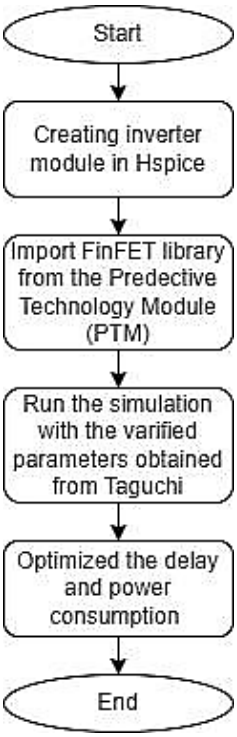

Figure 3. Flowchart of simulation on HSPICE.

4. RESULTS AND DISCUSSION

In this section, the effect of variations in WFIN, LG, and HFIN on the electrical characteristics of devices is discussed. The objective of this paper is to optimize VTH, ION/IOFF, SS, and DIBL using the DoE based on the WFIN, LG, and HFIN. Concurrently, the VTH, ION/IOFF, SS, and DIBL performances of the FinFET are statistically analyzed using the Taguchi method. If the device aims for a higher ION/IOFF ratio, the LTB characteristic is used to perform the DoE. In terms of IOFF performance, the device requires low subthreshold leakage by leveraging the STB characteristics. Meanwhile, in terms of VTH, the STB characteristic is used, as low-threshold devices exhibit greater sensitivity to structural variations (LG, WFIN, HFIN), making them more effective for analyzing threshold voltage shifts [29], [30], [31].

4.1 Effects of Physical Parameters Variation on V_{TH}, I_{ON}/I_{OFF} RATIO, SS, and DIBL

For FinFET devices, the VTHs can be adjusted by using various gate materials, whose work functions may play a crucial role in controlling VTH values [8]. The VTH is nominal at all points, suggesting that none of the parameter combinations make a significant difference. The VTH of FinFETs is primarily influenced by gate LG, WFIN, and HFIN, while the gate material work function can also play a role in other studies. In this work, the gate material is held constant, and variations in VTH are analyzed as a function of geometric parameters. The results show that VTH remains stable across most parameter combinations, indicating that the selected range of geometrical variations has a limited impact on threshold modulation. This suggests that at the 7 nm node, fin geometry affects other performance metrics, such as ION/IOFF, SS, and DIBL, rather than VTH itself. The VTH was determined using the constant-current procedure, defined as the Vg at which IDS reaches 10^{-7} A/μm, with a drain bias of VDS = 0.7 V. This approach enables assessment across device geometries.

The proposed 7 nm device has a higher ION/IOFF ratio that is satisfactory for any electrical device [22]. A higher HFIN can lead to a higher ION/IOFF ratio. Hence, in terms of the ION/IOFF ratio, the proposed device has a higher value, resulting in significantly better performance than the older MOSFET. Based on existing technology, the proposed 7 nm device operates with minimal leakage and drive current, achieving a better ION/IOFF ratio. Furthermore, when the channel LG is reduced, the SS can exhibit greater immunity to SCEs. Figure 4(C) illustrates the SS roll-up versus the channel LG for different WFIN.

In comparison, the smaller width is 5 nm, allowing for more SS to roll up. The main reason is that the narrower width can induce a shorter-scaling LG, which results in less degradation of subthreshold behavior than the wider one [32]. As the LG is narrowed to 10 nm, the DIBL effect becomes more pronounced. However, despite the trend of DIBL in short-channel devices, where channel widths are clearly increasing, this trend is not consistent. This phenomenon may be due to the etch bias not being easily controlled [33]. As the channel width increases, the DIBL increases due to the improved uniformity of VTH implantation. As the channel LG increases, the DIBL value also increases. The cause is like the statement made during the DIBL discussion. The internal electric field due to the LG reduces the impact of the punch-through effect [33], [34].

As shown in Figure 4(a), the VTH extracted using the constant-current method (ID = 10^{-7} A/μm at VDS = 0.7 V) exhibits minimal variation across different geometrical configurations. For instance, VTH increases marginally from 0.7452 V to 0.7487 V as the gate LG increases from 6 nm to 10 nm. Similarly, as HFIN increases from 30 nm to 40 nm, VTH rises slightly from 0.7444 V to 0.7471 V. In contrast, variations in WFIN from 4 nm to 10 nm cause a smaller change, ranging from 0.7482 V to 0.7488 V. Previous work [22], which suggests that gate-induced control enhances with longer channels and taller fins but alterations in WFIN have a considerably lesser effect, validates these findings. In general, the VTH remains consistent across all studied geometries, suggesting that enhancing ION/IOFF ratios and SS, rather than VTH, may be more beneficial for device optimization at the 7 nm node.

Figure 4(b) demonstrates how both WFIN and HFIN exhibit an influence on the ION/IOFF ratio. The ratio increases from 144,000 to 224,000 as WFIN grows from 5 nm to 10 nm. Similarly, the ratio increases from 261,240 to 263,760 when HFIN increases from 30 to 40 nm. On the other hand, the ratio decreases from 235,000 to 128,000 as the gate LG is reduced from 15 nm to 10 nm, indicating an increase in edge current. These findings follow trends showing that a larger fin enhances current drive, while a shorter LG degrades IOFF. Thus, choosing geometry tuning is essential for

achieving an optimal balance between performance and leakage in nanoscale FinFETs.

From Figure 4(c), it is observed that SS decreases with narrower fins and increases with longer gate LGs and taller fins. Specifically, as WFIN increases from 5 nm to 10 nm, SS decreases from approximately 72.0 mV/dec to 69.5 mV/dec, while increasing HFIN from 30 nm to 40 nm at LG = 12 nm, WFIN = 5 nm, where there is SS degradation from 68.3 mV/dec to 75.6 mV/dec. Furthermore, as LG increases from 10 nm to 15 nm at WFIN = 5 nm and HFIN = 40 nm, the rease increases from 68.4 mV/dec to 79.8 mV/dec. It should be noted that the SS values differ slightly between the WFIN sweep (72.0 mV/dec at WFIN = 5 nm, LG = 13 nm, HFIN = 40 nm) and the LG sweep (79.8 mV/dec at WFIN = 5 nm, LG = 13 nm, HFIN = 40 nm). This discrepancy occurs because the values were extracted under different parameter sweeps. These results align with earlier TCAD-based studies, which suggest that fin narrowing reduces the scaling LG, thus improving electrostatic control and short-channel [24], [30].

As presented in Figure 4(d), DIBL is highly sensitive to both LG and WFIN. A reduction in LG from 15 nm to 10 nm significantly increases DIBL from approximately 240 mV/V to 470 mV/V, reflecting severe SCEs at smaller gate LGs. Similarly, a narrower WFIN of 4 nm yields a much higher DIBL of approximately 440 mV/V; however, increasing WFIN from 7 nm to 10 nm raises DIBL from 215 mV/V to 280 mV/V. This points to increasing charge sharing and reduced gate control. The DIBL improves with HFIN, from 230 mV/V at 30 nm to 370 mV/V at 35 nm, then drops to 260 mV/V at 40 nm. This non-linear trend suggests a significant trade-off between vertical electrostatics and drive current capacity. These results are consistent with prior TCAD-based studies [34], underscoring the importance of coordinating FinFET geometries to reduce SCEs while maintaining high performance.

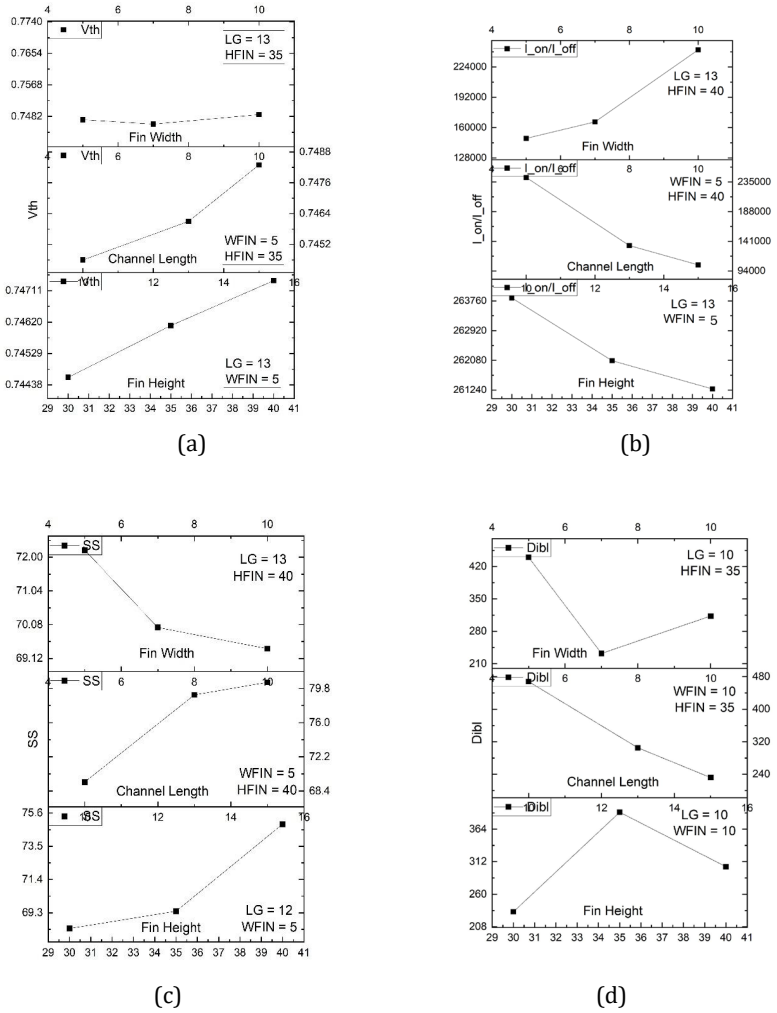

Figure 4. Effect of a) VTH, b) ION/IOFF, c) SS, and d) DIBL on different L_G, W_{FIN}, and H_{FIN}.

4.2 Optimization of VTH, ION/IOFF RATIO, SS, and DIBL

The effects of geometry scaling on VTH are shown in Figure 4(a), where optimizing VTH leads to a decrease. The combination of the observed geometry indicates that LG is 13 nm, WFIN is 7 nm, and HFIN is 35 nm. The VTH is 0.7461 V, which causes the source-drain regions to be very close to each other, reducing the current controlled by the gate. Some of the charges allow flow between the source and the drain in the channel, hence lowering the VTH. However, further reduction of the parameter decreases the device's stability, which likely indicates that SCEs are worsening. Moreover, Figure 4(b) shows the SNR for the three factors in the ION/IOFF characteristics. As the device shrinks, the ION/IOFF exhibits significant improvements with the Taguchi-derived combination, with ratios mostly up to 10^6. Notably, the combination to achieve the optimum ratio is LG is 13 nm, WFIN is 5 nm, and HFIN is 40 nm. The rising ION/IOFF drops drastically at Lg around 15 nm, indicating the relative increase in IOFF is substantial compared to the slight rise in ION. This observation is crucial, as it demonstrates how the combinations parameter can affect FinFET performance.

Furthermore, reducing parameters has yielded a higher ION/IOFF ratio. When the ratio increases, it indicates that the device is becoming faster and reducing the leakage current. The figure and table below illustrate the effect of each factor on the current ratio. It represents the optimal combination based on SNR. Correspondingly, from Figure 4(c), it can be observed that the SS performs better when the parameters are LG = 13 nm, WFIN = 5 nm, and HFIN = 40 nm. It yields an SS result of approximately 72 mV/dec, resulting in low power, as lower SS reduces the power. Fundamentally reducing the voltage to achieve the desired on-off switch [34]. The SS obtained in this analysis provides a rough qualitative indication of the reduction in SCE of a short transistor [11]. Lastly, as shown in Figure 4(d), DIBL reduces the FinFET barrier height under drain voltage. Note that DIBL must be less than the specified value to ensure the device can enter an off state. The higher the value, the greater the chance that a device failed to enter the off condition. DIBL on FinFET depends on WFIN. The channel LG must be greater than or equal to WFIN to suppress DIBL [33] effectively. Based on the results, it suggests that the combination of parameters LG is 10 nm, WFIN is 10 nm, and HFIN is 35 nm has yielded an effective DIBL of approximately 390 mV/V.

The optimization of FinFET electrical characteristics was conducted using Signal-to-Noise Ratio (SNR) analysis based on the Taguchi method, as illustrated in Figures 5(a–d). This analysis shows the impact of three essential geometric features on VTH, the ION/IOFF ratio, SS, and DIBL: channel LG, WFIN, and HFIN. The x-axis indicates the discrete levels of each geometrical parameter in these figures, and the mean SNR value for each performance metric is shown on the y-axis. The optimal geometry combinations for increased FinFET reliability and overall performance were thus determined by a higher SNR, which reduced device performance variability.

For VTH, Figure 5(a) shows consistent VTH performance at LG = 10 nm, WFIN = 10 nm, and HFIN = 30 nm, which is the optimum geometric design based on the highest SNR. Based on the SNR trend, larger fins enhance electrostatic integrity, while shorter channel LGs improve gate control and minimize variability. Furthermore, increasing HFIN to 30 nm reduces SNR due to increased SCEs; therefore, 30 nm is the optimal HFIN for VTH stability. Using Silvaco ATLAS simulation employing the constant current procedure at ID = 1 nA, the generated VTH for the optimum design (LG = 10 nm, WFIN = 10 nm, HFIN = 30 nm) was 0.7461 V. The high channel doping concentration (1E18 cm^{-3}), a gate work function of 4.85 eV, and the quantum confinement effects modeled using the BQP model are a few of the factors contributing to this value being higher than the standard VTH. These parameters were set to study geometric effects. For accurate VTH tuning, however, further calibration with a particular value would be performed.

The SNR evaluation of the ION/IOFF ratio as a function of geometric parameters is shown in Figure 5(b). The extracted ION/IOFF ratio reached 262,072 at LG = 15 nm, WFIN = 5 nm, and HFIN = 40 nm, yielding the best performance. The combination of a longer gate LG with a thin fin and tall HFIN is influenced by this optimum design. For instance, the enlarged HFIN increases the conducting volume, boosting drive current (ION), while the narrow WFIN optimizes electrostatic control, lowering leakage current (IOFF). The longer channel enhances the overall reliability of the current ratio by reducing the SCEs.

As WFIN decreases and HFIN increases, SS performance improves, enhancing electrostatic control (Figure 5(c)). At LG = 15 nm, WFIN = 5 nm, and HFIN = 40 nm, the most ol configuration, based on its highest SNR, was determined, where with ating SS reacheof/dec. Taller fins improve gate-to-channel coupling, while smaller fins reduce the electrostatic scaling factor LG, thereby enhancing gate control. By reducing leakage, those improvements contribute to superior switching characteristics and decreased power consumption. The energy-efficient design of nanoscale transistors is further enhanced by lower SS, which allows operation at lower supply voltages [34]. The reduction of SCEs, which is essential to sustaining performance in short-gate devices, results in improved hisinudy.

The optimum configuration was established at LG = 15 nm, WFIN = 5 nm, and HFIN = 40 nm, with a DIBL of 390 mV/V, as shown in Figure 5(d). Therefore, a longer gate LG effectively suppresses barrier lowering via enhancing electrostatic separation between the source and drain. In addition, by decreasing charge sharing from the drain, the smaller WFIN improves lateral gate control. In addition, increasing HFIN to 40 nm enhances the vertical gate's influence, thereby reducing SCEs and improving DIBL performance.

4.3 Pareto Analysis of Variance (ANOVA)

Analysis of Variance (ANOVA) was employed to investigate further the impact of each geometrical parameter on each device's performance and to verify the findings. Figure 6 shows the Pareto diagram of designs targeting VTH, ION/IOFF, SS, and DIBL performance for the FinFET. It is observed that interaction occurs across all parameters and characteristics. The interaction is classified as (A×B), (A×C), and (B×C). The STB analysis was selected for the optimal VTH, a justified choice. Following the next characteristic, the current ratio, the interaction shows that the LTB analysis produced the same result as Taguchi. Furthermore, the SS and DIBL values determined by NTB analysis are supported by the interaction depicted in Figures 5(a) and 5(d). Based on the results, it is verified that every combination yields the optimal result among the interactions.

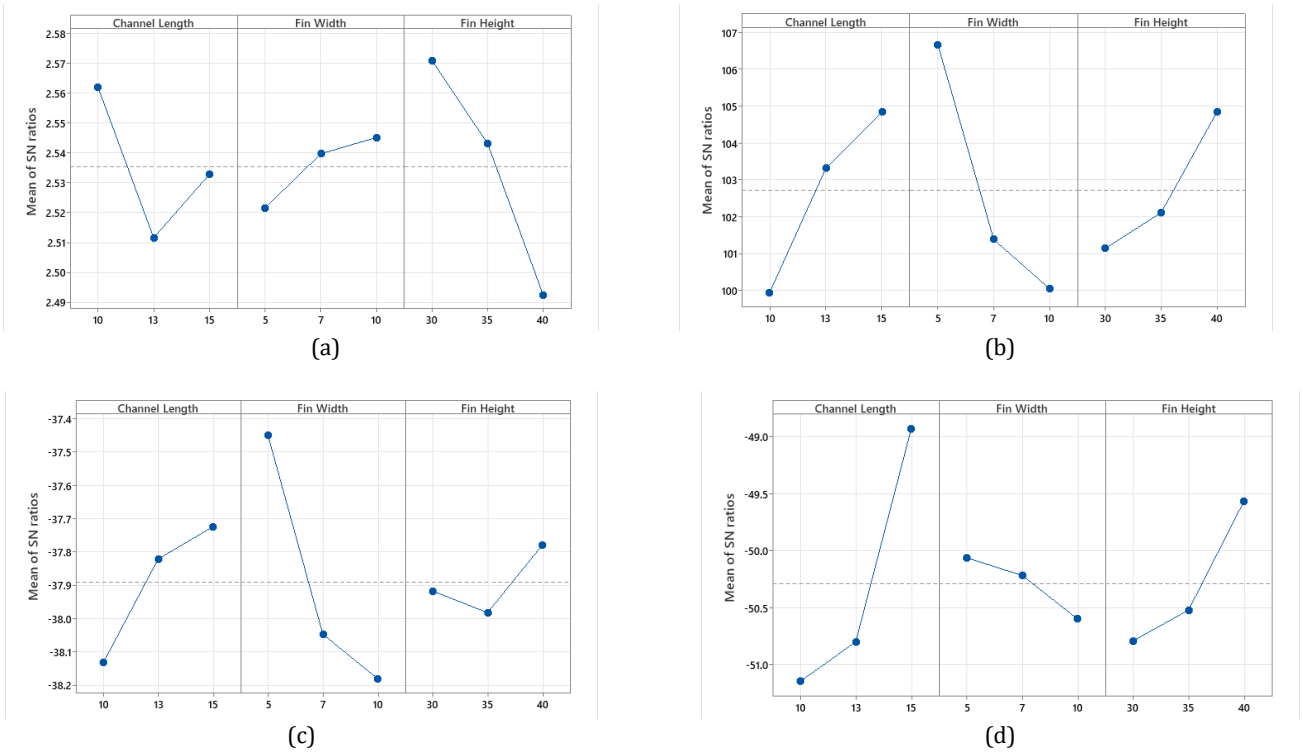

Figure 5. Average SNR against factor level for a)VTH b)ION/IOFF c)SS d)DIBL on channel length, fin width, and fin height.

Figure 6(a) illustrates the interaction effects of channel LG, WFIN, and HFIN on the VTH. The top-left interaction plot between LG and WFIN indicates that VTH increases with channel LG, with the highest value of 0.752 V observed at LG = 13 nm and WFIN = 5 nm. This implies that by suppressing SCEs and improving gate modulation, an acceptable channel LG and a narrow WFIN enhance electrostatic control. Larger fins (HFIN = 40 nm) lead to higher VTH at LG = 13 nm, based on the bottom-left interaction plot between LG and HFIN. The vertical gate coupling in controlling channel potential is emphasized. On the other hand, the bottom-right relationship between WFIN and HFIN demonstrates that while both taller fins (HFIN = 40 nm) and narrower fins (WFIN = 5 nm) improve VTH, their combined effect does not yield a linear gain, indicating a saturation effect or physical scaling limitations. This nonlinearity indicates that, to avoid a performance decrease, robust vertical and lateral scaling must be appropriately balanced.

The interaction charts for ION/IOFF ratios for various channel LG, WFIN, and HFIN configurations are illustrated in Figure 6(b). The greatest ION/IOFF ratio, approximately 357,143, can be observed in the top-left plot (LG × WFIN) at LG = 13 nm and WFIN = 5 nm. It demonstrates that a narrow WFIN with a modest gate LG improved the current drive while decreasing leakage. The current ratio increases, and off-state leakage decreases with narrower fins, thereby further enhancing electrostatic integrity and gate control. Conversely, when HFIN = 40 nm is paired with LG = 13 nm in the bottom-left plot (LG × HFIN), the ION/IOFF ratio increases, indicating that vertical gate control can enhance device efficiency. To increase ION while preserving low IOFF, larger fins provide a larger effective channel. The largest value at WFIN = 5 nm and HFIN = 40 nm in the bottom-right plot (WFIN × HFIN) suggests that this combination yields the best ION/IOFF performance. Nonetheless, the trend shows deterioration when WFIN exceeds 5 nm, even at increasing HFIN values. The research suggests that the best design to improve the ION/IOFF ratio is achieved with LG = 13 nm, WFIN = 5 nm, and HFIN = 40 nm. Figure 5(b) exhibits the trade-off between vertical scaling and narrow-fin in reducing leakage while elevating current and confirms the preceding SNR results.

The SS can be observed in Figure 6(c), where lower values lead to low-power operation and switching characteristics. The interaction plots demonstrate that at LG = 13 nm, WFIN = 5 nm, and HFIN = 40 nm, the lowest SS, around 72–73 mV/dec, is established. Narrow fins increase electrostatic gate control, which reduces SCEs, based on the channel LG × WFIN interaction. Similarly, the channel LG × HFIN interaction indicates that increasing HFIN enhances vertical

gate coupling, thereby reducing subthreshold leakage. Hence, the optimum combination of a high HFIN and a narrow WFIN leads to the best SS performance, as demonstrated by the WFIN × HFIN interaction.

The DIBL interaction graphs are shown in Figure 6(d), with lower values indicating suppression of SCE control. The DIBL reduces as LG increases in the channel LG × WFIN interaction, exhibiting the lowest values at LG = 15 nm and WFIN = 10 nm. The observed trend suggests that the drain impact on the channel barrier reduces as gate LG increases. Conversely, the channel LG × HFIN interaction indicates that fins with HFIN = 40 nm strengthen electrostatic control, particularly at longer channel LG, leading to a decline in DIBL. In the WFIN × HFIN plot, the minimum DIBL is observed at WFIN = 5 nm, HFIN = 40 m w ich wherearrow and tall fins effectively suppress both lateral and vertical electrostatic coupling from the drain. Overall, the optimal DIBL performance is achieved with LG = 15 nm, WFIN = 5 nm, and HFIN = 40 nm. Notably, DIBL is reduced to approximately 232 mV/V, highlighting improved SCE immunity in aggressively scaled FinFETs.

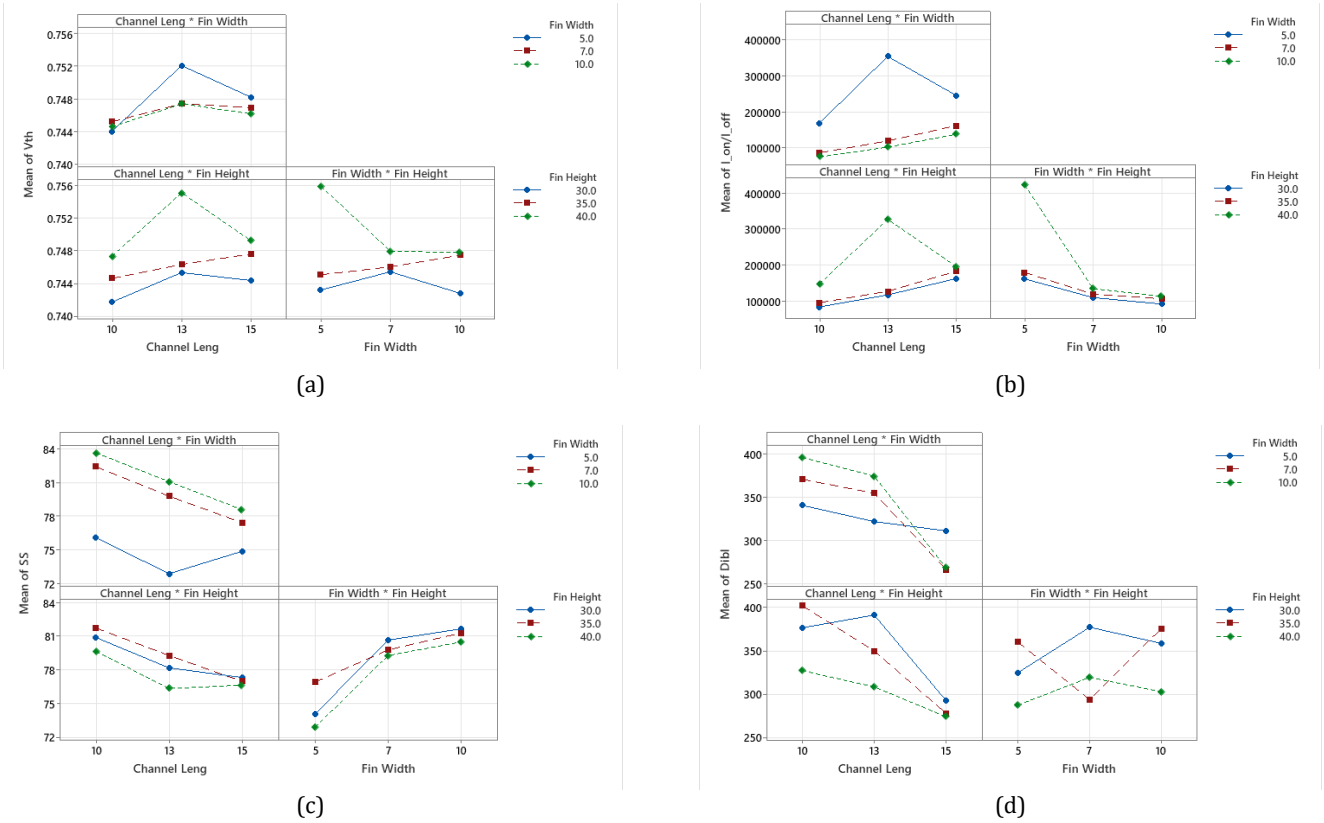

Figure 6. Average SNR against factor level for a) VTH b) ION/IOFF c) SS, and d) DIBL on channel length, fin width, and fin height.

4.4 Implementation of Inverter Performance for Circuit-Level Optimization

Table 2 demonstrates that this combination parameter improves the power of this work at the nanoscale compared to others. The VTH optimization achieved combinations, resulting in a 46.9% improvement, reducing the time from 1.90E-08 s to 1.01E-08 s. This includes a 93.8% reduction in power consumption from 9.833E-11 W to 6.13E-12 W, compared to the default PTM setup. In this study, 33 geometry combinations were evaluated, comprising 27 primary configurations generated from the Taguchi DoE (with three levels for each of the three parameters: LG, WFIN, and HFIN), along with six additional validation runs to fine-tune the optimal conditions. These improvements are due to the low voltage used to reduce power consumption. In addition, it has been established that the smaller the device, the lower the voltage that can be employed for low-power applications. The delay can be compared between the default settings, and it is observed that the delay is improved in this work. The default setting refers to the inFET configuration provided by the official PTM library, which serves as a widely used industry baseline.

The improvements in optimized electrostatics and better control of SCEs in the new configurations. Reducing and increasing HFIN results in increased current (ION) and reduced leakage current (IOFF), resulting in improved delay and power characteristics. Additionally, the refined device geometries enable operation at low voltages, further reducing leakage power in the inverter circuit. These findings support the effectiveness of the proposed device-level optimization in enhancing energy efficiency and circuit-level speed [35].

Table 2 Power and delay for each optimization combination

Type	Delay (s)	Power (W)
This Work	1.01E-08	6.13E-12
Default	1.900E-08	9.833E-11
Paper 1[36]	-	3.989E-9
Paper 2[37]	-	2.807383E-9

5. CONCLUSION

In this study, the influence of geometric scaling and process parameters on the performance of Finmined is examined, with specific key performance indicators. This includes VTH, current ratio, SS, and DIBL. FinFET performance is improved by reducing geometric dimensions and optimizing process parameters for low-power applications. The findings show a reduction in SCE and an improvement in on-current while maintaining a low off-current. The results of VTHforSS and DIBL also indicate device stability and performance, confirming the effectiveness of these parameter changes for achieving low-power, high-performance FinFETs. By varying the gate LG, WFIN, and HFIN, we evaluated their impact on electrical parameters, including the ION/IOFF ratio, SS, and DIBL—the optimal configuration for VTH. The VTH of 0.7461V was caused by the source-drain regions being very close to each other, to the point that the current controlled by the gate is reduced, as noted at LG = 13 nm, WFIN = 7 nm, HFIN = 35 nm, yielding a VTH of 0.7461V. The best ION/IOFF ratio of 262.072 and an SS of 72 mV/dec were achieved with narrower fins and taller channels at LG = 13 nm, WFIN = 5 nm, and HFIN = 40 nm. For effective DIBL suppression, the optimal geometry was LG = 10 nm, WFIN = 10 nm, HFIN = 35 nm, resulting in a DIBL of approximately 232 mV/V. The Taguchi approach was then employed to optimize the FinFET model to increase current and improve transistor performance while reducing current. With the Taguchi approach, the design space was effectively explored, and an ideal set of parameters was developed. The chosen parameter combination, involving VTH, DIBL, SS, and ION/IO, the FF ratio, is the most effective at achieving the expected performance targets, based on the NR analysis. Despite varying overall performance metrics, this optimization procedure demonstrated robustness and dependability—the Taguchi method for semiconductor device optimization. Using optimized FinFET characteristics in a logic circuit, especially an inverter circuit, PICE yielded considerable gains in circuit performance. The optimized inverter demonstrated lower power consumption and smaller delay, making it ideal for low-power applications.

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