International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

Performance evaluation of novel mid-insulation gate junctionless transistors at the device and circuit level

Sonali Keithellakpam [a], Papu Doley [a], and Nipanka Bora [a]*

[a]*North Eastern Hill University (A Central University), Shillong-793022, India*
∗Corresponding author. Tel.: +91-0364 2307930-3673; e-mail: nbora@nehu.ac.in

Received 24 September 2025, Revised 31 January 2026, Accepted 4 February 2026

ABSTRACT

This work proposes a novel gate-engineered Mid-Insulation Gate Junctionless Transistor (MiG-JLT) and presents a comparative performance evaluation against the conventional Symmetric Double Gate Junctionless Transistor (SDG-JLT). Under identical physical parameters, the proposed MiG-JLT demonstrates a nearly 35% enhancement in ON-state current, achieving an ON current of approximately 2.5×10^{-5} A and an I_{ON}/I_{OFF} ratio of about 2.5×10^{8}. For a silicon body thickness of 10 nm, the device exhibits a peak transconductance of $\sim 7 \times 10^{-5}$ S, and a drain conductance of $\sim 1.3 \times 10^{-4}$ S at low drain bias, confirming its improved analog performance. The effects of doping concentration, surface potential distribution, and channel width are systematically analyzed. Circuit-level inverter analysis further demonstrates enhanced transfer and switching characteristics. Overall, the proposed MiG-JLT shows strong potential for high-performance nanoscale and SPICE-compatible device applications.

Keywords: *Mid-insulation gate, Junctionless transistor, Surface potential, Drain current, Transconductance*

1. INTRODUCTION

The concept of Moore's law has been ruling the semiconductor industry for several decades, driving continuous scaling of devices into the nanometer regime. To align with this trend, the dimensions of the metal-oxide-semiconductor field-effect transistor (MOSFET) have been progressively reduced. However, further dimensional scaling significantly alters the conventional behaviour of MOSFETs. To establish source-channel and channel-drain junctions, an ultra-sharp doping profile is required, typically achieved through rapid thermal annealing, which increases fabrication complexity and cost per function [1]. At nanoscale dimensions, leakage current and short-channel effects (SCEs) [2, 3] severely degrade device performance, ultimately limiting MOSFET scalability. To address these challenges, researchers have explored advanced multi-gate architectures such as tunnelling field effect transistors (TFETs) [4, 5], FinFETs [6, 7], and gate-all-around (GAA) MOSFETs [8, 9]. While TFETs suffer from low ON-state current and large subthreshold swing (SS), making them incompatible for high-performance circuits despite their high energy efficiency, FinFET and GAA MOSFETs, although effective in mitigating SCEs, and enhancing electrostatic control, remain inversion-mode devices and therefore exhibit non-negligible leakage currents and complex fabrication processes.

In 2010, J.P. Colinge *et al.* [10] introduced a novel transistor architecture known as the Junctionless Transistor (JLT), which has gained considerable attention in very large-scale integration (VLSI) design. Unlike conventional MOSFETs, JLTs do not incorporate metallurgical junctions, thereby eliminating the need for complex doping concentration gradients. In this device, the source, channel, and drain are uniformly doped with the same doping polarity, and the conduction mechanism is governed by bulk current rather than surface potential, as in typical MOSFETs. JLTs exhibit several advantages, including a near-ideal subthreshold swing (60 mV/dec), reduced leakage current and mitigation of SCEs, and a simplified fabrication process. Multiple architectures of JLT have been reported in the literature [11–13]. However, because these devices are heavily doped to enhance current flow, they inherently suffer from leakage current, which degrades the I_{ON}/I_{OFF} ratio.

Lately, gate architectural engineering of junctionless transistor studies has been the focus. Ajay *et al.* [14] investigated the sensitivity of split-gate JLT for biosensing applications, while Sandeep Kumar *et al.* [15] developed a theoretical framework of a dielectric-modulated trench double-gate junctionless FET aimed at biosensing applications. Neha G. *et al.* [16] introduced a junctionless transistor featuring dielectric-separated independent gates, tailored for efficient implementation in digital logic circuits. Existing gate-engineered JLT models have primarily explored vertical gate splitting, which has been referred to in the literature as either parallel gated JLTs [17] or split gated JLTs [18]. In this work, a novel gate structure-engineered model of a junctionless transistor is modelled and studied with the help of extensive 3-D TCAD simulations. Furthermore, an inverter circuit is designed using the MiG-JLT structure to study its performance over the other available comparable structures.

2. DEVICE ARCHITECTURE

In this work, the three-dimensional configuration of the proposed MiG-JLT is depicted in Figure 1.

The core innovation in our proposed device design is the intentional creation of a neutral region by splitting the gate along the width (Z-axis) through the introduction of an insulating oxide layer. To ensure process compatibility and ease of fabrication, silicon dioxide (SiO_2), which already serves as the gate dielectric, is employed for the gate splitting. The silicon body of the device incorporates the source, channel, and drain regions, all of which are uniformly doped with a high donor concentration (N_D) to ensure efficient carrier transport. The device dimensions are defined with a channel length of 45 nm and a silicon body thickness of 10 nm. Since the body thickness is limited to 10 nm, quantum mechanical effects are not considered in this study [19]. An ultra-thin SiO_2 insulating layer of 1 nm is incorporated to maximize the drain current (I_D). The device employs dual-gate electrodes positioned on the top and bottom surfaces, both fabricated from p^+ polysilicon, and exhibiting a work function of 5.1 eV. These gates are simultaneously biased to maintain symmetric control over the channel. A fixed spacing of 10 nm is maintained between the mid-insulation gates on both the top and bottom to preserve electrostatic integrity and device performance.

Although this work is based solely on device simulation, the proposed MiG-JLT is compatible in principle with a standard CMOS process flow. In a practical implementation, the device could share the same substrate preparation, channel doping, gate-oxide growth, and gate-stack deposition steps used for conventional junctionless or planar CMOS transistors, so no exotic material or process modules are required [20]. The MiG configuration would then be formed using an additional lithography and etch step that selectively removes the gate electrode in the central region above the channel, thereby defining the mid-insulating segment while preserving the two outer gate sections. This localized patterning is analogous to well-established gate recess or cavity-etch steps reported for split-gate and cavity-engineered junctionless devices [21, 22], indicating that fabrication of the proposed structure is realistically achievable within existing CMOS technology. The physical parameters used are provided in Table 1.

Table 1. Physical parameters of the proposed device

Parameter	Symbol	Value
Channel length (nm)	L	45
Silicon thickness (nm)	t_{Si}	10
Oxide thickness (nm)	t_{ox}	1
Doping concentration (cm^{-3})	N_D	1.2×10^{19}
Work function (eV)	Φ_m	5.1
Spacing between the gates (nm)	d	10
Width of the device (nm)	W	50

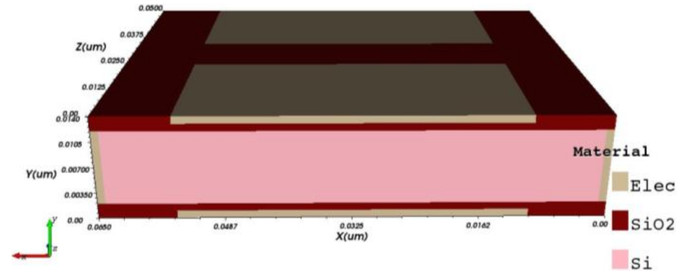

Figure 1. Proposed mid-insulation junctionless transistor

3. RESULTS AND DISCUSSION

This section presents the simulation results of the proposed MiG-JLT developed on silicon-on-insulator (SOI) technology. Device behaviour was investigated using the Synopsys Sentaurus TCAD device simulator, a widely adopted tool for semiconductor device modelling. The simulation framework incorporated considerations for prominent short-channel effects, including drain-induced barrier lowering (DIBL) and carrier trapping, to accurately reflect nanoscale device physics. Carrier transport was modelled using Fermi-Dirac carrier statistics with impact ionization accounted for, ensuring a precise representation of charge behaviours under various operating conditions. The Lombradi mobility model was implemented to account for the influence of doping levels as well as the transverse and longitudinal electric fields. To address leakage mechanisms, Shockley-Read-Hall (SRH) recombination was incorporated into the simulation framework. Quantum mechanical effects were deliberately omitted, as the silicon body thickness was restricted to 10 nm, in agreement with previously established findings [19].

Figure 2 shows the surface potential variation along the channel width (Z-axis) for different gate voltages (V_{GS}) while drain voltage (V_{DS}) is kept constant at 0.5 V, highlighting the core electrostatic behaviour investigated in this study. The surface potential is evaluated along the channel width at the longitudinal midpoint of the MiG-JLT. The extracted profiles display a pronounced maximum at the center of the channel, directly beneath the middle insulating region, and lower

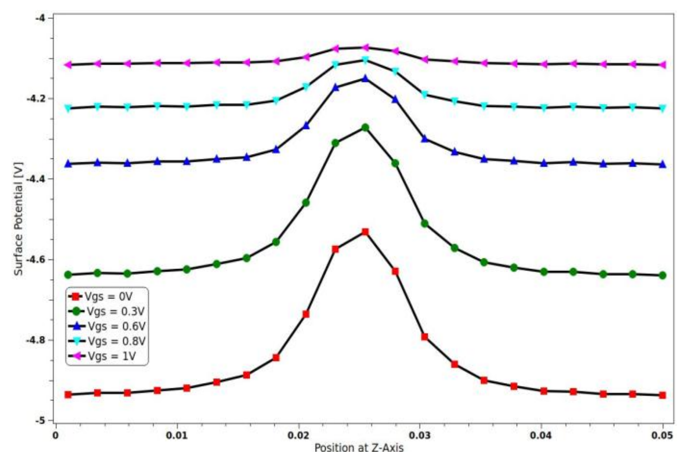

Figure 2. Surface potential curve along the position of the Z-axis (channel width) with varying V_{GS}

potential under the two gated segments. This non-uniformity originates from the lateral discontinuity in gate control: in the under-gate regions, the channel is strongly coupled to the metal through a thin gate dielectric, whereas in the central gap, the silicon is influenced only through fringing fields, which correspond gate-channel capacitance. Consequently, the gate-induced modulation of charge is weaker in the middle, and a higher local surface potential (electrostatic barrier) is required to satisfy charge balance in the uniformly doped junctionless channel, in agreement with quasi-2D Poisson-based models for split-gate and cavity-type junctionless FETs. As the gate bias increases, the entire profile shifts upward, and the curvature across the width progressively flattens, indicating that stronger gate fields enhance lateral coupling, reduce the central barrier, and drive the channel toward a more uniform conduction path, consistent with earlier analytical and simulation studies of split gate and cavity-engineered JL structures [23].

3.1. Analytical Electrostatic Model

To analytically investigate the electrostatic behaviour of the proposed MiG-JLT, the device is assumed to operate in the junctionless regime, with a uniform n-type doping concentration throughout the source, channel, and drain regions. As the silicon body thickness is limited to 10 nm, it allows the use of a quasi-two-dimensional electrostatic approximation and neglects the QME [19]. In addition, the introduction of the mid-insulation layer creates a lateral discontinuity in gate electrostatic control along the channel width (z-direction), resulting in a non-uniform effective gate capacitance that plays a key role in forming the surface potential and electric field distribution of the proposed device. The quasi-two-dimensional Poisson equation:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,z)}{\partial z^2}=\frac{qN_D}{\varepsilon_{Si}} \tag{1}$$

where q is the charge carrier, ε_{Si} is the dielectric constant of silicon.

In the gate-controlled regions, the silicon-oxide interface boundary condition is expressed as:

$$-\varepsilon_{Si}\frac{\partial\phi}{\partial n}|_{gate}=C_{ox}(V_{GS}-\phi_S) \tag{2}$$

where $C_{ox}=\varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area, ϕ_S is the surface potential under the gate.

In the mid-insulation region, electrostatic control is achieved through fringing electric fields, modelled using an effective fringing capacitance:

$$-\varepsilon_{Si}\frac{\partial\phi}{\partial n}|_{mid}=C_{fr}(V_{GS}-\phi_S), C_{fr}\ll C_{ox} \tag{3}$$

Solving the governing equation with the above boundary conditions yields the surface potential distribution along the channel width [25]:

$$\phi_S(z)=\phi_0+A\cosh\left(\frac{z}{\lambda}\right) \tag{4}$$

where the characteristic electrostatic length λ is defined as:

$$\lambda=\sqrt{\frac{\varepsilon_{Si}T_{Si}}{C_{eff}}} \tag{5}$$

$C_{eff}=C_{ox}$ in the gated regions and C_{fr} in the mid-insulation region.

Since $C_{fr}\ll C_{ox}$, the characteristic length λ becomes larger in the mid-insulation region, producing a local maximum in surface potential, as observed in TCAD simulations (Figure 2).

The lateral electric field along the channel width is obtained from the gradient of the surface potential:

$$E_z(z)=-\frac{d\phi_S(z)}{dz}=-\frac{A}{\lambda}\sinh\left(\frac{z}{\lambda}\right) \tag{6}$$

The reduced effective gate capacitance in the mid-insulation region results in a localized electrostatic barrier. As the V_{GS} increases, lateral coupling strengthens, reducing this barrier and leading to a more uniform conduction path, consistent with the simulated surface-potential and transfer characteristics. Figure 3 shows the calibration of our simulation setup with the help of fabrication data available from the S. Barraud *et al.* [24] results. Here, the I_D for the NMOS tri-gate junctionless transistor is evaluated by varying V_{GS} while keeping V_{DS} constant at both low (V_{DS} = 0.04 V) and high (V_{DS} = 0.9 V) bias conditions. The simulations are performed with a doping concentration of 1.2 × 10^{19} cm^{-3} and a gate length of 13 nm. The inset labelled "Exp" refers to the experimental results reported by S. Barraud *et al.*, whereas "Sim" corresponds to the present simulation outcomes. During the calibration of the simulation setup, our simulation demonstrated good agreement with reported experimental data for a comparable tri-gate structure. Figure 4 presents the comparative I_D characteristics of the proposed MiG-JLT and the conventional SDG-JLT at different V_{GS}.

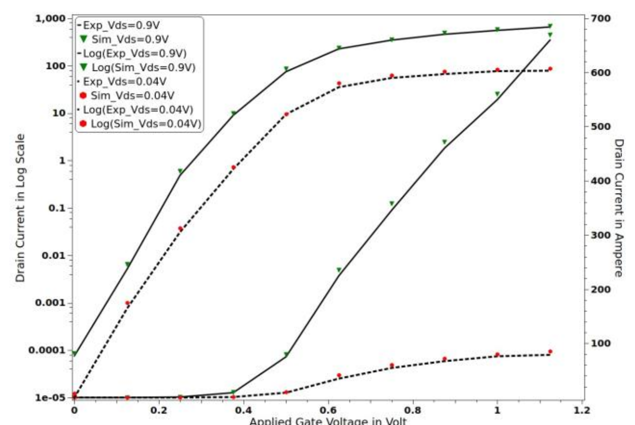

Figure 3. The calibration curve of I_D variation with V_{GS} at constant V_{DS} = 0.04 V, 0.9V

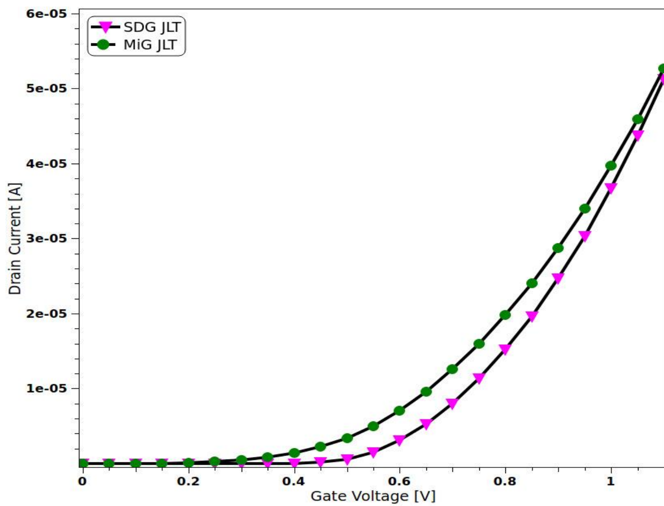

Figure 4. Comparison curve of I_D vs V_{GS} for SDG-JLT and MiG-JLTs in a linear scale

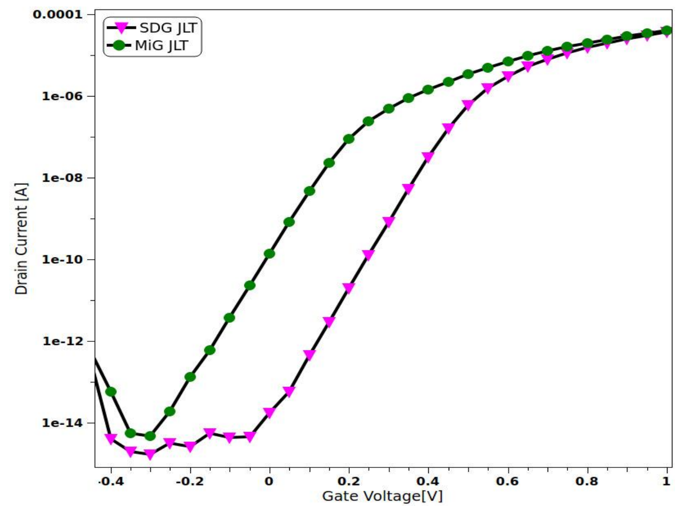

Figure 5. Comparison curve of I_D vs V_{GS} for SDG-JLT and MiG-JLTs in logarithmic scale

At $V_{GS} = 0.7$ V, it is observed that the MiG-JLT architecture exhibits an ON-state current approximately 35% higher compared to the conventional SDG-JLT. This improvement in I_{ON} current arises from the insertion of the gate insulator at the midpoint of the gate width along the channel. The introduction of this insulating layer alters the surface potential distribution, leading to a non-uniform profile by creating a higher potential in the central region beneath the mid-insulator. As a result of this effect, the channel conduction improves, yielding a higher I_{ON} compared to other structures. The same behaviour is illustrated on a logarithmic scale in Figure 5.

For the MiG-JLT device, the ON-state current at $V_{GS} = 0.7$ V is approximately 2.5×10^{-5} A, while the OFF-state current is around 1×10^{-13} A, yielding an I_{ON}/I_{OFF} ratio of roughly 2.5×10^{8}. Its leakage current characteristics closely match those of SDG-JLT, with only a marginal increase detected around $V_{GS} = -0.2$ V. As the V_{GS} is further reduced to about −0.5 V, the current shows a slight rise due to the gate-induced drain leakage (GIDL) effect. This behaviour can be attributed to band-to-band tunnelling near the drain-channel junction, where the high electric field facilitates carrier generation, thereby increasing the leakage current. Figure 6 shows the surface potential variation along the channel length for different V_{GS} while V_{DS} is kept constant at 0.5 V.

When the V_{GS} raises from 0 to 1 V, a noticeable change is observed in the bending of the potential curve. At $V_{GS} = 0$ V, the curve bending is pronounced, indicating that the channel region is fully depleted. In contrast, at the highest V_{GS} of 1 V, the potential curve flattens, signifying that the channel is nearing the flat-band condition. Figure 7 shows the I_D variation with varying doping concentration (N_D) at a constant V_{DS} of 0.5 V for MiG-JLT presented in both linear and log scale.

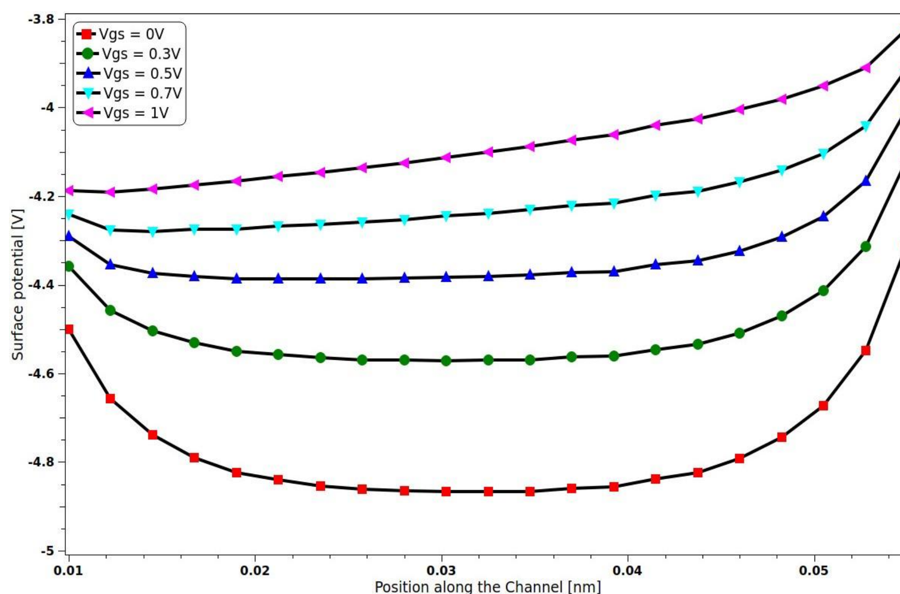

Figure 6. Surface potential profile along the channel at different V_{GS} (0, 0.3, 0.5, 0.7, and 1 V)

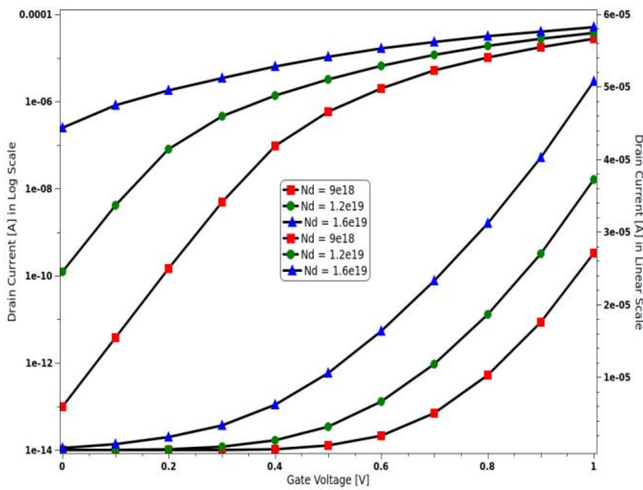

Figure 7. I_D versus V_{GS} at different doping concentrations, N_D for MiG-JLT in linear and log scale

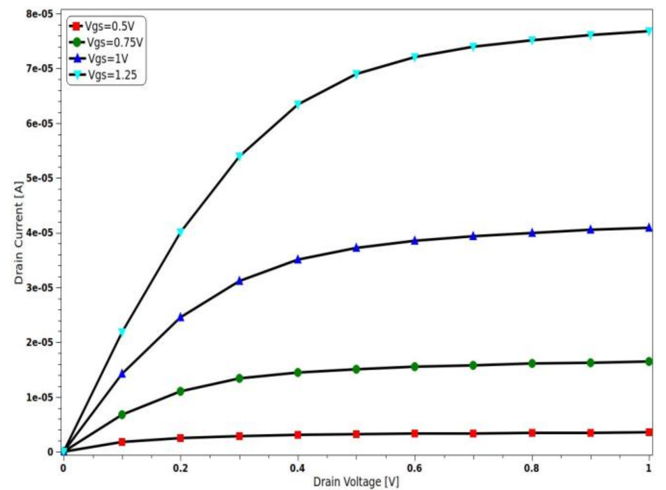

Figure 8. I_D versus V_{DS} at V_{GS} of 0.5, 0.75, 1, and 1.25 V

An increase in doping concentration substantially enhances both the ON-state and the leakage currents due to the higher density of mobile carriers. This necessitates a stronger electric field for depletion, degrading the subthreshold behaviour of the device, increasing the OFF-state current, and lowering the I_{ON}/I_{OFF} ratio. Figure 8 depicts the I_D versus V_{DS} for V_{GS} (0.5, 0.75, 1, and 1.25 V) in MiG-JLT. The I_D rises significantly with V_{GS} once the threshold voltage is surpassed, particularly in the range of V_{GS} 0.75–1.25 V. Figure 8 shows the I_D with V_{DS} by varying V_{GS} (0.5, 0.75, 1, and 1.25 V) for MiG-JLT. The I_D is found to increase with increasing V_{GS}, especially once the device exceeds the threshold voltage, corresponding to V_{GS} values between 0.75–1.25 V.

Figures 9 and 10 display the transconductance and drain conductance, respectively, for different silicon film thicknesses. For all devices, g_m exhibits a broad maximum in the high V_{GS} region (~1.3–1.4 V). From the simulated curves, the peak transconductance increases monotonically with T_{Si}: devices with $T_{Si} = 8$, 10, 12, and 14 nm attain approximate maxima of 4×10^{-5}, 7×10^{-5}, 8×10^{-5}, and 9×10^{-5} S, respectively, as obtained by graphical extraction at the flattest portion of each g_m-V_{GS} curve. Similarly, the g_d is extracted from the simulated g_d-V_{DS} characteristics for the same set of thickness. In the near-linear region around $V_{DS} \approx 0$ V, the devices with $T_{Si} = 8$, 10, 12, and 14 nm exhibit conductance of approximately 1×10^{-4}, 1.3×10^{-4}, 1.6×10^{-4}, and 1.9×10^{-4} S, which decrease to about 5.5×10^{-5}, 7×10^{-5}, 8.5×10^{-5}, and 1×10^{-4} S respectively, at $V_{DS} \approx 1$ V. These values are read graphically at the endpoints of the g_d-V_{DS} curves and represent the incremental slope $\delta I_D/\delta V_{DS}$ under a fixed gate bias. As anticipated, both the transconductance and drain conductance rise in tandem with the thickness of silicon, highlighting the strong dependence of analog performance on the body thickness.

4. CIRCUIT PERFORMANCE ANALYSIS

In this section, the circuit performances were studied by designing an inverter circuit in 3-D TCAD. The voltage transfer characteristic (VTC) and switching characteristics were studied. Figure 11 shows the design of the CMOS inverter circuit based on the MiG-JLT structure.

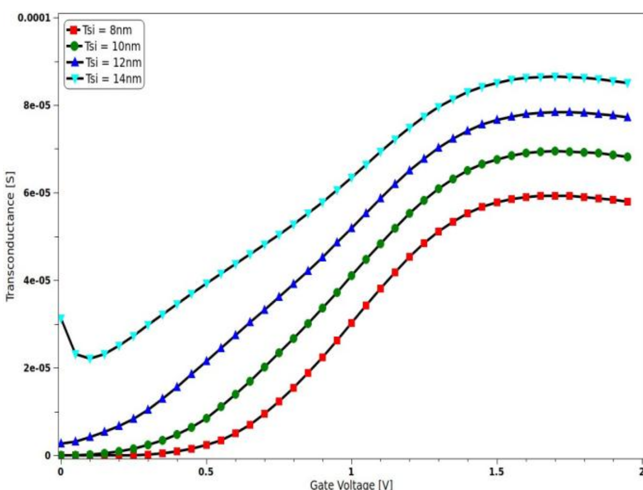

Figure 9. Transconductance as a function of $T_{Si} = 8$, 10, 12, and 14 nm

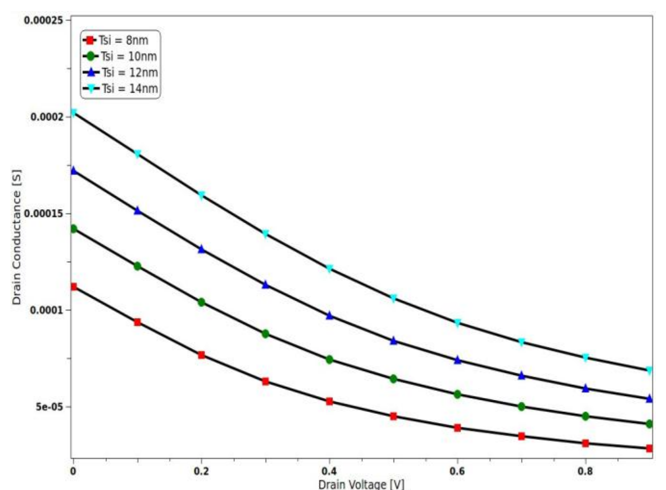

Figure 10. Drain conductance as function of $T_{Si} = 8$, 10, 12, and 14 nm

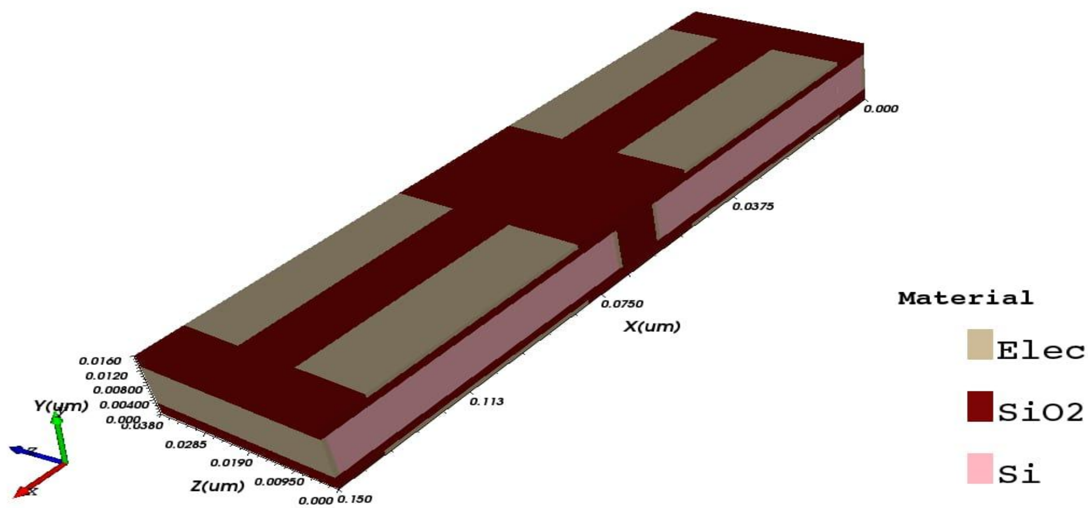

Figure 11. CMOS inverter based on MiG-JLT using 3-D TCAD

Here, the NMOS and PMOS are realized by alternating the doping within the same device, enabling the design of complementary devices suitable for CMOS applications. For a fair comparison, similar structures of SDG-JLT and single-gate JLT (SG-JLT) are also developed. All the device architectures are modelled using TCAD simulations to evaluate their performance at both device and circuit levels. Figure 12 shows the VTC of the symmetric double gate (SDG) inverter, single gate (SG) inverter, and MiG-JLT inverter. The results show that the MiG-JLT inverter exhibits performance comparable to that of the SDG inverter, with both achieving steeper switching slopes and improved noise margins compared to the SG inverter.

Figure 13 displays the switching characteristics of the MiG-JLT inverter by comparing it with the SDG inverter and SG inverter. The results clearly indicate that the MIG-JLT inverter achieves better switching performance than its counterparts, the SDG and SG inverters.

5. CONCLUSION

This work presented a comprehensive performance evaluation of a MiG-JLT. The introduction of a mid-insulating gate segment significantly modifies the electrostatic behaviour of the channel, resulting in enhanced ON-state current, improved transconductance, and controlled drain conductance. Analytical modelling based on quasi-two-dimensional electrostatics supports the simulation findings and explains the observed surface potential and electric field distributions. The proposed MiG-JLT demonstrates strong potential for high-performance nanoscale and SPICE-compatible device applications.

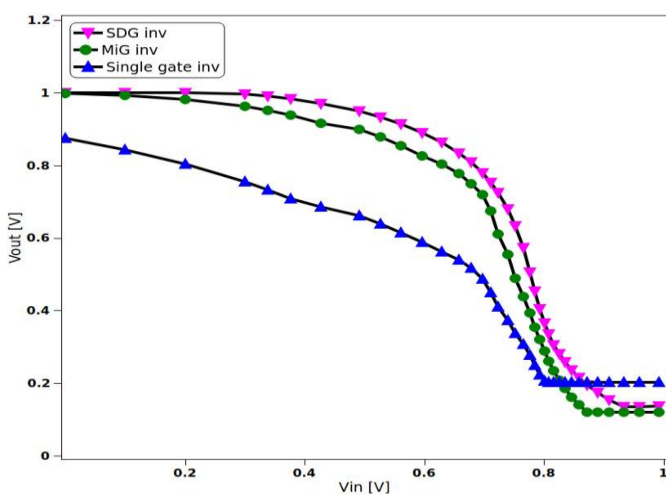

Figure 12. Comparison of VTC of MiG-JLT, SDG-JLT, and SG-JLT

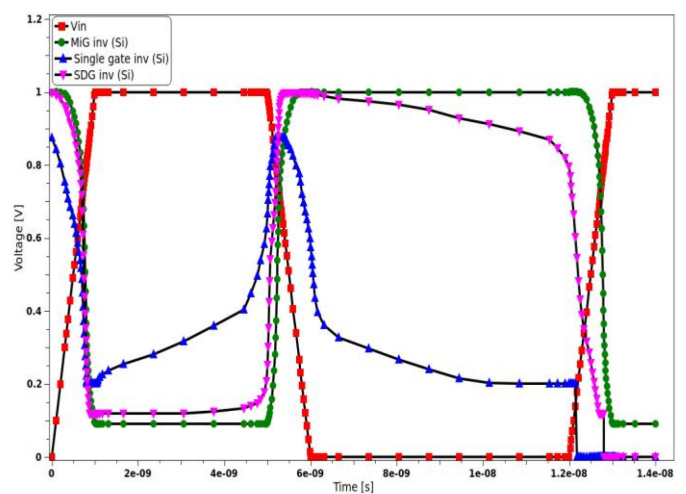

Figure 13. Comparison of the switching characteristics of MiG-JLT, SDG-JLT, and SG-JLT

ACKNOWLEDGMENTS

We are very thankful to the Chips to Startup (C2S) program, MeitY, Govt. of India, for providing the necessary software support for this research work.

REFERENCES

[1] T. K. Chiang, "A new quasi-2-D threshold voltage model for short-channel junctionless cylindrical surrounding gate (JLCSG) MOSFETs," *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 3127–3129, 2012.

[2] J. T. Park and J. P. Colinge, "Multiple-gate SOI MOSFETs: Device design guidelines," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2222–2229, 2002.

[3] P. Kuo, Y. Lu, and T. Chao, "High-Performance GAA Sidewall-Damascened Channels Junctionless FETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3821–3826, 2014.

[4] Z. Wang *et al.*, "Ultra-Low Power Hybrid TFET-MOSFET Topologies for Standard Logic Cells with Improved Comprehensive Performance," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, IEEE, 2019, pp. 1–5.

[5] G. L. Priya and N. B. Balamurugan, "New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation," *AEU - International Journal of Electronics and Communications*, vol. 99, pp. 130–138, 2019.

[6] B. Parvais *et al.*, "The device architecture dilemma for CMOS technologies: Opportunities & challenges of finFET over planar MOSFET," in *2009 International Symposium on VLSI Technology, Systems, and Applications*, IEEE, Apr. 2009, pp. 80–81.

[7] N. B. Bousari, M. K. Anvarifard, and S. Haji-Nasiri, "Improving the electrical characteristics of nanoscale triple-gate junctionless FinFET using gate oxide engineering," *AEU - International Journal of Electronics and Communications*, vol. 108, pp. 226–234, 2019.

[8] D. Sharma and S. K. Vishvakarma, "Precise analytical model for short channel Cylindrical Gate (CylG) Gate-All-Around (GAA) MOSFET," *Solid-State Electronics*, vol. 86, pp. 68–74, 2013.

[9] A. Goel, S. Rewari, S. Verma, and R. S. Gupta, "High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for high frequency applications," *Microsystem Technologies*, vol. 26, no. 5, pp. 1697–1705, 2020.

[10] J. P. Colinge *et al.*, "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.

[11] N. Bora, N. Deka, and R. Subadar, "A drain current and transconductance analytical model for symmetric double gate junctionless FENT," *Journal of Nano Research*, vol. 65, pp. 39–50, 2020.

[12] N. Bora, N. Deka, and R. Subadar, "Quantum mechanical analysis on modeling of surface potential and drain current for nanowire jlfet," *Journal of Nano Research*, vol. 64, pp. 123–134, 2020.

[13] N. Bora, "An Approach for Drain Current Modeling Including Quantum Mechanical Effects for a DMDG Junctionless Field Effect Nanowire Transistor," *Silicon*, vol. 14, no. 9, pp. 4945–4954, 2022.

[14] Ajay, R. Narang, M. Saxena, and M. Gupta, "Modeling and simulation investigation of sensitivity of symmetric split gate junctionless fet for biosensing application," *IEEE Sensors Journal*, vol. 17, no. 15, pp. 4853–4861, 2017.

[15] S. Kumar, B. Singh, and Y. Singh, "Analytical Model of Dielectric Modulated Trench Double Gate Junctionless FET for Biosensing Applications," *IEEE Sensors Journal*, vol. 21, no. 7, pp. 8896–8902, 2021.

[16] N. Garg, Y. Pratap, M. Gupta, and S. Kabra, "Dielectric Separated Independent Gates Junctionless Transistor (DSIG-JLT) for Highly Scaled Digital Logic Implementation," *IEEE Transactions on Nanotechnology*, vol. 20, pp. 262–269, 2021.

[17] A. K. Raibaruah and K. C. D. Sarma, "A Potential Model for Parallel Gated Junctionless Field Effect Transistor," *Silicon*, vol. 14, no. 2, pp. 711–718, 2022.

[18] S. Singh, B. Raj, and S. K. Vishvakarma, "Analytical modeling of split-gate junction-less transistor for a biosensor application," *Sensing and Bio-Sensing Research*, vol. 18, pp. 31–36, 2018.

[19] B. Yu, L. Wang, Y. Yuan, P. M. Asbeck, and Y. Taur, "Scaling of nanowire transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 2846–2858, 2008.

[20] B. Smaani *et al.*, "Recent progress on field-effect transistor-based biosensors : device perspective," *Beilstein Journal of Nanotechnology*, vol. 15, pp. 977–994, 2024.

[21] D. Singh, G. C. Patil, and B. D. Choudhury, "Split Gate Bulk-Planar Junctionless FET-Based Biosensor for Label-Free Detection of Biomolecules," *IEEE Sensors Journal*, vol. 24, no. 18, pp. 28611–28618, 2024.

[22] S. Khan and E. Rahman, "Designing the cavity architecture in double gate junctionless field effect transistors for enhanced biomolecule detection," *Nanoscale Advances*, vol. 7, no. 12, pp. 3746–3763, 2025.

[23] S. Kumar, A. K. Chatterjee, and R. Pandey, "Analytical modeling of recessed double gate junctionless field-effect-transistor in subthreshold region," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 37, no. 2, 2024.

[24] S. Barraud *et al.*, "Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm," *IEEE Electron Device Letters*, vol. 33, no. 9, pp. 1225–1227, 2012.

[25] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, New Jersey: John Wiley & Sons, 2007.