International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

Improvement of gate oxide thickness uniformity in advanced U-MOSFETs through multi-layer furnace oxidation

Lee Boon Thuan [a,c*], M.K. Md Arshad [b,c*], and W.M.W Norhaimi[c]

[a]*SilTerra Malaysia Sdn Bhd. Kulim Hi-tech Park, 09090, Kulim, Kedah.*
[b]*Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, Jln Kangar-Alor Setar, 01000, Kangar, Perlis, Malaysia.*
[c]*Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia*
** Corresponding author. e-mail: mohd.khairuddin@unimap.edu.my, boonthuan@studentmail.unimap.edu.my, bt.lee@yahoo.co.uk*

Received 30 August 2025, Revised 31 January 2026, Accepted 5 February 2026

ABSTRACT

Gate oxide uniformity is very important to the electrical wafer test performance such as Breakdown Voltage (B_{VDSS}), Gate Source Leakage Current (I_{GSS}), Gate Charge and reliability for vertical trench MOSFETs (U-MOSFETs), particularly in advanced scaling designs with compact cell layouts for lower Drain Source On Resistance (R_{DSON}). This study investigates gate oxide formation in a high-density N-type 30V UMOSFET with a 0.8 µm cell pitch from Product B. Conventional dry oxidation produces non-uniform oxide thickness, especially at the trench corners, leading to degradation of the B_{VDSS} and leakage characteristics (I_{GSS}). To address this, we propose a multi-layer thermal oxidation process combining the dry and wet oxidation, achieving improved corner coverage while maintaining a target gate oxide thickness of 500 Å. Transmission electron microscopy (TEM) analysis confirms that the multi-layer thermal oxidation (dry and wet oxidation) method reduces thickness variation from more than 25% to less than 10% compared to pure dry oxidation. Electrical characterization shows enhanced B_{VDSS}, I_{GSS} and stable threshold voltage (V_{TH}) without impacting (R_{DSON}). These results demonstrate that the proposed multi-layer thermal oxidation process is an effective approach for fabricating robust gate oxides in next-generation, scaled power MOSFETs. It is suggested that trench depth and P-body doping are further optimized to improve the balance between breakdown voltage and threshold voltage.

Keywords: *UMOSFET, Gate oxide uniformity, B_{VDSS}, I_{GSS}, V_{TH}, R_{DSON}, TEM, Thermal oxidation, Dry and wet oxidation*

1. INTRODUCTION

The gate oxide is a key component of metal-oxide-semiconductor field-effect transistors (MOSFET). It is made of silicon dioxide (SiO_2) that separates the gate control electrode and silicon surface, which serves as a dielectric or insulating layer for channel formation. The formation of gate oxide in power semiconductor MOSFETs are generally categorized into two primary architectures, lateral and vertical, which based on their physical structure and the direction of current flow through the device, as illustrated in Figure 1. Lateral power MOSFETs see Figure 1(a), often referred to as Laterally Diffused MOSFET (LDMOS) due to their current flowing from source to drain on a flat surface, making the gate oxide fabrication relatively simple but limiting the performance due to geometry scaling on lateral cell pitch, which requires increasing the chip to handle higher voltage rating. This lateral structure makes the device can easily integrated with analog and digital control for low-power applications such as smart power IC, and power management [1]**.** In contrast the vertical MOSFET conducts current flows vertically from gate-source at the top, through the body and drift region, to drain at the bottom. Planar vertical MOSFETs see Figure 1(b) is generally an upgrade version of LDMOS which physically different in substrate material and has a thicker drift region that supports higher blocking voltages [2]. This property makes it suitable for medium to high voltage power electronics, though at the cost of increased resistance compared to U-MOSFETs. Vertical trench MOSFET or U-MOSFET [see Figure 1(c)] improves performance by etching the gate into vertical trenches, allowing current to flow vertically through the channel walls. This unique physical structure creates the conduction path, which lowers the on-resistance (R_{DSon}) [3] [4] [5] and enables high density, making it ideal for medium-voltage applications such as DC–DC converters [6] and motor drives. In summary, the architectures layout of lateral and vertical power MOSFET design distinguish the result on trade-offs between resistance, current capability, and voltage handling. The challenge of growing gate oxide in the vertical trench or U-MOSFET has shown significant impact for gate oxide thickness uniformity in the scaling of geometry [7] and device performance in terms of reliability [8] [9] for advance cell pitch for lower R_{DSON} [10] [11].

Table 1 summarizes the U-MOSFET product which encounter B_{VDSS} not meeting the electrical requirement and some of the product has to revise the Epitaxial (Epi) substrate in order to meet the B_{VDSS} requirement, however this changes has drawn back on the R_{DSON} performance [12] which depends to end-user to define on the application of the product. In this work, we focus on the B_{VDSS}

improvement for advance cell pitch on Product B which require stringent requirement on B_{VDSS} above 30 V without sacrifice the R_{DOSN} performance. The N-type U-MOSFET, for 30 V was fabricated with an advanced cell pitch of 0.8 µm (0.2 µm spacing / 0.6 µm MESA) for attractive R_{DSON} however the B_{VDSS} performance is below 30 V as shown in Figure 2. The R_{DSON} for other products were sacrifice by changing the substrate Epi in order to achieve the B_{VDSS} according to electrical requirement.

Figure 3 illustrates the cross-sectional profile of the UMOSFET, with terminal connections labeled based on the top view layout to identify the source, gate and drain. The outer ring, also known as the termination ring, is designed according to product-specific requirements and design rules [13] [14]. The gate oxide within the vertical trench source region plays a critical role in channel formation, which directly defines key electrical characteristics such as V_{TH}, I_{DSS} and B_{VDSS} [15].

Table 2 summarizes the static characteristic data of the fabricated N-type 30 V U-MOSFETs obtained from wafer level testing. The process evaluation considered substrate structure (single Epi vs. dual Epi with different resistivity and thickness), trench depth (1.5–2.0 µm), and gate oxide thickness (500 Å and 800 Å, formed by dry oxidation). The N-body implant process condition followed the process of record (POR) at 1.0×1013cm−2−2, 150 keV.

As shown in Table 2, the measured parameters for gate leakage in the forward (I_{GSSP}) and reverse (I_{GSSN}) directions, absolute gate leakages (IGSSN-ABS) are all within nominal range without major variation. However, the interaction of threshold voltage (V_{TH}), breakdown voltage (B_{VDSS}), and drain-source leakage current (I_{DSS}), confirm that thinner oxides (500 Å) support the 30 V product targets, while the thicker oxide (800 Å) demonstrates improved leakage suppression, consistent with preliminary requirements for future 80 V product developments.

The result shows that B_{VDSS} performance with a 500 Å gate oxide does not meet the product requirement, as highlighted in shaded red for the 30 V devices, with additional failures observed in V_{TH} and I_{DSS}. Based on Epi split, a noticeable increased in B_{VDSS} was observed when moving from dual Epi to single Epi; however, this improvement came at the expense of higher R_{DSON}. By increasing the gate oxide thickness from 500 Å to 800 Å, resulted in a significant improvement in B_{VDSS} but also caused a violation in the electrical characteristic in V_{TH}, which exceed the functional limit of 1.5 V for 30 V products. For instance, values of 1.98 V and 3.0 V correspond to designs intended for 40 V and 80 V products, respectively.

Subsequently, failure analysis (FA) was performed on the failed unit with a 500 Å gate oxide. At the source's location, Figure 4(a) reveals that the gate oxide thickness at the bottom corner is approximately 25% thinner, leading to localized high electric-field stress and degradation of B_{VDSS} performance [16]. In contrast, the finger or gate location, shown in Figure 4(b) demonstrates a uniform gate oxide thickness throughout the trench structure. A comparison of the FA profiles between the source and gate regions highlights growing concerns regarding the gate oxide reliability. As the device scaling advances toward narrower cell pitches and higher current densities, the need for a robust and reliable gate oxide formation process becomes increasingly critical. To address this, several researchers have investigated methods to improve trench gate oxide uniformity, including trench sidewall plasma treatment [17], trench corner rounding using sacrificial oxidation prior to gate oxidation [18] [19], chemical vapour deposition (CVD) [20], and multi-layer oxidation processes [16].

Therefore, this study is aimed to address this critical knowledge gap by examining oxide growth behavior at trench corners, where thinning occurs, and its impact on B_{VDSS}, particularly in aggressively scaled devices (0.8 µm pitch) designed for N-type 30 V products with a 500 Å gate oxide thickness. To overcome the limitations of achieving uniform trench gate oxide at this thickness in advanced cell pitch designs, we propose a hybrid oxidation fabrication method.

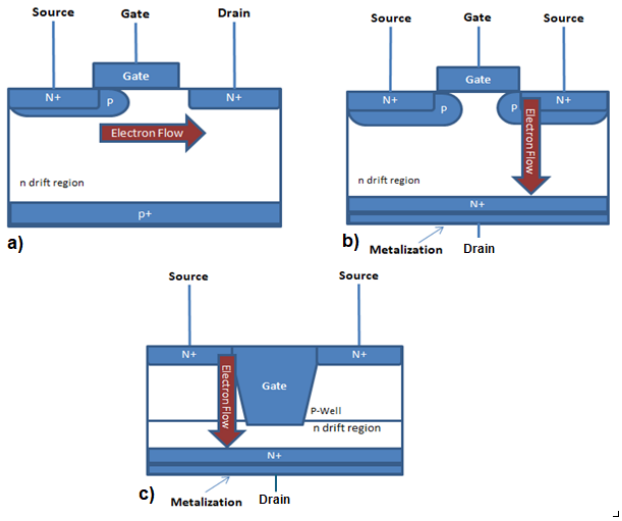

Figure 1. Structure reference for types of Power MOSFET (a) Lateral, (b) Vertical with Poly on silicon surface, (c) Vertical with Poly in the silicon trench (current and electron flows in opposite way)

Table 1. Summary of U-MOSFET product in wafer level test

Product	Cell Pitch µm	Trench CD (SPACE) µm	MESA CD (Silicon) µm	Gate Oxide Å	Igss, V_{TH} drift	B_{VDSS} (Gate Oxide non uniformity)
Product A	0.8	0.2	0.6	500	● ●	P-type (30V) Epi revise (sacrifice the R_{DSON})
Product B	0.8	0.2	0.6	500	● ●	N-type (30V) Not allow for Epi revise (concern on R_{DSON})
Product C	0.9	0.2	0.8	600	● ●	P-type (30V), N-type (30V) Epi revise (concern on R_{DSON})
Product D	1.0	0.2	0.9	600	● ●	N-type (30V to 100V) Epi revise (no concern on R_{DSON})
Product E	1.2	0.2	1.0	800	● ●	

Legend
● Pass ● Sacrifice Rdso ● Fail ● V_{TH}, Body Implant Adjust

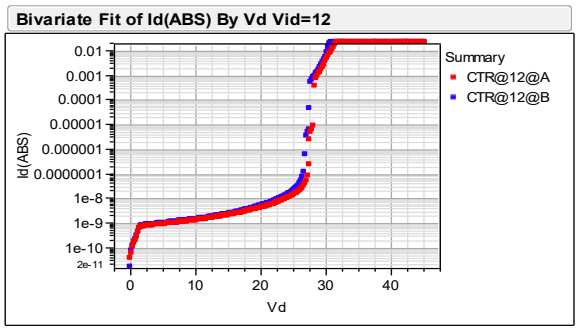

Figure 2. B_{VDSS} represented by drain source current (I_d-V_d) for Product B, N-Type 30 V

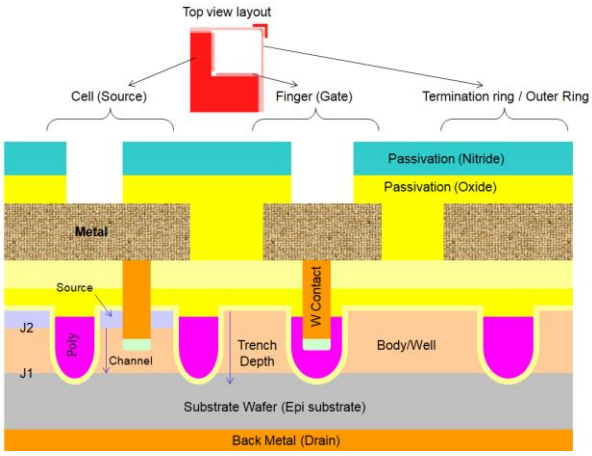

Figure 3. Cross-sectional view of U-MOSFET structure with terminal connection points (source, gate and termination ring)

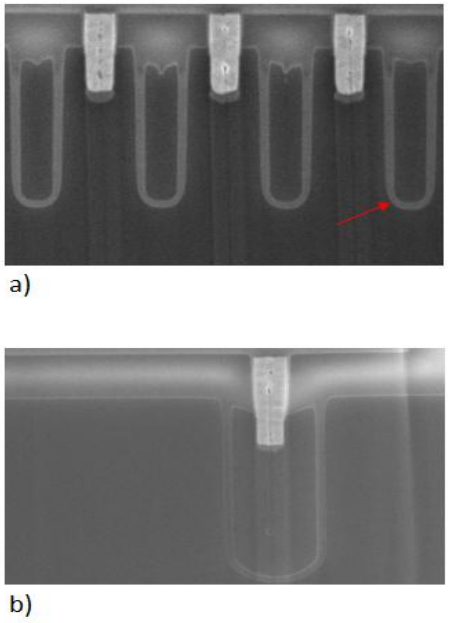

Figure 4. (a) Cross-Sectional profile of gate oxide profile review on cell location or source location showing gate oxide thinning at trench bottom (cell pitch 0.8µm with space CD 0.2 µm and MESA CD 0.6 µm), (b) Cross-Sectional profile on gate location shows conformal gate oxide structure along the trench side wall (drawn trench spacing CD 0.6 µm)

Table 2. Static characteristic of N-Type 30 V product in wafer level test

Substrate Wafer	Trench	Gate Ox	NBody Implant Dose	wf_num	IGSSP	IGSSN	IGSSN (ABS)	VTH	BVDSS	IDSS
Top:R0.145Ωcm*, T2.62µm,	2.0µm	500Å (Dry)		12	5.1E-10	-1.1E-09	1.1E-09	1.15	25.2	1E-02
Bottom:R0.05Ωcm*, T1.6µm (Dual Epi)				13	3.2E-10	-1.2E-09	1.2E-09	1.19	25.3	1E-02
Top:R0.145Ωcm*, T2.62µm,	2.0µm	500Å (Dry)		16	3.7E-10	-1.2E-09	1.2E-09	1.18	25.0	1E-02
Bottom:R0.05Ωcm*, T1.5µm (Dual Epi)				17	3.8E-10	-1.2E-09	1.2E-09	1.16	25.0	1E-02
Top:R0.145Ωcm*, T2.50µm,	2.0µm	500Å (Dry)		18	4.6E-10	-1.1E-09	1.1E-09	1.14	25.0	1E-02
Bottom:R0.05Ωcm*, T1.6µm (Dual Epi)			B11 / 150KeV / 1.0E13	19	1.0E-10	-1.0E-09	1.0E-09	1.15	25.0	1E-02
Top:R0.145Ωcm*, T2.75µm,	1.7um	500Å (Dry)		14	2.2E-10	-1.2E-09	1.2E-09	1.15	26.3	1E-02
Bottom:R0.05Ωcm*, T1.6µm (Dual Epi)	2.0µm	500Å (Dry)		15	3.9E-10	-1.3E-09	1.3E-09	1.18	25.7	1E-02
Top:R0.130Ωcm*, T2.62µm,	1.5µm	500Å (Dry)		20	2.3E-10	-1.2E-09	1.2E-09	1.00	26.3	1E-02
Bottom:R0.05Ωcm*, T1.6µm (Dual Epi)	1.7µm	500Å (Dry)		21	2.4E-10	-1.2E-09	1.2E-09	0.99	25.3	1E-02
	2.0µm	500Å (Dry)		22	4.1E-10	-1.2E-09	1.2E-09	1.02	25.3	1E-02
	2.0µm	800Å (Dry)		23	1.4E-10	-3.1E-10	3.1E-10	1.98	30.1	3E-04
R0.23, T6.0 (Single Epi)	2.0µm	500Å (Dry)		24	4.1E-10	-1.1E-09	1.1E-09	1.67	30.4	4E-06
	2.0µm	800Å (Dry)		25	1.1E-10	-2.6E-10	2.6E-10	3.00	36.1	1E-08

2. MATERIALS AND METHODS

2.1. Fabrication Process and Device Structure

The fabrication process of vertical trench or U-MOSFET, illustrated in Figure 3 and detailed in Figure 1A in Appendix 1, employs an advanced cell pitch of 0.8 µm, consisting of 0.2 µm of spacing and 0.6 µm MESA width. Trenches were patterned using photolithography and etched to a depth of 1 µm by plasma etching through an oxide hard mask. This was followed by two sacrificial oxide steps, with each oxide layers subsequently removed by HF cleaning. The purpose of the sacrificial oxidation is to repair the silicon surface damage and improve corner rounding prior to final gate oxide growth and polysilicon deposition. Table 3 summarizes the advanced cell pitch dimension before and after the gate oxidation process. While the overall cell pitch remains at 0.8 µm, both the trench (Critical Dimension) CD and MESA CD are altered due to silicon consumption during oxidation [21] [22]

Table 3. Advanced cell pitch dimension before and after gate oxidation.

No	Product A Process Step	Cell Pitch CD (0.8 µm)	Trench CD 0.2 µm (Spacing)	MESA CD 0.6 µm (Silicon)
1	Oxidation 1 (Sacrificial / Sacox 1)	0.8 µm	0.250	0.550
2	Oxidation 2 (Sacrificial / Sacox 2)	0.8 µm	0.300	0.500
3	Gate Oxide (500Å)	0.8 µm	0.350	0.450

2.2. Thermal Gate Oxidation Experiment

Following by the sacrificial oxidation and cleaning steps described in Section 2.1, the next critical process is the formation of the gate oxide inside the vertical trenches. This process step determines the interface quality of gate oxide and directly impacts the device's electrical performance on B_{VDSS}.

In this study, two thermal oxidation processes were carried out based on current furnace process option which available in CMOS fabrication environment and the main concern is the superior performance of thermal oxidation quality [23] [24] [25] . Figure 5 illustrate the setup of trench gate oxide thickness 500 Å for N-type 30 V Product B with POR scheme single step thermal dry oxidation and multi-layer thermal oxidation (dry and wet oxidation). Figure 6 presents the relationship between two types of thermal oxidation time and resulting oxide thickness. Figure 6(a) shows the correlation for thermal dry oxidation, while Figure 6(b) shows the same for combined of dry and wet oxidation (with a fix 100 Å dry oxidation before wet oxidation). Both graphs include the linear and polynomial fits plot, highlighting how process time can be optimized to achieve the precise gate oxide thickness using different thermal oxidation methods.

For single step thermal dry oxidation process, the resultants of gate oxide thickness are validated at 200 Å, 250 Å and 500 Å. As this is to understand how the gate oxide uniformity behaves for thermal dry oxidation scheme. The second method is a multi-layer thermal oxidation (dry and wet oxidation), the thermal oxidation is grown in two steps (100 Å plus 150 Å) to reach 250 Å, and in another step two steps (100 Å plus 400 Å) to reach 500 Å. And the TEM profile structure of each process combination process will be presented as final results of vertical trench or U-MOSFET gate oxide uniformity.

Figure 7 compares the furnace process thermal profiles for achieving a total oxide thickness of 500 Å using two methods. Figure 7(a) shows the temperature profile for dry oxidation, which involves a rapid ramp-up to a high temperature, a steady high-temperature oxidation step at 950 °C for 90 minutes, and a subsequent cool-down step at the end. Figure 7(b) presents the thermal profile for multi-layer oxidation (dry and wet oxidation), combining initial dry oxidation (100 Å) at 950 °C with a very short process time (10 minutes) to ensure a high quality Si/SiO_2 interface formation in the trench and followed by wet oxidation (400 Å) at 950 °C for (6 minutes) the final oxide thickness 500 Å, with additional annealing (1000 °C) for wet oxidation in-order to avoid on interface traps and density defects, for improving oxide quality, and enhancing electrical properties [26] [27].

Equation 1 and Equation 2 describe the fundamental oxidation reaction for dry and wet processes, respectively [28].

$$Si + O_2 = SiO_2 \quad (1)$$

$$Si + 2H_2O = SiO_2 + 2H_2 \quad (2)$$

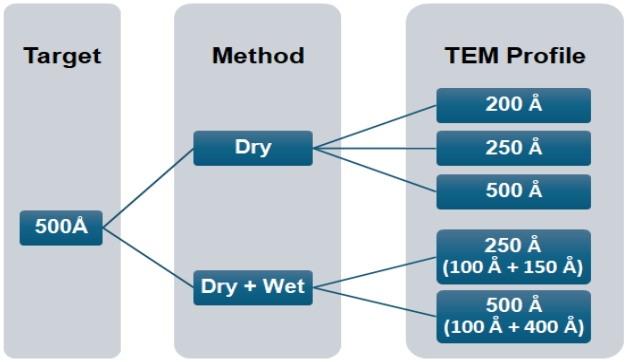

Figure 5. Thermal gate oxidation process for gate oxide target 500Å for dry oxidation and multi-layer thermal oxidation (dry and wet oxidation) with various thickness validation

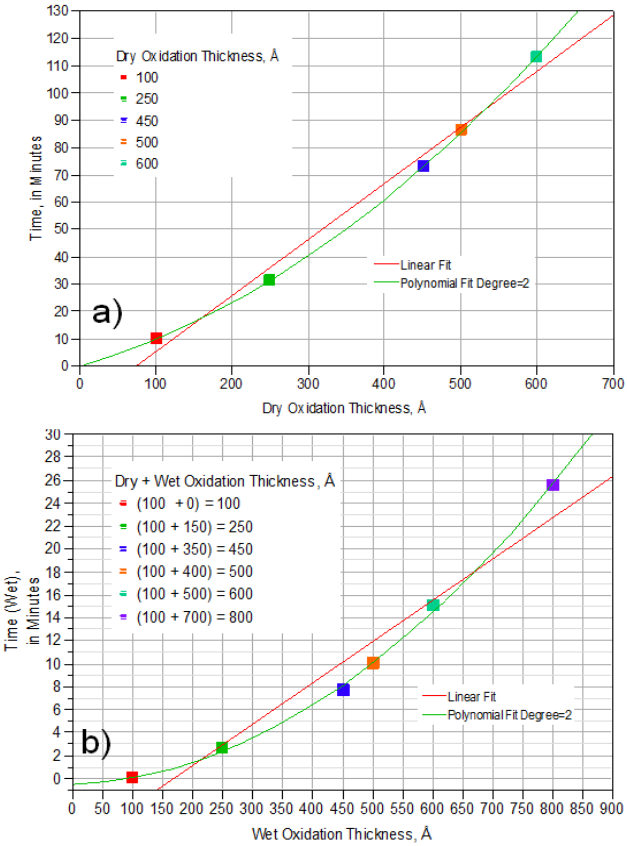

Figure 6. (a) Dry oxidation thickness by process time, (b) Wet oxidation thickness by process time (fix 100 Å before wet oxidation)

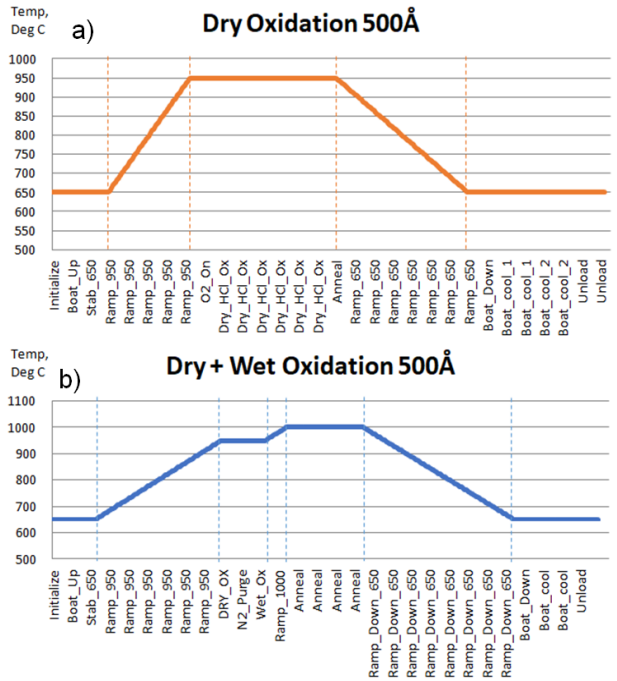

Figure 7. (a) Dry oxidation thermal profile for 500 Å, (b) Multilayer thermal oxidation (Dry oxidation 100 Å and wet oxidation 400 Å) process thermal profile with additional anneal process with final total thickness of 500 Å.

3. RESULTS AND DISCUSSION

3.1. Thickness Measurement and TEM Profile Review

Table 4 summarizes the average gate oxide thicknesses obtained from TEM profiling under different thermal oxidation condition, comparing conventional dry oxidation with multi-layer thermal oxidation (dry and wet oxidation) process. The measurements include the target oxide thickness, as well as the trench bottom and trench sidewall thicknesses, to validate process uniformity. These results are critical for evaluating UMOSFET device reliability and B_{VDSS} performance.

For the dry oxidation process, the 200 Å target thickness was achieved with good stability, showing a deviation within 5%. However, at the 250 Å target, the oxide thickness declined by about 10%, below the target, while at the 500 Å target, a significant thinning effect was observed, with the trench bottom thickness reduced by more than 25% compared to the target, as shown in Figure 2A (in Appendix).

In contrast, the multi-layer (dry and wet oxidation) process demonstrated improved uniformity within the trench profile. At the 250 Å target, the oxide thickness was slightly higher than expected, with an average increase of about 10%. For the 500 Å target, both the trench bottom and sidewall thickness remained within the 10% range, as shown in Figure 3A (in Appendix).

Overall, the experiment results indicate that the multi-layer thermal oxidation (dry and wet oxidation) approach is more effective in achieving uniform trench gate oxide formation at advanced scaling dimensions. In particular, this method successfully addresses the significant non-uniformity observed with the conventional dry oxidation process at the 500 Å target thickness.

Table 4. Gate oxide TEM profile thickness summary in average value (refer to appendix 2 and 3 for TEM profile)

No	Condition	Gate oxide thickness, Å	Trench bottom thickness, Å	Trench side wall thickness, Å	Remark
1	Dry	200	209	201	+ 5%
2	Dry	250	223	225	- 10%
3	Dry	500	314	434	- 25%
4	Dry + Wet	250	255	274	+ 10%
5	Dry + Wet	500	491	550	+/- 10%

3.2. Electrical Characteristic

Table 5 presents the measured electrical parameters of UMOSFET devices fabricated on different wafer substrate Epi type using the multi-layer thermal oxidation (dry and wet oxidation) process with different trench depths (1.1 µm, 1.3 µm, and 1.5 µm) and gate oxide thicknesses (500 Å and 800 Å). The table compares the threshold voltage (V_{TH}), breakdown voltage (B_{VDSS}), leakage currents (I_{GSSP}, I_{GSSN}, I_{DSS}), and the effect of different P-body implant conditions.

For devices with a 500 Å gate oxide, the threshold voltage (V_{TH}) values were consistently stable across all trench depths, ranging from 1.55 V to 1.86 V, which is within the expected design window. The leakage currents (I_{GSSP} and I_{GSSN}) remained in the order of 10^{-9} A, indicating that gate oxide integrity was maintained even at deeper trenches.

The breakdown voltage (B_{VDSS}) showed clear dependence on wafer substrate thickness and trench depth. At a trench depth of 1.1 µm, B_{VDSS} reached values up to 34.68 V, while at 1.3 µm, the breakdown voltage slightly decreased (≈ 32–33 V). Interestingly, at 1.5 µm trench depth with thicker wafer substrate epitaxial T5.2, the B_{VDSS} recovered and in some cases exceeded 33.44 V, suggesting that deeper trenches can enhance electric field distribution provided the gate oxide remains uniform. It is worth mentioning that with a 500 Å gate oxides, all trench depths achieved value above 30 V, which notable improvement compared to the earlier results is presented in Table 1.

The introduction of a thicker oxide (800 Å) at the 1.1 µm trench depth led to a significant increase in breakdown voltage, reaching 38.53 V, which represents the highest B_{VDSS} across all measured conditions. This confirms the role of oxide thickness in suppressing premature breakdown and improving device robustness.

The drain leakage current (I_{DSS}) remained within the low 10^{-9} A range for all conditions, confirming minimal impact from trench depth or oxide variation. This result validates the earlier TEM findings (Table 3), where the dry + wet oxidation process provided consistent trench oxide coverage, thereby reducing the risk of leakage-induced breakdown.

In summary, the electrical results in Table 5 validate the structural findings in Figure 4 and Table 4, demonstrating

that the multi-layer thermal oxidation (dry and wet oxidation) process produces consistent gate oxide quality and improved B_{VDSS} performance, especially when combined with optimized trench depth (1.1–1.5 µm) and thicker oxide formation (800 Å)

Figure 8(a) shows the transfer (I_d–V_g) and Figure 8(b) shows the gate leakage (I_g–V_g) characteristics of UMOSFET devices fabricated with dry-only and dry + wet oxidation sequence, both using a 500 Å gate oxide thickness.

In Figure 8(a), the I_d–V_d characteristics define the drain-to-source leakage and B_{VDSS} by applying a drain voltage with the source grounded. The I-V curves clearly indicate that the multi-layer oxidation process yields lower leakage and sustains higher breakdown voltages compared to dry oxidation, reflecting enhanced oxide robustness at the trench corners where electric field crowding is most critical.

Figure 8(b) shows the I_g–V_g characteristics under both positive and negative gate bias. This evaluation is crucial for evaluating gate oxide reliability under stress conditions, elucidating charge trapping mechanisms, and identifying leakage pathways. The results demonstrate that devices fabricated with the multi-layer thermal oxidation (dry and wet oxidation) process exhibit consistently lower leakage currents than dry-only oxides for both polarities, confirming improved gate oxide integrity.

These trends are in strong agreement with the measured parameters summarized in Table 5. Specifically, Table 5 shows that multi-layer thermal oxidation (dry and wet oxidation) consistently achieves higher B_{VDSS} values and significantly reduced gate and drain leakage currents (I_{GSS} and I_{DSS}) relative to dry oxidation alone. The correlation between the electrical curves in Figure 8 and the quantitative data in Table 4 validates the advantage of the multi-layer oxidation process: the inclusion of a wet oxidation step improves oxide uniformity and passivassion interface traps, leading to reduced leakage, enhanced reliability, and overall superior device performance at the 500 Å gate oxide level.

Table 5. Static characteristic data of UMOSFET

Substrate Wafer	Trench	GATE-OX	Pbody-Imp	IGSSP	IGSSN	IGSSN(ABS)	VTH	BVDSS	IDSS
R0.20, T5.0	1.1um	Dry+Wet 500Å	B/150KEV/9E12	5.664E-10	-3.780E-09	3.77988E-09	1.71	33.78	5.612E-09
	1.3um			7.166E-10	-6.074E-09	6.07409E-09	1.77	32.95	6.119E-09
	1.5um			8.144E-10	-9.584E-09	9.58373E-09	1.55	31.34	7.935E-09
R0.20, T5.2	1.1um	Dry+Wet 500Å	B/150KEV/9E12	5.842E-10	-4.001E-09	4.00145E-09	1.75	34.39	5.005E-09
	1.3um			6.841E-10	-5.989E-09	5.98876E-09	1.75	33.46	5.736E-09
	1.5um		B/150KEV/1E13	8.142E-10	-8.938E-09	8.93811E-09	1.86	32.29	6.662E-09
R0.20, T5.5	1.1um	Dry+Wet 500Å	B/150KEV/9E12	5.860E-10	-3.732E-09	3.73196E-09	1.72	34.68	4.964E-09
		Dry+Wet 800Å	B/150KEV/1E13	1.696E-10	-2.871E-10	2.87078E-10	2.74	38.53	1.092E-08
	1.5um	Dry+Wet 500Å	B/150KEV/9E12	7.481E-10	-9.528E-09	9.52756E-09	1.74	33.44	5.813E-09

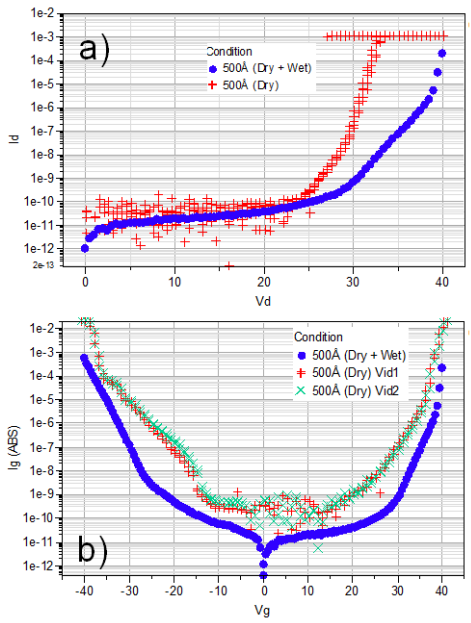

Figure 8. (a) B_{VDSS} represented by drain source current (I_d-V_d) characteristic with force drain voltage to source, (b) I_{GSS} represented by Gate source leakage current (I_g-V_g) characteristic.

4. CONCLUSIONS

In this study, we investigated the wafer fabrication process and optimized the 500 Å gate oxide thicknesses for N-type 30 V U-MOSFETs with an advanced cell pitch of 0.8 µm. The objective was to achieve the target B_{VDSS} of 30 V, by ensuring excellent gate oxide uniformity at a thickness of 500 Å, thereby delivering high performance and long-term reliability. The optimized process incorporated sacrificial oxidation steps to repair surface damage and create rounded trench corners before the final gate oxidation, thus improving the oxide integrity in areas exposed to high electric fields.

Two thermal oxidation strategies were compared between pure dry oxidation and a multi-layer thermal oxidation (dry and wet oxidation) process. TEM profile analysis revealed that the dry oxidation process produced consistent thinner oxide from the trench sidewall towards the bottom corner, struggling to achieve 500 Å thicknesses. This resulted in a noticeable non-uniformity and under grown oxide at trench bottoms. In contrast, the multi-layer thermal oxidation (dry and wet oxidation) approaches provide much better gate oxide thickness control and uniformity across the trench profile, effectively minimizing the gate oxide thinning at the trench corners.

Electrical characterization data confirmed the advantages of the multi-layer thermal oxidation method, exhibiting higher breakdown voltage (B_{VDSS}) and lower gate leakage current (I_{GSS}). Using this multi-layer thermal oxidation scheme, the devices achieved superior leakage performance without sacrificing breakdown capability, demonstrating its robustness for N-type 30V U-MOSFETs (Product B). Furthermore, the multi-layer thermal oxidation scheme is scalable and applicable to higher gate oxide thickness requirements for 40 V, 60 V, 80 V and 100 V products.

ACKNOWLEDGMENTS

This project was experimented by SilTerra Malaysia Sdn Bhd. The authors would like to thank Universiti Malaysia Perlis and SilTerra staff for providing the research materials.

REFERENCES

[1] R. Bott, "Lateral Power Mosfets Hardened Against Single Event Radiation Effects," *Igarss 2014*, no. 1, pp. 1–5, 2014.

[2] Z. J. Shen, D. Okada, F. Lin, A. Tintikakis, and S. Anderson, "Lateral discrete power MOSFET: Enabling technology for next-generation, MHz-frequency, high-density DC/DC converters," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 1, no. C, pp. 225–229, 2004.

[3] M. Annese, P. Montanini, F. Toia, L. Zullino, and C. Contiero, "20V-40V Symmetrical Vertical Trench nMOS (SVT MOS) design for display driver ICs," in *2006 IEEE International Symposium on Power Semiconductor Devices & IC's*, 2006, pp. 1–4.

[4] ALPHA & OMEGA, "Power MOSFET basics," *ALPHA OMEGA Semicond.*, pp. 1–10, 2008, [Online]. Available: http://www.aosmd.com/res/application_notes/mosfets/Power_MOSFET_Basics.pdf.

[5] M. M. A. H. and A. H. M. Z. Alam., "A new vertical power MOSFET with extremely reduced on resistance and high switching speed with multilayer structure," *First Int. Conf. Electr. Comput. Eng. (ICECE 2001), Dhaka, Bangladesh, 2001-01-01*, vol. 32, no. 1, pp. 163–166, Jan. 2001.

[6] S. G. Kim *et al.*, "A novel trench gate MOSFET with a multiple-layered gate oxide for high-reliability operation," *J. Korean Phys. Soc.*, vol. 60, no. 10, pp. 1552–1556, 2012.

[7] S. A. Suliman *et al.*, "The dependence of UMOSFET characteristics and reliability on geometry and processing," *Semicond. Sci. Technol.*, vol. 16, no. 6, pp. 447–454, Jun. 2001.

[8] J. Hao, A. Ghosh, M. Rinehimer, J. Yedinak, and M. A. Alam, "BVDSS Instability in shielded trench power MOSFETs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, no. January, pp. 6E.5-1-6E.5–4.

[9] G. Niu, W. T. K. Chien, G. Zhang, J. Yu, X. Zhao, and X. Duan, "Gate oxide reliability improvement for UMOS technology," *Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits, IPFA*, vol. 2015-Augus, no. Table 1, pp. 342–345, 2015.

[10] W. B. G. Richard K. Williams, "Vertical Trench-Gated Power MOSFET Having Stripe Geometry And High Cell Density," US6204533B1, 2001.

[11] K. Kobayashi, A. Kaneko, Y. Murase, and H. Yamamoto, "Sub-micron Cell Pitch 30 V N-channel UMOSFET with Ultra Low On-resistance," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, May 2007, pp. 205–208.

[12] H. Wang, "Power MOSFETs with Enhanced Electrical Characteristics," University of Toronto, 2009.

[13] B. (BE); Michael A. A. In't Zandt, Veldhoven (NL); Erwin A. Hijzen and H. (NL) Raymond J. E. Hueting, "Edge Termination in A Trench gate MOSFET," USOO6833583B2, 2004.

[14] C. (US); Yeeheng Lee, San Jose, CA (US); Madhur Bodbe, Sunnyvale, C. (US); Daniel Calafut, San Jose, CA (US); Hamza Yilmaz, Saratoga, C. (US); H. C. Xiaobin Wang, San Jose, CA (US); Ji Pan, San Jose, and O. (US) Saratoga, CA (US); Jongoh Kim, Portland, "Termination Trench For Power MOSFET Applications," 2015.

[15] S. Kuboyama, A. Maru, N. Ikeda, T. Hirao, and T. Tamura, "Characterization of microdose damage caused by single heavy ion observed in trench type power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6 PART 1, pp. 3257–3261, 2010.

[16] M. Neuber, O. Storbeck, M. Langner, K. Stahrenberg, and T. Mikolajick, "Multi-staged deposition of trench-gate oxides for power MOSFETs," *J. Vac. Sci. Technol. B*, vol. 37, no. 3, p. 032202, 2019.

[17] L. Jin *et al.*, "Sidewall Modification Process for Trench Silicon Power Devices," *Electron.*, vol. 12, no. 11, 2023, doi: 10.3390/electronics12112385.

[18] H. S. Ng, "Review on Methods for Trench MOSFET Gate Oxide Reliability and Switching Speed Improvement," *ECS Trans.*, vol. 27, no. 1, pp. 21–26, 2010.

[19] Ng Hong Seng, "Improved corner rounding method for trenched MOSFET," in *2010 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*, Nov. 2010, no. Trench Bottom Corner Rounding, pp. 1–3.

[20] K. Hieber, M. Stolz, and C. Weiczorek, "Lower Pressure CVD and Plasma Enhance CVD," *Proc. - Electrochem. Soc.*, vol. 84–6, no. Cvd, pp. 205–212, 2011.

[21] B. E. Deal and A. S. Grove, "General relationship for the thermal oxidation of silicon," *J. Appl. Phys.*, vol. 36, no. 12, pp. 3770–3778, 1965.

[22] V. Šimonka, A. Hössinger, J. Weinbub, and S. Selberherr, "Growth rates of dry thermal oxidation of 4H-silicon carbide," *J. Appl. Phys.*, vol. 120, no. 13, 2016.

[23] Dah-Bin Kao, J. P. McVittie, W. D. Nix, and K. C. Saraswat, "Two-dimensional silicon oxidation

experiments and theory," in *1985 International Electron Devices Meeting*, 1985, no. 1, pp. 388–391.

[24] H. Z. Massoud, J. D. Plummer, and E. A. Irene, "Thermal Oxidation of Silicon in Dry Oxygen: Growth-Rate Enhancement in the Thin Regime: II . Physical Mechanisms," *J. Electrochem. Soc.*, vol. 132, no. 11, pp. 2693–2700, 1985.

[25] S. A. Suliman, "Properties of Si / SiO2 interfaces in vertical trench MOSFETs," *Ext. Abstr. Sixth Int. Work. Junction Technol. IWJT '06*, no. 100, pp. 225–228, 2006.

[26] R. Sharangpani and Sing-Pin Tay, "Effect of growth and annealing conditions on interface charge of dry and wet oxides grown using rapid thermal oxidation," in *9th International Conference on Advanced Thermal Processing of Semiconductors, RTP 2001*, 2001, pp. 273–286.

[27] C.-T. Wu, J. Sharp, G. Madson, and J. Michalowicz, "The Effects of Hydrogen Annealing on Gate Oxide Integrity of U-Shaped Trench MOSFET with 400 Å Gate Oxide," *J. Electrochem. Soc.*, vol. 153, no. 10, p. G916, 2006.

[28] A. Anusha, C. Parameswaran, P. Revathi, and V. Velmurugan, "Numerical simulation of dry and wet oxidation of Silicon by TCAD Sprocess," in *International Conference on Advanced Nanomaterials & Emerging Engineering Technologies*, Jul. 2013, pp. 513–516.

Supplementary Appendix 1

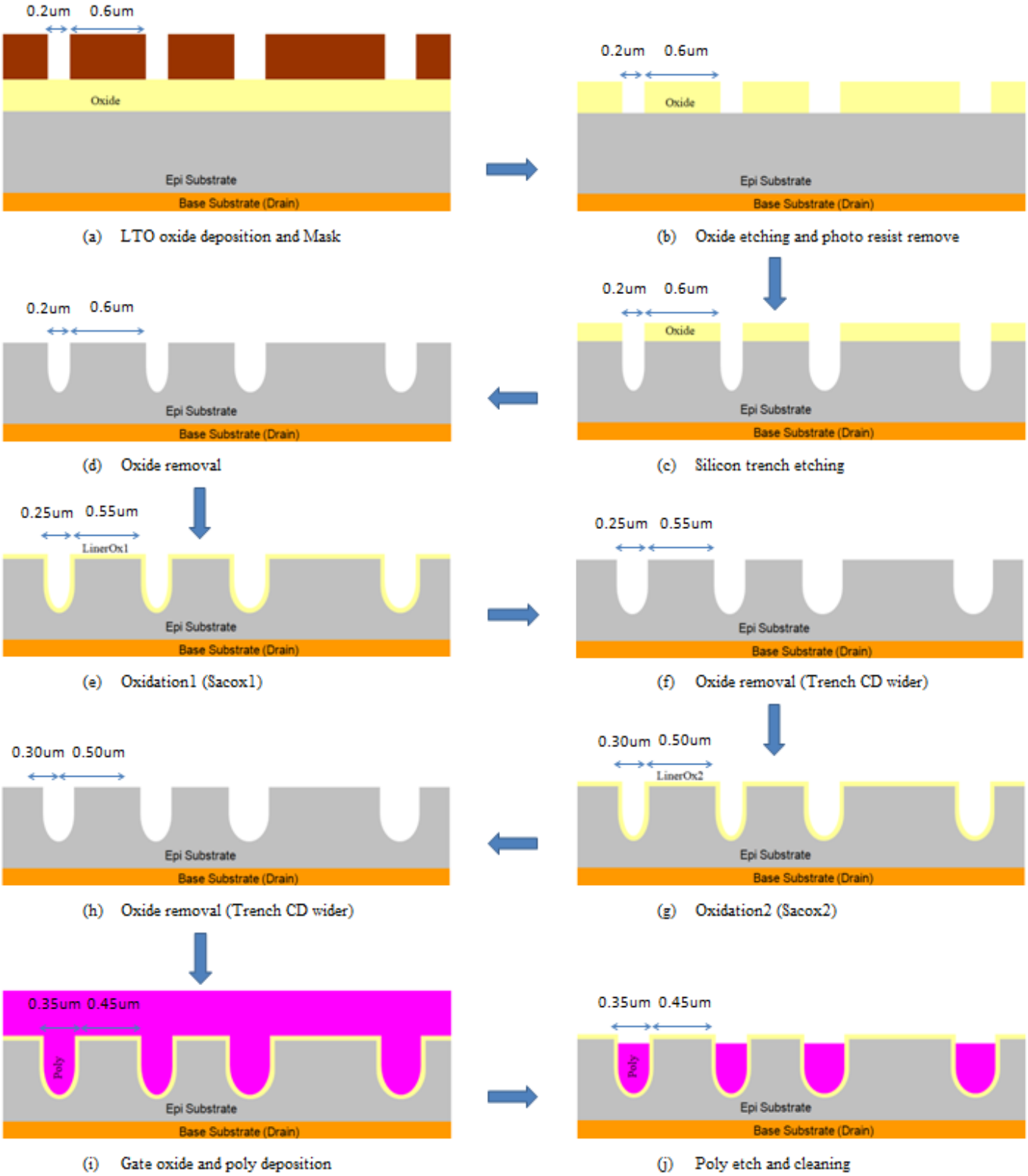

Figure 1A: Fabrication of UMOSFET for Gate Oxide Module with advanced cell-pitch sizing dimension before and after gate oxidation

Supplementary Appendix 2

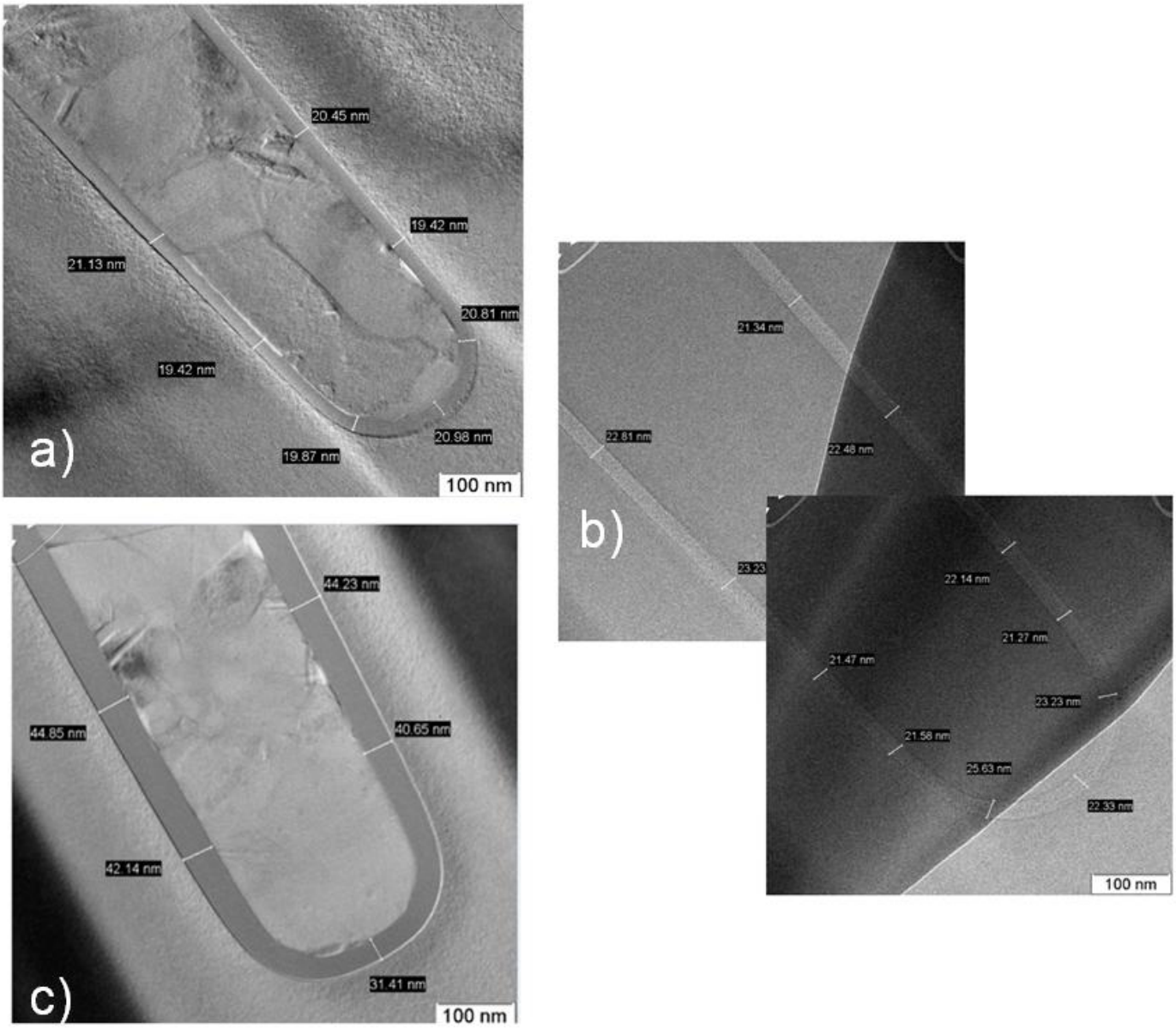

Figure 2A. (a) Dry oxidation for 200 Å, (b) Dry oxidation for target 250 Å, (c) Dry oxidation for target 500 Å

Supplementary Appendix 3

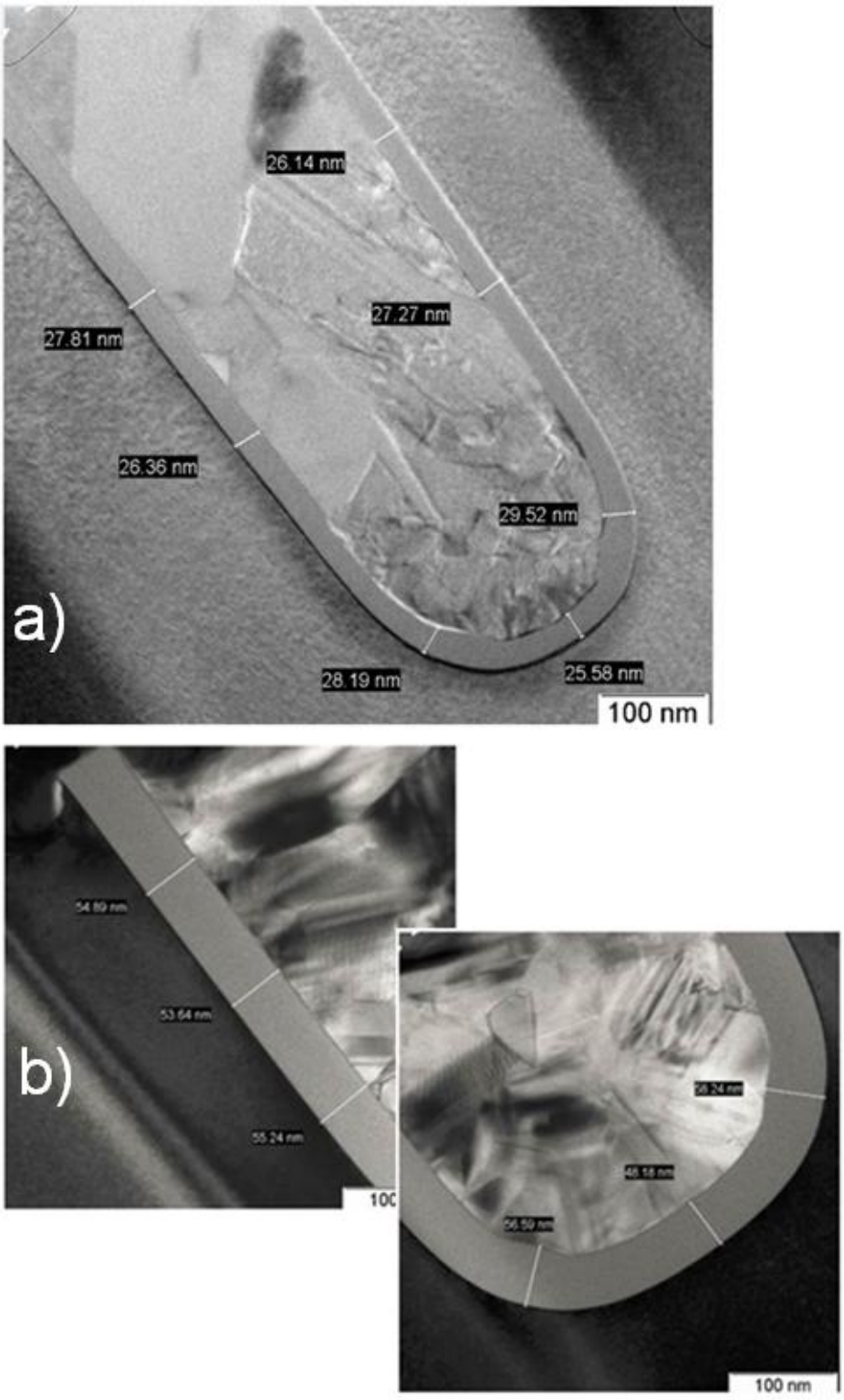

Figure 3A. (a) Dry oxidation (100Å) plus wet oxidation (150Å) total target 250Å, (b) Dry oxidation (100Å) plus wet oxidation (400Å) total target 500Å