UNIVERSITI MALAYSIA PERLIS
International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

Evaluate the impact of advanced cell pitch on U-MOSFET wafer edge I_{GSS} failure in a CMOS environment

Lee Boon Thuan [a,c]*, M.K. Md Arshad [b,c]*, and W.M.W Norhaimi[c]

[a]SilTerra Malaysia Sdn Bhd. Kulim Hi-tech Park, 09090, Kulim, Kedah.
[b]Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, Jln Kangar-Alor Setar, 01000, Kangar, Perlis, Malaysia.
[c]Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia
* Corresponding author. e-mail: mohd.khairuddin@unimap.edu.my, boonthuan@studentmail.unimap.edu.my, bt.lee@yahoo.co.uk

Received 30 August 2025, Revised 31 January 2026, Accepted 5 February 2026

ABSTRACT

Power MOSFET remains a key device platform in the semiconductor market demand, and this has drawn attention to SilTerra in the long-term supply chain, which provides additional manufacturing loading. In this work, the evaluation of the advanced cell pitch of a vertical trench MOSFET or U-MOSFET was selected due to its process compatibility in a CMOS fabrication environment. A major challenge was identified during the product ramping stage, exhibiting inconsistency for gate-to-source leakage (I_{GSS}) on the wafer edge across different production lots, along with trench Final Inspection Critical Dimension (FICD) and threshold voltage (V_{TH}) variation. Failure analysis revealed that affected I_{GSS} failure wafers have shown a wider trench critical dimension (CD) and misalignment between the contact and trench on the wafer edge. Inline containment activities were implemented on precise process control for trench final inspection critical dimension (FICD) and tighter alignment measurement in order to achieve stable I_{GSS}; however, this stringent inline process control has increased the rework rate. With the systematic trench mask development inspection critical dimension (DICD) split, it is confirmed that wider trench spacing or CD increases I_{GSS} failure at the wafer edge and overall V_{TH} variation; the optimal trench FICD control target is identified at 200 nm +/- 12 nm for stable I_{GSS} performance, and it is observed that CD bias between DICD and FICD is not at zero. To address the alignment mark issues, the layout structure was evaluated using technology computer-aided design (TCAD) simulation and tape-out for the experiment. The result of the new alignment has demonstrated a better process margin with the lowest I_{GSS} failure.

Keywords: *U-MOSFET, I_{GSS}, DICD, FICD, R_{DSON}, ASML alignment*

1. INTRODUCTION

The power electronics industry has become a mainstream segment in the global electronics market due to its long-term role in the supply chain for consumer products [1] [2] [3] [4], such as portable devices [5], energy conversion platforms for solar panels [6] [7], as well as e-bikes and e-vehicles [8]. Power MOSFET has come into the picture for its process compatibility in the CMOS wafer fabrication environment, and the focus in this publication is on vertical trench MOSFET, also known as U-MOSFET [9]. This is due to U-MOSFETs having an unique electrical characteristics such as low R_{DSON} and higher breakdown voltage when compared to traditional D-MOSFETs [10] [11] [12].

A significant design breakthrough for U-MOSFETs is the scaling of cell pitch below 1 µm using sophisticated lithography and etching techniques. The results of cell pitch reduction for high-density U-MOSFETs, which increase the channel density and reduce the specific on-resistance [13] [14]. In order to remain competitive in the market, the cell pitch design in this study is set up at 0.8 µm. One of the primary side effects of aggressive cell-pitch scaling in U-MOSFETs is wafer edge I_{GSS} failure. Table 1 summarizes the yield data for product A (PMOS 30V), highlighting how I_{GSS} failure correlates with trench final inspection critical dimension (FICD) and its impact on threshold voltage. It is clear that wider trench FICDs above 212 nm tend to have higher wafer edge I_{GSS} failures, as shown in Figure 1 and Figure 2. Observed that threshold voltage drifted with trench FICD variation due to MESA dimension and required redefining the body implants for channel length and optimizing the source implant to meet the device electrical characteristics [15].

Table 2 displays the cell pitch and FICD sizing for Product A, comparing the drawn layout to the final CD after the subsequent gate oxidation process step [16] [17] and the reference MESA CD is 0.45µm for a complete gate oxide with polysilicon deposition.

Figure 3 illustrates the MESA, or active silicon critical dimension (CD), at the cell region based on the I_{GSS} failure reference at the wafer edge from lot A and the lot B yield map. The MESA CD for lot A at the centre is 0.437 µm and edge 0.435 µm, and lot B's centre is 0.454 µm and edge 0.452 µm. This level of CD uniformity is generally acceptable within process control limits for the centre region; however, the deviation near the wafer edge has implications of I_{GSS} failure with abnormal contact misaligned to the trench. Such a deviation leads to gate-to-

source current leakage or I_{GSS} failure on the wafer edge since the contact profile has exceeded the silicon surface, which touches the gate oxide and polysilicon gate. The ASML mark structure validation for U-MOSFET technology is shown in Figure 4. It is observed that there are profile differences for centre to edge, and the contact-to-trench alignment mark trend shows high variation. The alignment system is operated based on the ASML alignment mark signal and will impact the overlay measurement performance [18] [19] [20].

Table 1. Product A (PMOS 30V) summary table

Lot	vid	Yield, %	I_{GSS}, %	Trench FICD, nm	V_{TH}, V	Remark
Lot A	1	96.7	2.4	212.1	-1.33	IGSS low
	2	84.9	14.6	221.2	-1.26	IGSS failure High
Lot B	1	99.0	0.5	196.6	-1.63	IGSS lowest
	2	98.5	1.0	197.2	-1.63	IGSS lowest
	3	98.8	0.8	197.0	-1.63	IGSS lowest
Lot C	1	87.0	12.9	211.9	-1.4	IGSS failure
	2	90.8	9.1	212.2	-1.4	IGSS failure
	3	92.0	7.9	211.3	-1.4	IGSS failure
Lot D	1	98.1	1.1	202.3	-1.7	IGSS lowest
						Body Implant dose adjust (VTH)

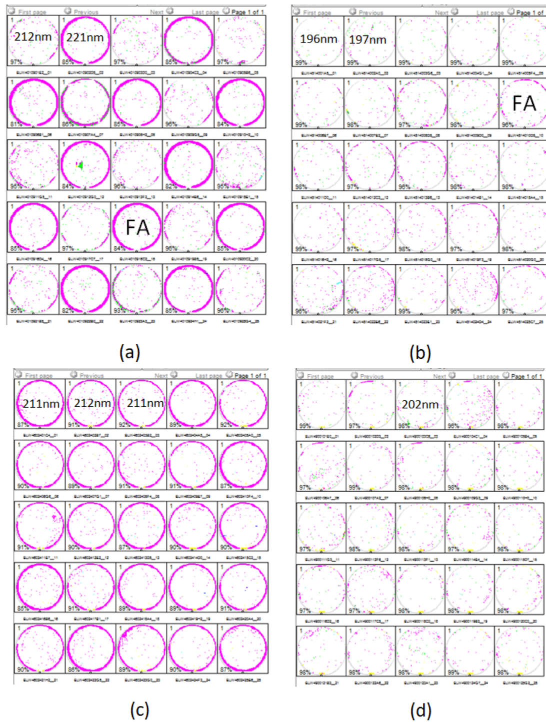


Figure 1. Product A yield map with various wafer I_{GSS} failure pattern on wafer edge in magenta colour (a) Lot A trench FICD 212.1 nm to 221.2nm, (b) Lot B trench FICD 196.6 nm to 197.2 nm, (c) Lot C trench FICD 211.3 nm to 212.2 nm, (d) Lot D trench FICD 202.3 nm

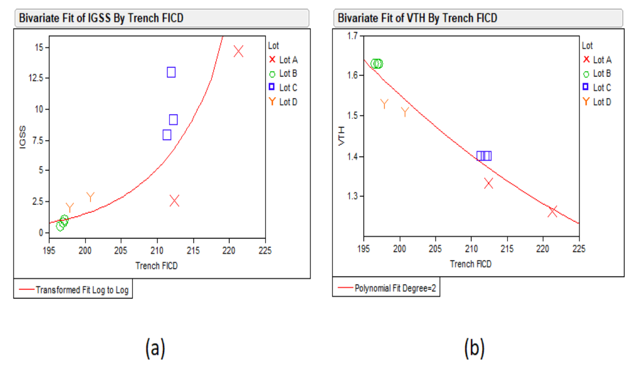


Figure 2. Product A trench FICD correlation (a) I_{GSS} trend by trench FICD trend (Space), (b) Threshold voltage (V_{TH}) by trench FICD trend (Space)

Table 2. Trench CD variation for cell pitch design 0.8μm

	Cell Pitch	Trench CD (SPACE)	MESA CD (Silicon)
Product A	0.8 µm	0.2 µm	0.6 µm
	800 nm	200 nm	600 nm
Oxidation1		250 nm	550 nm
Oxidation2		300 nm	500 nm
Gate Oxide		350 nm	450 nm

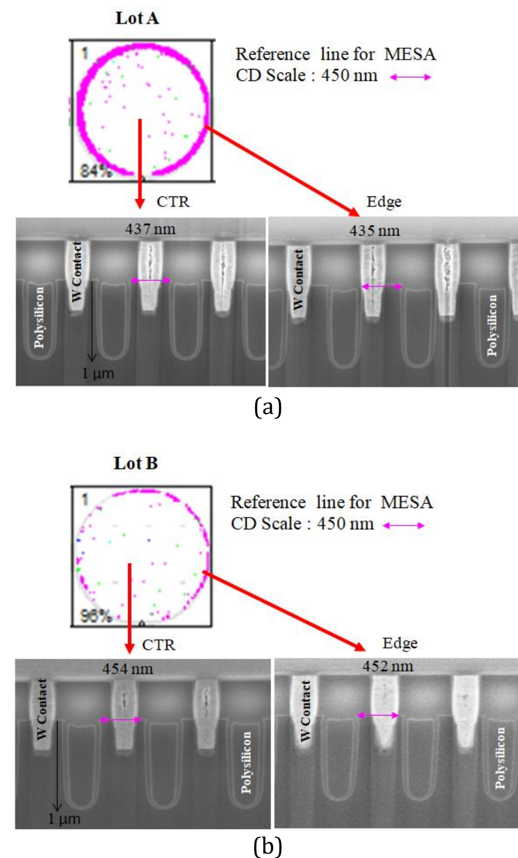


Figure 3. (a) Lot A cross-sectional profile of cell location on center and edge of the wafer, (b) Lot B cross-sectional profile of cell location on center and edge of the wafer

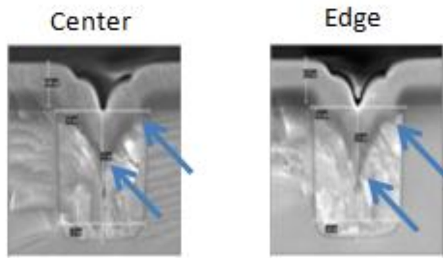


Figure 4. Cross sectional profile of ASML alignment mark (AH53 label I3) on center and edge of the wafer

2. MATERIAL & METHODS

2.1. The Wafer Map, Frame Layout, and Device Structure

The fabrication process of the vertical trench MOSFET (U-MOSFET) was carried out in detail to ensure device performance stability and reliability. Figure 5 illustrates the 8-inch wafer map employed for this product, while Figure 6 presents the reticle shot of the frame structure layout. The frame structure layout includes the following key elements: (a) frame layout, which comprises the main device chip and test element group (TEG). The TEG is designed for critical features such as the ASML alignment mark, registration mark (overlay), layer identification (ID), and critical dimension (CD) cell for process monitoring; (b) ASML alignment mark, the mark enables precise alignment between photolithography layers, particularly for critical layers such as contact and trench formation in this case, ensuring device consistency across the wafer [21] [22]; (c) overlay box, used for accurate overlay measurements between two mask layers in order to verify lithographic alignment tolerance and process control [23] [24].

Additionally, Figure 7 depicts the complete U-MOSFET cross-sectional structure; the terminal connections for source, gate, drain, and termination ring are clearly defined and correlated with the device's top-view layout. This structure representation ensures a comprehensive understanding of the device architecture and facilities' correlation between design and fabricated structure.

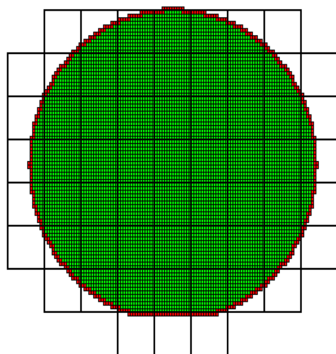
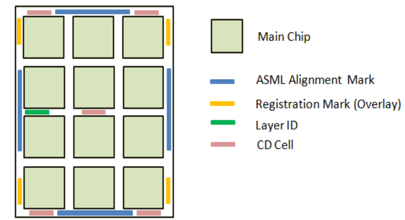
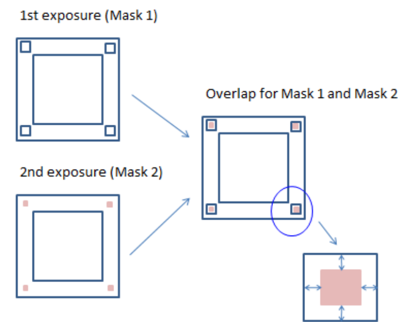


Figure 5. 200mm (8 inches) wafer map



(a)

(b)



(c)

Figure 6. (a) Frame structure layout for one reticle shot with test key option, (b) ASML Alignment mark structure (c) Overlay Box-in-Box structure for two layers

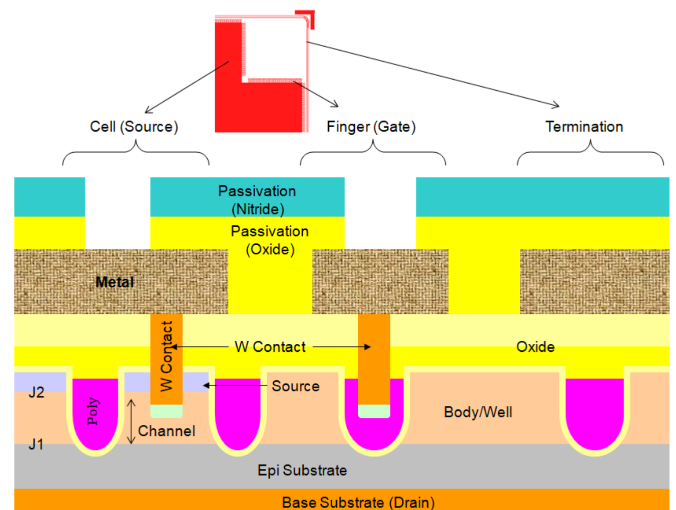


Figure 7. Cross-sectional structure view of U-MOSFET with each terminal connection points

2.2. Inline Process Control for Trench FICD and Contact-to-Trench Alignment Mark

In this session, we focus on the control plan from inline measurement to process control plan and trench CD split as the initial stage of wafer edge IGSS failure containment.

Figure 8 illustrates the flow chart of trench FICD target and contact mask alignment control. Inline measurement control of trench critical dimension (CD) was performed using high-resolution critical dimension scanning electron microscopy (CD-SEM) from KLA-Tencor. Measurements were taken at cell locations, including the center, edge, and intermediate points, to accurately monitor across-wafer CD variations from develop inspection critical dimension (DICD) to FICD. Followed by contact to trench alignment measurement control, the overlay between the contact and trench layers was evaluated by measuring positional shifts in both the x and y directions. Alignment targets and control limits were set according to design rules, and any deviations detected were corrected using tool feedback mechanisms from +/- 50nm to +/- 30nm. Maintaining the precise contact-to-trench alignment was crucial to ensure stable I_{GSS} electrical performance and overall yield stability.

Process control strategies were established to maintain the consistency of trench FICD and ensure accurate contact to trench alignment performance, as shown in Figure 9 and Figure 10 for a better trench profile control. The trench module process sequence film stack from Figure 9 illustrates the final trench profile formation, beginning with the Trench-Mask, followed by Trench-Ox-Etch and Trench-Si-Etch. Figure 10 presents the contact module process sequence film stack, which defines the contact profile formation and alignment to the underlying trench structures, and it starts with Contact-Mask to Contact-HM-Etch and Contact-Si-Etch. Each process stage was closely monitored and optimized accordingly using the predefined input-output variables to ensure trench FICD consistency and contact-to-trench alignment accuracy.

The stringent inline process control monitor involves trench etch process equipment tool parametric factors, such as Radio Frequency (RF) hours and Electro-Static-Chuck (ESC) gas flow rates; this is to determine how well the trench FICD can be controlled or sustained. Figure 11 displays the trench etch process tool parameters factor based on actual inline trench FICD and yield performance; (a) the prediction profiler illustrates the influence of key process variables, which impact the yield drop towards larger trend FICD, which was due to higher ESC RF hours usage and supported by higher ESC gas flow rates, which means the degradation of the ESC chuck is a key factor of trench FICD drift over the cycle of process equipment life count. (b) The cube plot provides a visualization of the combination effects of the trench FICD, ESC RF hours, and ESC gas flow rates based on yield variables. The cube plot facilitates a clear comparison response to different factor settings and is imposed by the hardware constraint, which provides valuable insights into process optimization by real-time data trend consolidation setup for proper process control.

To explore how trench width or CD bias influences device performance, we introduced three process splits with controlled variations in Trench Mask DICD. As shown in Table 3, each split was systematically configured by the photolithography process dose factor. Split A is the process of record (POR), with DICD target at 200 nm. Split B, DICD, was set to a wider target at 210 nm, while Split C introduced the largest DICD target at 240 nm. The trench etch FICD will be the final target for the inline validation study for I_{GSS} failure. This systematic approach enabled us to evaluate the influence of trench geometry on subsequent process behavior such as contact-to-trench alignment performance on the current ASML alignment mask test key.

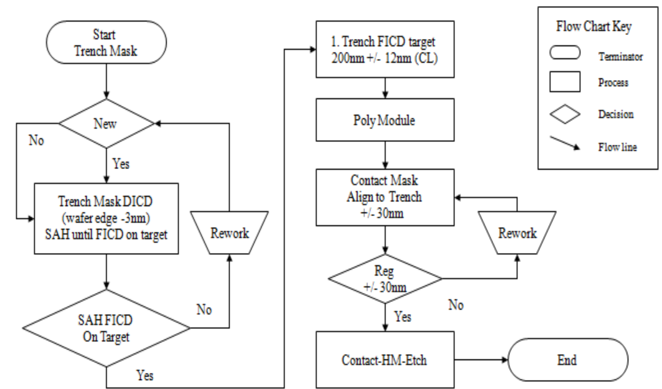


Figure 8. The flow chart of trench CD control and contact to trench alignment control

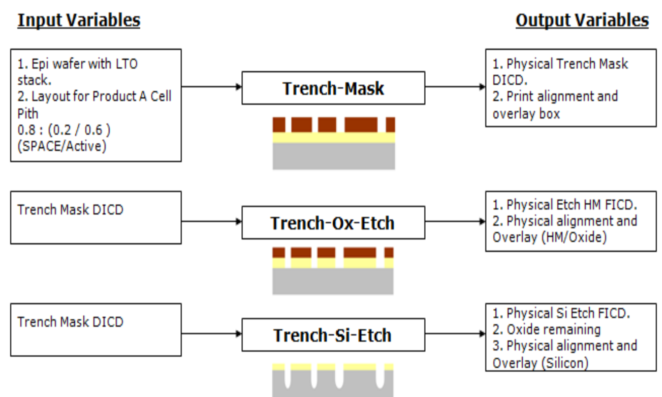


Figure 9. Trench module process module sequence film stack

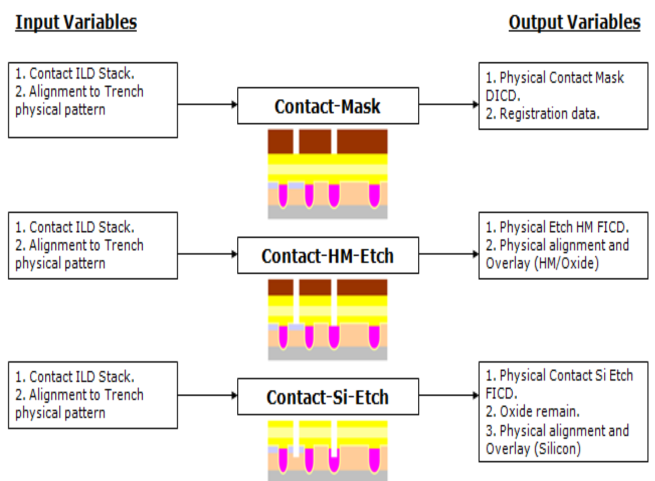
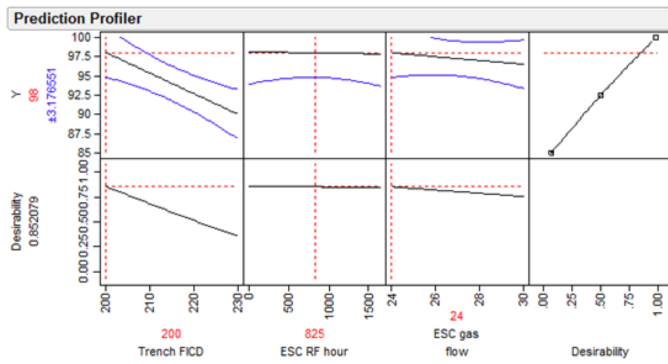
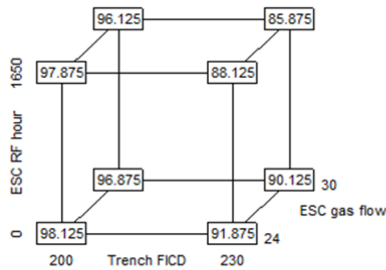


Figure 10. Contact module process sequence film stack



(a)



(b)

Figure 11. Trench etch process equipment tool parametric factor (a) Prediction profiler based on inline data trend and hardware limitation, (b) Cube plot based on inline data trend and hardware limitation

Table 3. Trench Mask DICD split (Space)

Process Step	Condition	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Trench Mask	Split A : 200nm	O				O		O		O		O		O		O		O		O		O		O		O
	Split B : 210nm		O				O		O		O		O		O		O		O		O		O		O	
	Split C : 240nm			O	O																					

2.3. Alignment Structure Layout Structure Design

The ASML alignment mark is used in semiconductor manufacturing for precise optical reference during photolithography; it optimizes overlay correction across wafers and can be segmented into full bar marks, segmented bars, grating structures, and tri-segmented or multi-segmented patterns, as shown in Figure 16. The fabrication of the trench mask reticle with the ASML alignment mark included designing the mark and trench shapes with CAD software (Cadence), putting the pattern onto the chrome layer, and checking that the alignment mark sizes were accurate. The reticle was then qualified using an ASML scanner and simulation of wafer printing to confirm alignment functionality under production conditions, and Table 4 summarizes the alignment mark space-line by segmentation according to ASML design requirements with newly modified sizing of 0.6 µm / 0.4 µm by naming it AH53S on the label (I13S). Each alignment mark structure, represented in Figures 13 through 17, was verified within its respective segmentation category. The layout structures were subsequently integrated into a unified frame structure for deployment, as shown in Figure 18. This is to make sure it worked well with regular ASML scanner operations and set the stage for comparing how effective the new segmentation is at fixing overlay error.

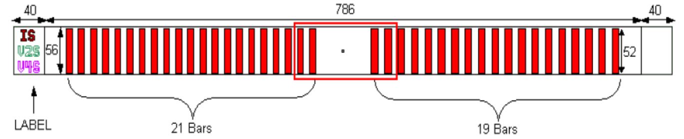


Figure 12. ASML alignment mark layout structure and overall size

Table 4. Alignment mark summary list for space and line by segmentation

Alignment Mark Label	Space / Line, µm	Remark
CMOS ASML test key Label (IS)	8 / 8	Simulation on SILVACO (Existing Alignment mark reference)
AH13 ASML test key Label (I2)	2.6 / 2.8	Simulation on SILVACO (BKM alignment mark to drop in new tape out)
AH53 ASML test key Label (I3)	1.6 / 1.6	Simulation on SILVACO (Existing Alignment mark for Product A)
AH14 ASML test key Label (I4)	1.15 / 1.15	Simulation SILVACO (BKM alignment mark to drop in new tape out)
AH53S (Modify) Label (I3S)	0.6 / 0.4	Simulation on SILVACO (To draw in cadence and drop in new tape out)

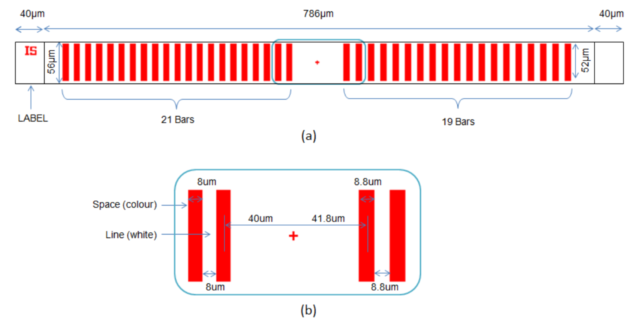


Figure 13. ASML segmentation (a) Alignment mark structure CMOS label (IS), (b) Original segmentation

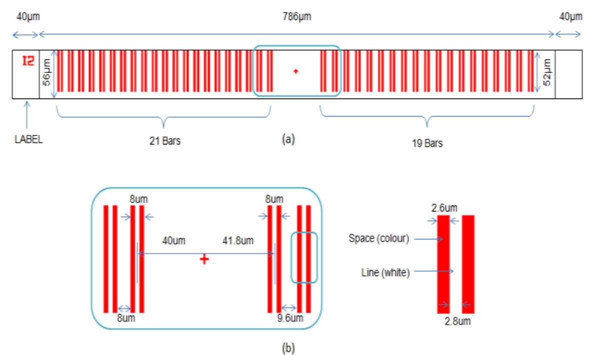


Figure 14. ASML segmentation (a) Alignment mark structure AH13 label I2, (b) Segmentation split into 2 bars

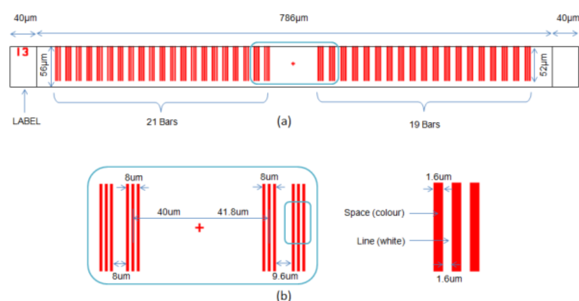


Figure 15. ASML segmentation (a) Alignment mark structure AH53 label I3, (b) Segmentation split into 3 bars

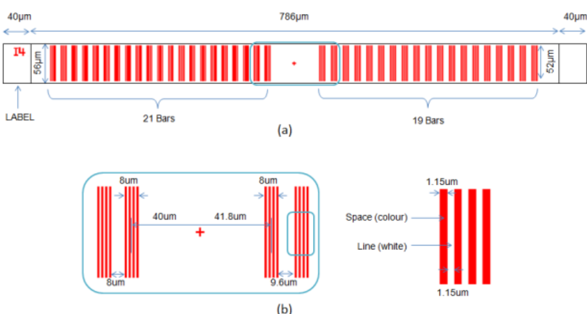


Figure 16. ASML segmentation (a) Alignment mark structure AH14 label I4, (b) Segmentation split into 4 bars

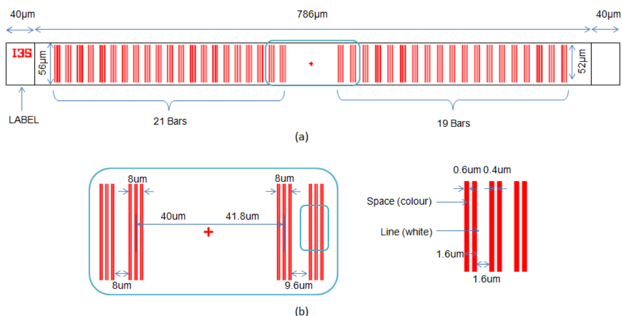


Figure 17. ASML segmentation (a) Alignment mark structure AH53S label I3S, (b) Segmentation split into 6 bars

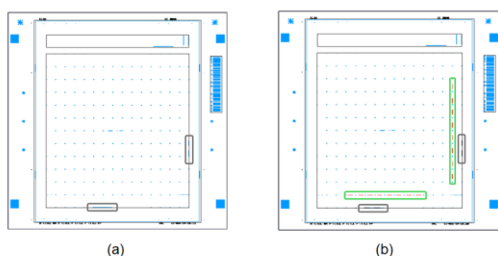


Figure 18. Frame structure (a) original trench mask reticle set, (b) new trench mask reticle set with additional alignment mark segmentation

3. RESULT & DISCUSSION

3.1. I_{GSS} Performance from Inline Process Control and Trench CD Split

Figure 19 presents the result of the trench module inline process control: (a) the trench FICD trend chart and (b) the IGSS trend chart based on inline E-test. The trend chart data was grouped into four distinct stages along the initial production ramping cycle.

The first stage was the initial performance of the trench FICD 200 nm +/- 30 nm spec limit (SL) and having high trench FICD fluctuation, which impacted the IGSS performance. Due to the wafer edge alignment limitation, the wafer edge IGSS failure has shown sensitivity to higher trench FICD spacing as mentioned in Figure 3 (a) and Figure 3 (b). Moving into the second stage, the IGSS performance improved because the trench FICD spec limit tightened to 200 nm +/- 20 nm and used the DICD feedback as a closed-loop function; however, the trench FICD changed over time, and we found out that this was due to hardware issues from the process tool during stage three, which we rectified during our investigation, as illustrated in Figure 19. And at stage four, the new trench FICD inline control was implemented to a 200 nm +/- 12 nm control limit (CL) to minimize the I_{GSS} failure. This adjustment has resulted in significant improvements in IGSS and enhanced overall yield performance; however, it also affected manufacturability, leading to an increased rework rate for the trench mask in order to maintain the trench FICD at 200 nm. This outcome highlights the trade-off between yield stability from stringent inline control and higher cost expenses due to an increase in rework rate.

Table 5 summarizes the impact of the trench module CD split on key performance data which focuses on yield, I_{GSS} and V_{TH}. The data clearly shows that trench CD split and I_{GSS} behavior are directly correlated. Wider trench CD spacing tends to show higher wafer edge I_{GSS} failure, as illustrated in Figure 20. From the DICD 240 nm group, it shows massive wafer edge I_{GSS} failure from 27.9% to 34.3%. Next, the DICD 210 nm group's shows IGSS at 9.7%, and the DICD 200 nm group I_{GSS} performance is at 4.6%, which still has a mild wafer edge ring pattern. To ensure consistent yield and reduce I_{GSS} failure, trench FICD needs to be tightly controlled – ideally targeted at 200 nm. This specific target helps achieve stable device performance; however, reproducibility will affect manufacturing capacity, especially at a high rework rate.

Besides I_{GSS} failure, trench FICD also influences the V_{TH} performance; it has been experimentally demonstrated by Y. Baba (et al) [25], the variation in trench dimensions can alter the U-MOSFET channel characteristic. This can be fixed by making changes to the body and source implant to define a functioning U-MOSFET channel length.

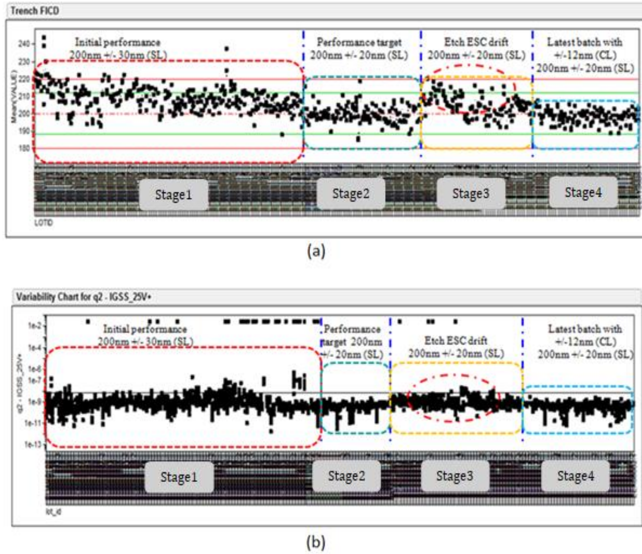


Figure 19. Trench module inline control chart (a) trench FICD trend, (b) E-test I_{GSS} performance trend from production ramping cycle

Table 5. Summary table for trench module CD split

No	Trench Mask DICD, nm (Space)	Trench Etch FICD, nm (Space)	Yield, %	I_{GSS}, %	V_{TH}, V
1	200	204	94.2	4.6	-1.307
2	210	214	86.3	9.7	-1.225
3	240	243	49.1	34.3	-1.022
4	240	238	57.5	37.9	-1.056

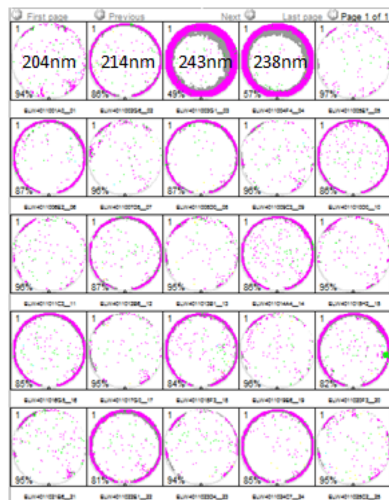


Figure 20. Trench module CD experiment yield map with FICD data

3.2. I_{GSS} Performance from Inline Process Control and Trench CD Split

Table 6 presents a comparative evaluation of the ASML trench alignment marks using both Cadence layout design and TCAD process simulations (Silvaco). The simulation incorporated feature scaling and segmentation effects on critical dimension (CD) widths. Among the evaluated configurations, the newly developed AH53S test key exhibited superior performance compared to the existing AH53 structure, which currently serves as the process-of-record (POR) alignment mark for vertical trench MOSFET or U-MOSFET applications. The cross-sectional profiles of ASML test keys demonstrated strong agreement with the TCAD simulation results, confirming the accuracy of each segmentation modeled structure.

Figure 21 summarizes the normalized overlay data across different ASML alignment mark segmentation designs; the overlay data define the uniformity and precision of wafer quality signal, which reflects the accuracy of ASML alignment mark segmentation. AH53S exhibited the best alignment performance on reduction of overlay to approximately 0.25 µm. With this optimized geometry, it helps to improve the structure loading effect of the profile after polysilicon etch compared with AH53 (POR) at 0.5 µm and AH14 slightly above 0.27 µm. The standard CMOS alignment mark was used for baseline study purposes and has shown high normalized overlay data around 0.75 µm; this is due to wider segmentation, causing the polysilicon etch loading effects on the trench structure and impacting the ASML wafer quality (WQ) signal. The normalized overlay data for the AH13 alignment structure hit almost 1.5 µm and observed an unusual void on the ASML physical profile.

Based on these results, the AH53S alignment mark structure was chosen as the main test key for future process development and prototyping. It is expected that its use will make lithographic processes more robust and the whole process more reliable in the production of advanced trench MOSFETs. AH53S does a great job of reducing distortion caused by the process variation and making alignment to overlay better.

Table 6. Trench alignment mark cross-sectional profile comparison by segmentation

Location	Standard CMOS (IS) 8 / 8	AH13 (I2) 2.6 / 2.8	AH53 POR (I3) 1.6 / 1.6	AH14 (I4) 1.15 / 1.15	AH53S (I3S) 0.6 / 0.4
Alignment Mark Segmentation (Cadence)	8.8um 8.8um	2.6um 2.8um	1.6um 1.6um	1.15um 1.15um	0.6um 0.4um
TCAD Simulation (SILVACO)					
Cross-Section Center					
Cross-Section Edge					

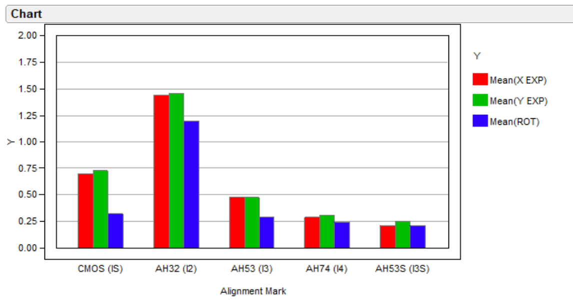


Figure 21. Normalized overlay data by ASML alignment mark segmentation

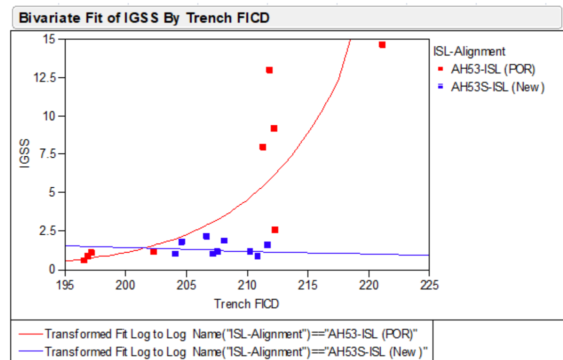


Figure 22. Normalized overlay data

3.3. I_{GSS} Performance from Inline Process Control and Trench CD Split

Table 7 summarizes the overall leading lot performance of the new alignment mark (AH53S); the table displays the yield, gate source leakage current (I_{GSS}), trench FICD and threshold voltage (V_{TH}) with the latest body implant adjustment for device matching purposes

Figure 22 summarizes the combination data from table 1 and table 7; the average yield performance for the new alignment mark (AH53S) is stable from 97.8% to 98.8%, and the I_{GSS} performance is well within 0.9% to 2.1%; even the trench FICD performance range is from 204.1 nm to 211.7 nm. It shows that the new alignment mark (AH53S) test key has a better margin; the POR alignment mark (AH53) starts showing high I_{GSS} failure with trench FICD above 210 nm. Threshold voltage (V_{TH}) value ranging from 1.78 V to 1.93 V, which is within the expected process window and the V_{TH} retarget, can be achieved by the body implant dose adjustment to match the device function.

Figure 23 displays the yield map fabricated using the new alignment mark (AH53S); the wafer map is clear without the wafer edge I_{GSS} pattern, even with the trench FICD process at a higher control limit.

Table 7. Summary table for new alignment mark (AH53S)

Lot	vid	Yield, %	I_{GSS}, %	Trench FICD, nm	V_{TH}, V	Remark
Lot F	2	98.2	1.1	207.6	-1.82	V_{TH}, adjustment by body implant dose
Lot F	3	98.6	0.8	210.9	-1.86	
Lot G	1	97.9	1.8	208.1	-1.93	
Lot G	2	98.8	1.1	210.3	-1.86	
Lot G	3	98.2	1.5	211.7	-1.89	
Lot H	1	97.8	2.1	206.7	-1.88	
Lot H	2	98.1	1.7	204.6	-1.81	
Lot H	3	98.8	0.9	207.2	-1.76	
Lot I	3	98.7	0.9	204.1	-1.78	

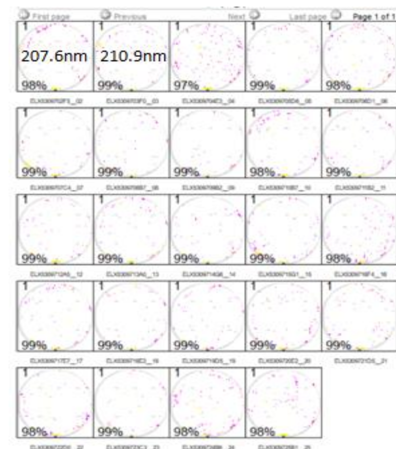


Figure 23. Product A yield map with new alignment mark (AH53S) from Lot F

4. CONCLUSION

This study has presented precise control of trench FICD, and tighter alignment measurement for contact-to-trench is essential to achieve stable yield performance and minimize I_{GSS} failures, particularly at wafer edges. The systematic trench mask DICD split confirmed that wider trench spacing directly increases I_{GSS} at the wafer edge, with the optimal control target identified at ~200 nm ± 12 nm. Stringent inline process monitoring and closed-loop feedback significantly reduced variability; however, it increased the trench mask and contact mask rework rates. The introduction of the newly designed ASML alignment mark (AH53S) has shown improvement of overlay accuracy, which enhanced the wafer quality signal strength compared to the POR alignment mark (AH53) and reduced the I_{GSS} failure within (~2%) from process variation to achieve stable yield (~98%). The AH53S test key has shown robustness in yield stability even with variation of trench dimensions to higher control (> 212 nm). Overall, the integration of optimized trench FICD control with the new alignment mark design establishes a more reliable and

reproducible process window for advanced vertical trench MOSFET (U-MOSFET) fabrication, ensuring better electrical performance, yield stability, and scalability for future generations of power devices. Additional process optimization on the body implant was carried out for threshold voltage (V_{TH}) device matching due to trench CD variation.

ACKNOWLEDGMENTS

The authors sincerely acknowledge Universiti Malaysia Perlis (UniMAP) and SilTerra for their valuable support and for providing the materials used in the research.

REFERENCES

[1] K. B. V. Research, "Global Power Semiconductor Market Size, Share & Industry Trends," 2023. [Online].Available:https://www.kbvresearch.com/power-semiconductor-market/.

[2] W. ELEKTRONIK, "Power Electronic News," no. August,2024,[Online].Available:https://www.powerelectronicsnews.com/galvanic-isolation-and-wbg-semiconductors-enhance-industrial-efficiency/%0A.

[3] A. Yoo, "Design, Implementation, Modeling, and Optimization of Next Generation Low-Voltage Power MOSFETs," University of Toronto, 2010.

[4] H. Choi, "Technology-push, demand-pull and spillover from the major market demand: The case of the United States wind power market," *Technol. Soc.*, vol. 79, no. August, p. 102684, Dec. 2024, doi: 10.1016/j.techsoc.2024.102684.

[5] T. Ogura, "Recent technical trends and future prospects of IGBTs and power MOSFETs," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 2068–2073, doi: 10.1109/IPEC.2014.6869872.

[6] P. L. Hower, S. Pendharkar, and T. Efland, "Current status and future trends in silicon power devices," in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 13.1.1-13.1.4.

[7] D. E. Berg, "Energy Conversion," *Energy Conversion, Second Ed.*, no. Mvd, pp. 851–895, Jul. 2017..

[8] K. Hussein, A. Fujita, and K. Sato, "Trend in power devices for electric and hybrid electric vehicles," in *The 20th Asia and South Pacific Design Automation Conference*, Jan. 2015, no. 1, pp. 416–416.

[9] M. Lotfi and D. Zohir, "Modeling and Simulation of Power MOSFET Using Orcad-Pspice," *Int. J. u- e-Serv. Sci. Technol.*, vol. 9, no. 9, pp. 37–44, Sep. 2016.

[10] I. T. AG, "Some key facts about avalanche," 2017. [Online]. Available: www.infineon.com.

[11] D. A. G. and J. Gowar, *Power MOSFETS: Theory and Applications, John Wiley and Sons*, 1st ed. Bristal, United Kingdom: John Wiley & Son, 1989.

[12] B. V. Barkhordarian, I. Rectifier, and E. Segundo, "Power MOSFET Basics," 2005. [Online]. Available: https://web.how2power.com/article/2005/october/power-mosfet-basics.php.

[13] S. A. Suliman *et al.*, "The impact of trench geometry and processing on the performance and reliability of low voltage power UMOSFETs," in *2001 IEEE International Reliability Physics Symposium Proceedings. 39th Annual (Cat. No.00CH37167)*, 2001, vol. 2001-Janua, no. February, pp. 308–314.

[14] K. Kobayashi, A. Kaneko, Y. Murase, and H. Yamamoto, "Sub-micron Cell Pitch 30 V N-channel UMOSFET with Ultra Low On-resistance," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, May 2007, pp. 205–208.

[15] F. O. Dainese *et al.*, "Behavior Investigation of trench-gate and vertical diffusion power MOSFET," *SBMicro*, vol. 14, 2014, [Online]. Available: https://sbmicro.org.br/eventos/sforum/volume-14.

[16] B. E. Deal and A. S. Grove, "General relationship for the thermal oxidation of silicon," *J. Appl. Phys.*, vol. 36, no. 12, pp. 3770–3778, 1965.

[17] V. Šimonka, A. Hössinger, J. Weinbub, and S. Selberherr, "Growth rates of dry thermal oxidation of 4H-silicon carbide," *J. Appl. Phys.*, vol. 120, no. 13, 2016.

[18] P. Samudrala *et al.*, "Alignment solutions on FBEOL layers using ASML scanners," in *SPIE Advanced Lithography*, Mar. 2017, p. 101471T.

[19] N. Ahmad, U. Hashim, M. J. Manaf, and K. I. Abdul Wahab, "Alignment Mark Architecture Effect on Alignment Signal Behavior in Advanced Lithography," in *2006 IEEE International Conference on Semiconductor Electronics*, Nov. 2006, vol. 2, no. 1, pp. 732–739.

[20] J. Huijbregste *et al.*, "Overlay performance with advanced ATHENA alignment strategies," in *Metrology, Inspection, and Process Control for Microlithography XVII*, May 2003, vol. 5038, p. 918.

[21] D. M. Qiu Jun, Yang Guanghua, Li Jing , Lu Zengxiong, "Development and Challenges of Lithographical Alignment Technologies," *Acta Opt. Sin.*, vol. 43, no. 19, p. 1900001, 2023.

[22] C. K. Tew, L. Y. M. Tobing, J. O. Yoo, and N. Singh, "Investigation of Immersion Alignment Mark Signal and Alignment Success Rate for Flat Optics with Aperture on Chip," in *2023 IEEE 25th Electronics Packaging Technology Conference (EPTC)*, Dec. 2023, pp. 592–595.

[23] B. Yan *et al.*, "Frame mark selection, placement, design and simulation," in *2022 International Workshop on Advanced Patterning Solutions (IWAPS)*, Oct. 2022, pp. 1–4.

[24] S. H. Lee, K.-N. Chen, and J. J.-Q. Lu, "Wafer-to-Wafer Alignment for Three-Dimensional Integration: A Review," *J. Microelectromechanical Syst.*, vol. 20, no. 4, pp. 885–898, Aug. 2011.

[25] Y. Baba and I. Omura, "Effect of cell size reduction on the threshold voltage of UMOSFETs," *Microelectron. Reliab.*, vol. 114, no. May, p. 113747, Nov. 2020.