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Characteristics prediction of sub-5 nm nanosheet field effect transistor (FET) using a machine learning approach

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ABSTRACT

The field-effect transistor (FET) is a vital component in various electronic devices, including integrated circuits (IC_S), switching modules, and microprocessors. The current technological breakthroughs have enabled the development of N5 (5 nm node) technology for fabricating transistors. Before the production of transistors, it was crucial to engage in modelling and simulation to reduce costs and save time. Hence, developing a methodology for predicting transistor characteristics is essential for minimizing expenses and time in advancing transistor technology. Machine learning (ML) enables data-driven modeling of complex nonlinear systems to gain knowledge and enhance their performance without explicit programming. ML trains machines to optimize the processing and understanding of data. Researchers have conducted several studies to enable ML to acquire knowledge without explicit autonomous programming. However, the previous ML model achieved a coefficient of determination (R^2) of only 0.98, or 98%. Here, we report on the use of Technology Computer-Aided Design (TCAD) to generate a dataset that achieves a high predictive performance. The Nanosheet Field-Effect Transistor (NSFET) can be modified by adjusting five essential factors: Gate Length (L_g), Sheet Width (F_w), Sheet Height (F_h), Spacer Length (L_{sp}), and equivalent oxide thickness (e_{ot}). An Artificial Neural Network (ANN) is used to forecast various features of NSFET, including Threshold Voltage (V_T), Off-State Current (i_{off}), Saturation Current (i_{sat}), and Subthreshold Swing (ss_{lop}). The results indicate that the ANN model accurately predicts NSFET properties, yielding an R^2 value of 0.9915 indicating strong correlation within the simulated dataset.

Keywords: *Nanosheet Field Effect Transistor, Artificial Neural Network, Technology Computer-Aided Design*

1. INTRODUCTION

Electronic devices can now be miniaturized to the nano-scale, as opposed to their previous size, which was limited to the micro-scale. A Field-Effect Transistor (FET) is an electrical device that functions as a capacitor, with one plate acting as a conducting channel connecting two ohmic contacts and source and drain electrodes [1]. A FET serves as the primary element in a wide range of electronic devices, including Integrated Circuits (IC_s), switching modules, and microprocessors. Based on recent improvements in node technology, the transistor fabrication technique has successfully reached N5 technology, corresponding to a node size of 5 nanometers. In the future, device fabrication technologies will be miniaturized to match existing standards. Transistors are essential in telecommunications, facilitating rapid data transmission in 5G technology. They are also employed in military applications, such as radar systems [2].

Before fabricating transistors, it is essential to undertake the process of modeling and simulating transistors to reduce costs and save time [3]. Another researcher used software simulation to fabricate a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [4]. The results indicated that the use of simulation significantly reduced the number of necessary steps and resulted in cost reductions in the production process. Machine Learning (ML) is an academic discipline that enables computers to acquire knowledge and improve their performance without the need for explicit programming. ML is a field that focuses on training machines to efficiently process data and extract valuable insights from it [5].

Several research groups have utilized ML to generate predictions regarding electronic devices [6]. Their research utilized a Neural Network (NN) to simulate MOSFETs. Another researcher utilized an Artificial Neural Network (ANN) to model a laterally diffused Metal-Oxide Semiconductor (LDMOS) [7]. Another researcher employed an ANN to demonstrate a conceptual framework for a Memristor [8]. Other studies have used ANN to forecast the performance of Fin-shaped Field-Effect Transistors (FinFET) [9]. ANN to predict the efficiency of Line Edge Roughness (LER) on FinFET [10]. Mehta and Wong employed an Auto Encoder to predict the I-V

(current-voltage) and C-V (capacitance-voltage) characteristics of FinFETs [11]. ANN to predict the I-V and C-V characteristics of Nanosheet Field-Effect Transistors (NSFET) [3]. Another report utilized a Multi-layer Neural Network to predict the characteristics of NSFETs [12]. However, all the studies mentioned above consistently produce ML models with an R^2 of less than 0.98 or 98%.

Herewith, we report the utilization of an ML to predict the properties of NSFET with a high level of accuracy, surpassing 0.98. Similar performance can be achieved by optimizing network architecture, such as modifying the layers used and replacing the architectural model. The Synopsys Sentaurus TCAD software, combined with Python programming, is used to design and run simulations of ML models.

2. RESEARCH DESIGN

2.1. NSFET Design and Parameters

The NSFET structure used in this study is adapted from the design reported by Kurniawan et al. (2021), as illustrated in Figure 1 [13]. In this work, the structure is reconstructed in the simulation environment with explicitly defined material regions, including Silicon (Si) for the channel and source/drain, Silicon Dioxide (SiO_2) as the gate dielectric, Oxide as the isolation layer, and Nitride as the spacer, representing a standard nanosheet field-effect transistor (NSFET) configuration for sub-5 nm technology analysis [14].

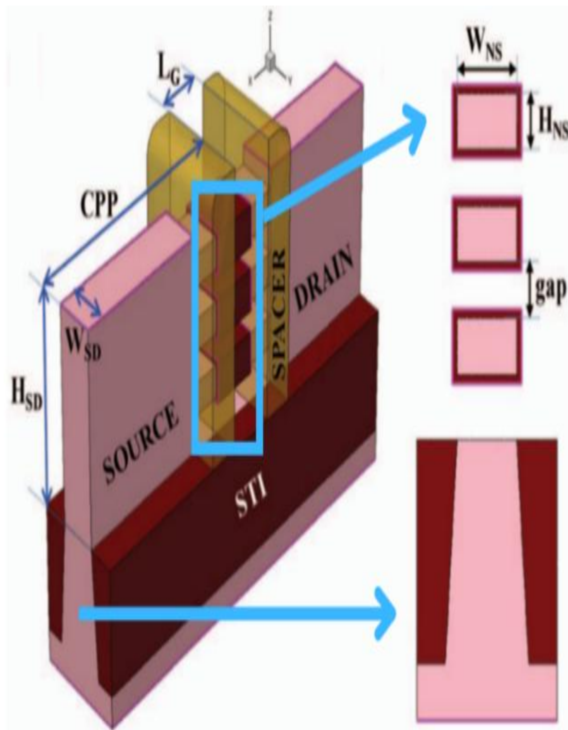

Figure 1. A schematic design of NSFET [13]

The geometrical and electrical parameters presented in Table 1 are adopted directly from Kurniawan et al. (2021) and serve as the baseline configuration in this work [13].

Table 1. Key parameters of the NSFET for simulation

Parameters	Value	Unit
Gate Length (L_g)	12	nm
Gate Pitch (CPP)	44	nm
Spacer Length (L_{sp})	8	nm
NS Height (F_h)	5	nm
NS Width (F_w)	10	nm
NS Channel gap (gap)	5	nm
Equivalent Oxide Thickness (e_{ot})	0.8	nm
S/D Height (H_{SD})	30	nm
S/D Width (W_{SD})	10	nm
Operating Voltage (V_{DD})	0.65	V
Channel Doping (N_{CH})	1×10^{17}	cm^{-3}
S/D Doping (N_{SD})	1×10^{20}	cm^{-3}
Gate Work Function (*WF*)	4.466	eV

The device design is created using the Sentaurus Structure Editor (SDE) within the Sentaurus Workbench. The design procedure is divided into three main stages. Firstly, the device geometry is constructed, and the contact regions, including the source, drain, and gate, are defined. Secondly, material doping is applied using Boron and Arsenic active concentrations in the appropriate areas [14]. Finally, the device is meshed and simulated for further electrical analysis.

2.2. Simulation Setup

The simulation is conducted using Sentaurus Workbench. The tools utilized in this study comprise Sentaurus Structure Editor (SDE), Sentaurus Mesh (SNMesh), Sentaurus Device (SDevice), and Inspect. Five key geometric parameters: Gate Length (L_g), Nanosheet Width (F_w), Nanosheet Height (F_h), Spacer Length (L_{sp}), and Equivalent Oxide Thickness (e_{ot}) are considered in this study due to their critical role in determining device performance. These parameters significantly influence electrostatic control, short-channel effects, and current conduction in nanosheet transistors [3]. To implement the simulation, each parameter is systematically varied while all other conditions are held constant, ensuring a comprehensive analysis of the device's behavior. The specific values for these parameters are listed in Table 2, which are adopted from Woo et al. (2021) [3]. The resulting simulation data are then used as a dataset for training the ML model.

Table 2. The optimization of the NSFET data sets

Parameters	Value	Unit
Gate Length (L_g)	11, 12, 13	nm
NS Width (F_w)	21, 23, 25, 27, 29	nm
NS Height (F_h)	4, 5, 6	nm
Spacer Length (L_{sp})	3, 4, 5	nm
Equivalent Oxide Thickness (e_{ot})	1, 1.5, 2	nm

2.3. Machine Learning (ML) Design and Modeling

The process of designing an ML model starts by identifying the problem to be addressed, which in this case is a regression task aimed at predicting key device

characteristics of nanosheet transistors based on five geometric parameters: L_g, F_w, F_h, L_{sp}, and e_{ot}. Once the model type is determined, data collection is conducted through TCAD simulations, generating a dataset of 405 distinct transistor configurations, including I-V and C-V characteristics, to ensure comprehensive coverage of the parameter space. The input features are standardized to facilitate stable and efficient learning, and the dataset was partitioned into training and testing subsets using an 80:20 ratio. Given that the dataset was generated through parametric sweeps, care was taken to randomize the data before splitting to minimize potential data leakage.

An Artificial Neural Network (ANN) is employed due to its ability to model complex non-linear relationships between the geometric parameters and device characteristics of NSFET. Inspired by early brain sensory processing, ANNs emulate networks of artificial neurons that can learn from data and solve a wide range of problems. In this study, the ANN architecture consists of four layers: an input layer, one or two hidden layers, and an output layer. The model used ReLU activation with Adam optimizer, trained for 100 epochs with early stopping. The input layer comprises five neurons corresponding to the five geometric parameters: gate length (L_g), sheet width (F_w), sheet height (F_h), spacer length (L_{sp}), and equivalent oxide thickness (e_{ot}). The number of neurons in each hidden layer is automatically determined using Hard Tuner's and RandomSearch to optimize predictive performance. The output layer is designed to predict the I–V and C–V characteristics of the NSFET, including the drain current and gate-related capacitances that define the device's electrical performance. Hyperparameter tuning explores the number of neurons per hidden layer and the learning rate, while early stopping is applied to prevent overfitting and ensure reliable predictions.

The model is trained on the training set, and its performance is evaluated on the test set using the MAE and R^2. According to Chicco et al. (2021), the theoretical foundation of regression models encompasses characteristics that reveal links within the data and offer alternative perspectives on broader viewpoints [16]. Overall, this ANN model effectively captures the underlying relationships between geometric parameters and device behavior, providing a reliable and computationally efficient alternative to full TCAD simulations.

2.4. Mean Squared Error (MSE)

MSE can be used if the data contains outliers that need to be removed. The MSE is good for attributing data with large weights to specific points [16]. The MSE equation is shown in Equation (1).

$$MSE = \frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2 \quad (1)$$

where n = number of observer data; yi = true value; and $\hat{y}_i$ = predicted value

2.5. Mean Absolute Error (MAE)

MSE is sensitive to outliers due to squared error penalization. MAE calculates the absolute differences in all data and takes the average in absolute values [16]. The MAE equation is shown in Equation (2).

$$MAE = \frac{1}{n}\sum_{i=1}^{n}|y_i - \hat{y}_i| \quad (2)$$

where n = number of observer data; y_i = true value; and $\hat{y}_i$ = predicted value

2.6. Coefficient of Determination (R^2)

The R^2 explains how independent data can explain existing dependent data [16]. The R^2 equation is shown in Equation (3).

$$R^2 = 1 - \frac{\frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2}{\frac{1}{n}\sum_{i=1}^{n}(y_i - \bar{y})^2} \quad (3)$$

where n = number of observer data; yi = true value; $\hat{y}_i$ = predicted value; and $\bar{y}$ = mean of observed values.

The ANN model is designed to achieve an R^2 value greater than 0.98. If this threshold is not reached, the modeling process is repeated to improve accuracy. Once trained, the model predicts the I-V and C-V characteristics of NSFET.

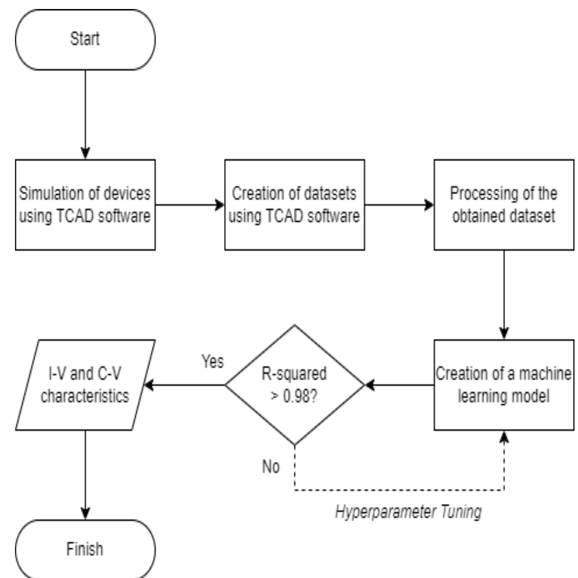

Figure 2. Flowchart for Creating an ML Model

With the application of Hard Tuner, the ANN architecture can efficiently optimize the number of neurons and hidden layers to achieve optimal predictive performance. This approach prevents both underfitting and overfitting, resulting in reliable and computationally efficient predictions of NSFET characteristics.

The constructed ANN architecture is illustrated in Figure 3, showing the schematic structure of the input layer, two hidden layers, and the output layer used to predict the I–V and C–V characteristics of the NSFET.

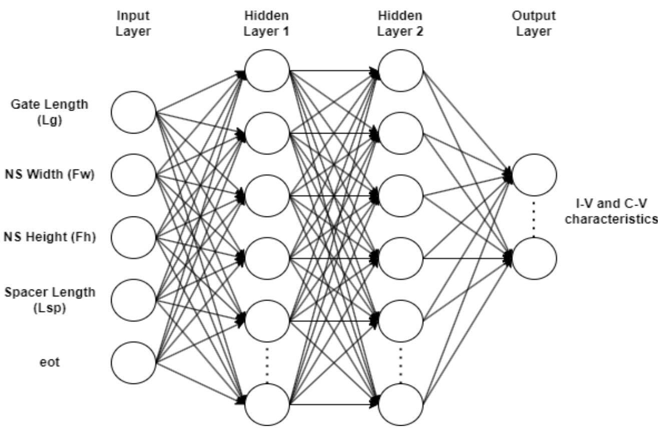

Figure 3. A schematic design of CNN architecture [13]

3. RESULTS AND DISCUSSIONS

3.1. Synopsys Sentaurus TCAD Simulation Results

The information is obtained from simulations performed using the Sentaurus Synopsys TCAD application. A total of 405 data points were collected by varying five distinct parameters. The I-V and C-V characteristics are determined by five factors: L_g, F_w, F_h, L_{sp}, and e_{ot}. This study involved the implementation of two step simulations. The initial simulation generates values for several parameters, including threshold voltage (V_T), maximum transconductance (g_{max}), off current (i_{off}), saturation current (i_{sat}), slope of the subthreshold swing (ss_{lop}), and output resistance (r_{out}). The second simulation produces gate-to-gate capacitance values measured in femto-farad units (C_{gg_fF}). In this scenario, a device is selected randomly, and its parameters are modified to assess if the I-V curve exhibits higher levels of exponential characteristics. Following an exponential curve, the device quickly transitions from the off state to the on state. The ss_{lop} is a metric employed to ascertain the speed of an entity [17]. The device selected as the starting point has a L_g of 11 nm, a F_w of 21 nm, a F_h of 4 nm, and a L_{sp} of 3 nm. The e_{ot} is then adjusted. These initial values produce the curve shown in Figure 4.

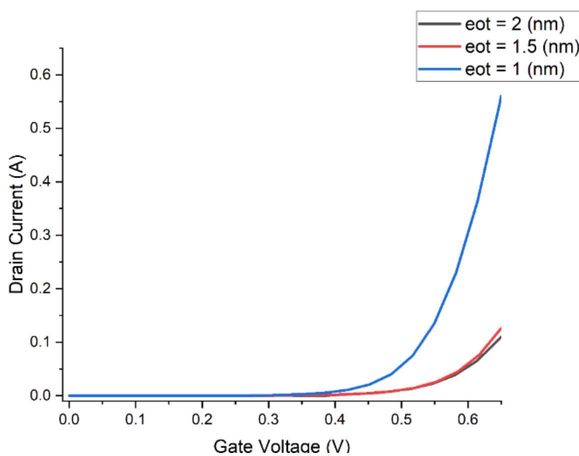

Figure 4. I-V characteristics with variations in e_{ot}

The results indicate that the curve has a more exponential structure when the e_{ot} value is 1 nm, as shown in Figure 4. This is because the ss_{lop} value for this curve is lower than the ss_{lop} value for the current curve. Thus, a value of 1 nm is selected as the subsequently determined e_{ot} value. Once the end of transmission (e_{ot}) value is acquired, the variation is performed using the least significant bit (L_{sp}) to yield the subsequent device values: L_g = 11 nm, F_w = 21 nm, F_h = 4 nm, and e_{ot} = 1 nm.

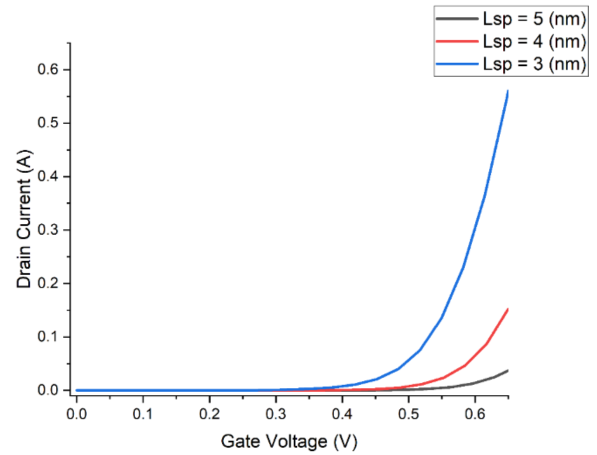

Figure 5. I-V characteristics with varying L_{sp}

Figure 5 demonstrates that the curve with an L_{sp} value of 3 nm has the most pronounced exponential structure. Subsequently, the F_h parameter is adjusted to get specific values for the device: L_g = 11 nm, F_w = 21 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm.

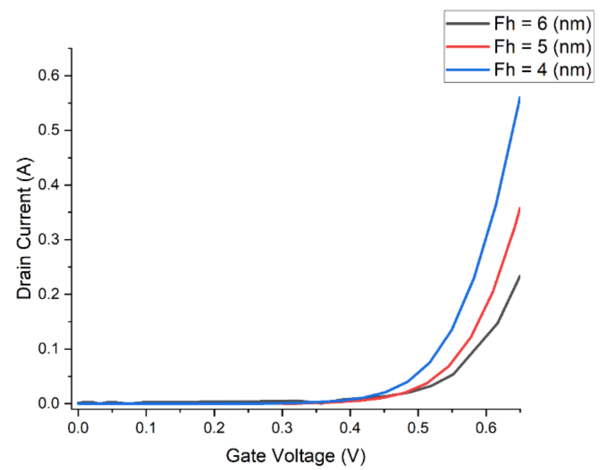

Figure 6. I-V characteristics with variations in sheet thickness (F_h)

Figure 6 demonstrates that the curve form of F_h = 4 nm is more exponential than that of F_h = 5 nm and F_h = 6 nm. The following parameter needs to be adjusted is F_w. The device is configured to have the following values: L_g = 11 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm.

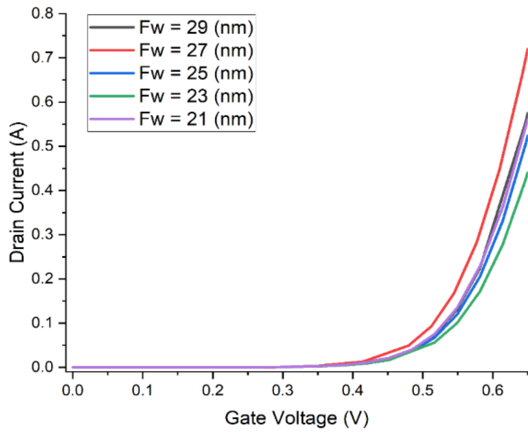

Figure 7. I-V characteristics with variations in sheet width (F_w)

Figure 7 displays a curve with a more pronounced exponential shape and a F_w (full width) of 27 nm. Subsequent modifications are applied to the L_g value. The device is configured with the following temporary values: F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm.

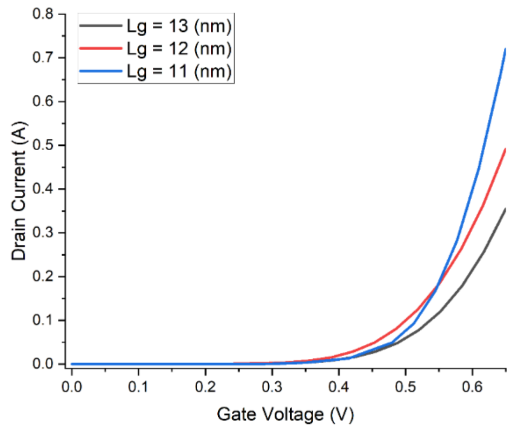

Figure 8. I-V characteristics with variations in L_g

Figure 8 shows that L_g = 11 nm has a more exponential-shaped curve. From the variations in the values carried out, it is found that the device with values L_g = 11, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm had a curve with the most exponential shape. Figure 10 shows the results of doping concentration on the device with the following parameters: L_g = 11, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm.

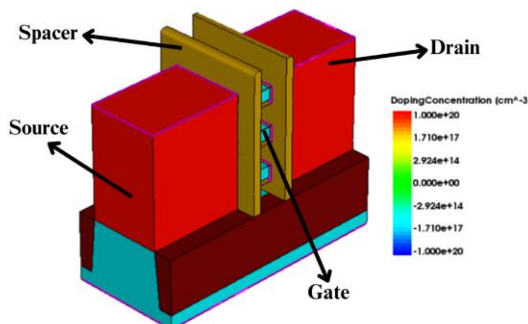

Figure 9. Doping at L_g = 11 nm, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1.5 nm

The devices selected through variation use silicon material on the source, drain, and gate with Boron Active Concentration doping as shown in Figure 9, which has a doping concentration with a value of 1×1,020 cm^{-3} on the source and drain, and the Boron Active Concentration doping concentration on the gate has a value ranging between -2.92×1014 cm^{-3} to -1.70×1020 cm^{-3}. The arsenic active concentration is doping the source and drain gates with a concentration of 1×1020 cm^{-3}. Devices with these values produce the characteristic values shown in Table 3.

Table 3. Parameters of NSFET Device Simulation Results with Parameters L_g = 11 nm, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm

Parameters	Value	Unit
V_T	3.99×10^{-1}	Volts (V)
g_{max}	7.90×10^{-5}	Siemens (S)
i_{off}	2.36×10^{-10}	Amperes (A)
i_{sat}	7.20×10^{-6}	Amperes (A)
ss_{lop}	1.20×10^{-1}	Volt per decade (V/dec)
r_{out}	1.16×10^{6}	Ohms (Ω)
C_{gg_fF}	8.18×10^{-2}	Femtofarads (fF)

A device with parameters L_g = 11 nm, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and e_{ot} = 1 nm produces the I-V and C-V curves shown in Figures 10a and 10b

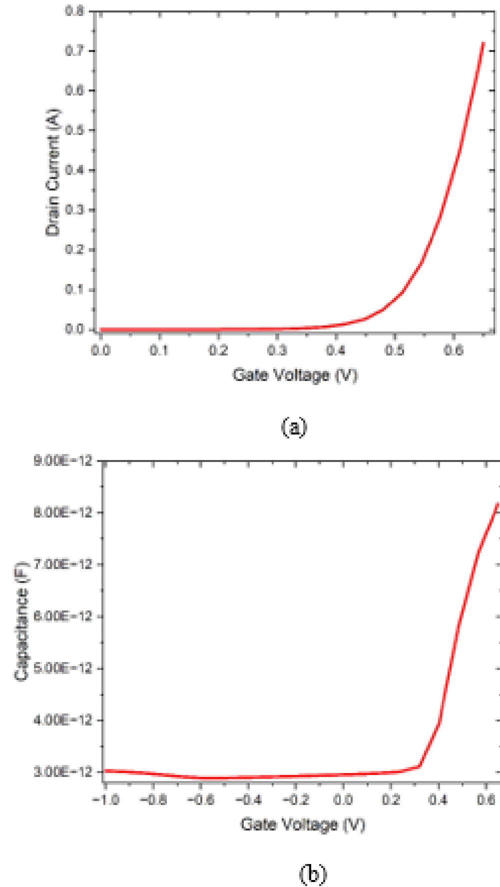

Figure 10. Device curve with parameters L_g = 11 nm, F_w = 27 nm, F_h = 4 nm, L_{sp} = 3 nm, and eot = 1 nm, (a) I-V curve and (b) C-V curve

3.2. Machine Learning (ML) Results

The study involved the development of an NSFET device and an ML model to accurately predict the properties of the NSFET. In the TCAD simulation, out of 405 TCAD simulations, 42 failed due to numerical convergence issues. From the remaining 363 samples, only 188 complete data points containing all target variables (V_T, g_{max}, i_{off}, i_{sat}, ss_{lop}, r_{out}, C_{gg_fF}) are retained. The incomplete samples are excluded to ensure consistency in supervised learning.

When conducting a targeted search for data that contains all the required values, there are only 188 occurrences of such data. The occurrence results from the fabrication technique employed in the device's creation or operation in inversion mode. According to these studies, gadgets that use fabrication technology of 5 nm or smaller are demonstrates strong performance. The data acquired further indicates that building transistor devices is not simple. Table 4 presents a comparison of the ML model created with the results obtained from previous resear

Table 4. Comparison of ML Models

No.	Researcher	Electronic Devices	ML Algorithm	Dataset Size	Output	Results
1.	Our study	Nanosheet Field-effect Transistors	Artificial Neural Network (ANN)	363	Predicts I-V and C-V characteristics	R^2 = 0.9915 dan MAE = 0.00996
2.	[12]	Nanosheet Field-effect Transistors	Artificial Neural Network (ANN)	31,680	Predicts FoMS (V_T, Ion, I_{off}, dan SS)	R^2 = 0.9872
3.	[11]	Fin-shaped Field Effect Transistor	Auto-Encoder	25-200	Predicts I-V and C-V characteristics	R^2 not reported MAE = 0.84-0.98

The ML model in Table V exhibits a higher R^2, specifically 0.9915. It suggests that the anticipated qualities of the NSFET being examined exhibit superior performance. The model yields a reduced MAE value, indicating a decrease in the average absolute error. ML was developed with an ANN with the support of Hard Tuner. The prediction characteristics are subsequently evaluated using the R^2 metric. The ML model generated an R^2 value of 0.9915. This indicates that the independent variable can account for 99% of the variation in the dependent variable, leaving only a small portion that cannot be attributed to it. Finally, the ML model provides an MAE value of 0.00996.

4. CONCLUSIONS AND RECOMMENDATIONS

This study examines an ANN-based compact model that accurately predicts the I-V and C-V characteristics of NSFET, including both conventional devices and those with dimensions below 5 nanometers. The ANN model is constructed by choosing five fundamental geometric parameters. The initiative effectively produced 363 data sets for the NSFET. It demonstrates the feasibility of creating devices utilizing fabrication technology that is 5 nm or smaller in scale. Furthermore, it suggests that creating NSFET devices is a laborious and lengthy procedure. The ML model exhibits a strong correlation between the anticipated and actual values, as indicated by its R^2 value of 0.9915. Additionally, the model yields an MAE value of 0.00996, indicating a small average discrepancy between the predicted and actual values. The ML model's indicates robust predictive capability from the improvement in the R^2 value as it approaches 1 and the decrease in the MAE value as it approaches 0. Future work may compare ANN performance with other regression models such as Random Forest and Gradient Boosting.

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DECLARATION OF INTEREST

There are no conflicts to declare.

DATA AVAILABILITY STATEMENT

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

AUTHOR CONTRIBUTION

REP: Writing - Original Draft, Writing - Review & Editing, Funding acquisition. MRF: Writing - Original Draft, Investigation, Data Curation. MAR: Formal analysis, Project administration, Conceptualization. WHK: Visualization. JNF: Visualization, Project administration. RP: Formal analysis. EH: Validation, Supervision. IH: Formal analysis, Project administration. BM: Formal analysis, Supervision.

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