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Analytical potential model of raised source drain double gate junctionless field effect transistors

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ABSTRACT

A 2D potential model is presented for a raised source drain double-gated junctionless field-effect transistor (RSD DG JLFET). The proposed raised source drain structure features a channel thickness that is smaller than the thickness of the source and drain regions. The potential model is derived by solving Poisson's equation, with separate solutions obtained for different regions. Initially, a parabolic potential profile is assumed to extend throughout the entire body. However, since the device comprises alternating depleted and non-depleted regions, the potential profile will not remain uniform across the entire channel. The boundary conditions are derived from the initial assumption, while the solutions to Poisson's equation vary across different regions. The developed model is compared with simulation results from TCAD and shows an excellent agreement with the TCAD simulation results.

Keywords: *Potential model, Raised source drain, JLFET, TCAD*

1. INTRODUCTION

Junctionless field-effect transistors (JLFETs) have emerged as a significant advancement in semiconductor device technology due to their simplified fabrication process and potential for enhanced scalability and performance. Traditional MOSFETs rely on doping junctions to create source and drain regions, which introduces fabrication complexity and challenges in nanoscale devices. JLFETs, in contrast, utilize a uniformly doped channel, eliminating the need for these junctions. The feasibility and simplicity of JLFET fabrication were initially demonstrated by [1], and this was further supported by the work of [2], who proposed the SOI gated resistor as a junctionless CMOS structure. These early studies highlighted the potential of JLFETs for scalable and cost-effective technologies, with further extensions to nanowire transistors by [3], reinforcing the promise of JLFETs in achieving high performance without junction complexities. The theoretical framework for JLFETs was expanded by [4], who presented a comprehensive theory for junctionless nanowire FETs, emphasizing their unique electrical characteristics. Subsequent research by [5–6] offered practical design guidelines and properties for JLFETs, further solidifying their applicability in modern electronics. However, as JLFETs are scaled down to nanoscale dimensions, several challenges arise. The work by [7], examined the electrical characteristics of 20-nm junctionless silicon nanowire transistors, highlighting their scalability, and [8] analysed threshold voltage variability due to random dopant fluctuations, a critical issue in nanoscale devices. Innovations like dual-material gates [9–11] and mobility improvement via uniaxial strain [12] have been explored to enhance device performance. Additionally, [13] investigated low-field mobility in ultrathin silicon nanowires, providing insights into carrier transport in JLFETs. The [14], demonstrates advancements toward high-frequency and compact applications. Parallel-gated JLFETs, explored by [15], provide alternative structural approaches and [16] introduced a potential model for parallel-gated JLFETs, emphasizing novel device configurations for enhanced performance. Semi-analytical models by [17] laid the groundwork for understanding subthreshold behavior in short-channel devices. Subsequent works by [18] included interface charge traps and temperature effects, improving model accuracy. Quantum mechanical effects were incorporated into threshold voltage models for dual-material double-gate JLFETs, addressing ultra-short channel scenarios [19] contributed a complete 2-D analytical potential model for symmetric double-gate devices. A simulation study of raised source-drain double gate JLFETs [20–21], offering insights into their performance improvements through structural modifications. Figure 1: shows a schematic diagram of the RSD DG Junctionless Transistor and Table 1 presents a

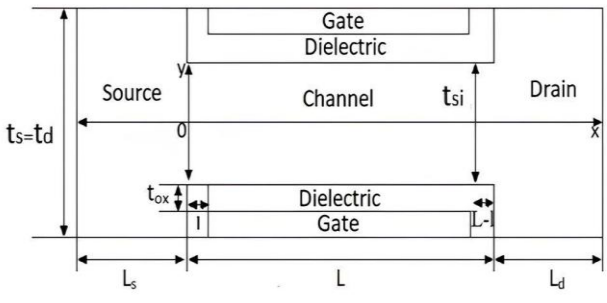

Figure 1. A schematic diagram of RSD DG junctionless transistor

Table 1. Comparison of JLFET devices

Source	Gate Structure	Channel Dimension (nm^2)	Gate length (μm)	S.S (mV/dec)	DIBL (mV/V)	$\frac{I_{on}}{I_{off}}$ $V_G; V_D$
[22]	GAA	12×23	1	15	199	$>10^6$ 5 V; 2 V
[23]	GAA	2×70	1	17	61	$>10^7$ 3 V; 0.5 V
[24]	Planer	10 μm×10	5	240	N/A	$>10^7$ 3 V; 1 V
[25]	Tri-gated	93×11	0.09	285	420	$>10^7$ 4 V; 1 V
[26]	GAA	12×45	.02×2	105	83	$>10^8$ 4 V; 1 V
This Work	Raised Soured Drain Double Gate	50×15	20 nm	75	61	$>10^8$ 4 V; 1 V

Table 2. Simulation specification

Parameter	Typical Value
Doping Concentration	10^{19} /cm^3
Gate Length (L)	20 nm
Channel Thickness (t_{Si})	10 nm
Device Width (W)	10 nm
Source/Drain Height	16 nm
Dielectric Thickness	2 nm

comparison of key performance metrics for various JLFET devices, highlighting the advantages of the RSD DG JLFET structure. Table 2 presents the simulation specifications.

For all modeling and simulation work, the control voltages were set to V_g = 0 V and V_{ds} = 0.1 V.

2. MATHEMATICAL MODEL FOR ELECTROSTATIC POTENTIAL

The Poisson's equation for N-channel double gate Junctionless FET at moderate doping concentration is [10]:

$$\frac{\partial^2 \emptyset(x,y)}{\partial x^2} + \frac{\partial^2 \emptyset(x,y)}{\partial y^2} = -\frac{qN_d}{\in_{Si}} \quad (1)$$

where $\emptyset(x,y)$, q, N_d, $\in_{Si}$ are the electrostatic potential, charge carrier, doping concentration and permittivity of silicon.

One solution of Poisson's equation can be assumed as a parabolic function [10]:

$$\emptyset(x,y) = C_o(x) + C_1(x)y + C_1(x)y^2 \quad (2)$$

The boundary conditions for the double gate JLFET can be used to determine the function of x.

At $y = 0, \emptyset(x,y) = C_0(x) = \emptyset_o(x)$

At $y = 0, \frac{d\emptyset(x,y)}{dy} = 0 = C_1(x)$

At y = $\frac{t_{Si}}{2}$, where t_{Si} is the silicon layer thickness.

From [19], the scale length of the device for the region $x = l$ to $x = L - l$ is $\lambda = \sqrt{\frac{t_{Si}(4t_{ox}\in_{Si} + t_{Si}\in_{ox})}{8\in_{ox}}}$

where, t_{ox} and $\in_{ox}$ are the gate oxide thickness and permittivity of the gate oxide.

The original potential equation is:

$$\emptyset(x,y) = \emptyset_o(x) + \frac{4\in_{ox}}{t_{Si}(4t_{ox}\in_{Si} + t_{Si}\in_{ox})} + \{\emptyset_{gs} - \emptyset_o(x)\}y^2 \quad (3)$$

With the addition of gate thickness t_g, the effective oxide capacitance is altered for the region $x = 0$ to $x = l$ and $x = L - l$ to $x = L$. So, the modified scale length is:

$$\lambda_1 = \sqrt{\frac{t_{Si}(4t_{ox} + t_g)\in_{Si} + t_{Si}\in_{ox}}{8\in_{ox}}}$$

The source-drain potential equation of the proposed structure is:

$$\frac{d^2\emptyset_o(x)}{dx^2} - \frac{\emptyset_o(x)}{\lambda_1^2} = C \quad (4)$$

where $C = -q\frac{N_d}{2\in_{Si}} - \frac{1}{\lambda_1^2}\emptyset_{gs}$.

i.e. $\emptyset_{gs} = V_{gs} - V_{fb}$

where V_{gs} is the gate to source voltage, and V_{fb} is the flat band voltage.

With $t_g$the permittivity of the additional gate layer $\in_g$ contribute to the gate capacitance.

The modified potential equation is:

$$\emptyset(x,y) = \emptyset_o(x) + \frac{4 \in_{ox}}{t_{Si}(4t_{ox} \in_{Si} + t_{Si} \in_{ox} + t_g \in_g)} + \{\emptyset_{gs} - \emptyset_o(x)\}y^2 \quad (5)$$

From [21], for $x = -L_s$, $\emptyset_o(-L_s) = 0$ and $x = L + L_d$, $\emptyset_o(L + L_d) = V_{ds}$:

$$\begin{aligned}\emptyset_o(x) == -q\frac{N_d}{2 \in_{Si}}x^2 &+ \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\left(e^{\frac{x}{\lambda}} - 1\right)\right. \\ &\left. - \frac{\left\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\right\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)e^{\frac{L_s}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\left(e^{-\frac{L_s}{\lambda}} - 1\right) + q\frac{N_d}{2 \in_{Si}}L^2\right]\frac{x}{L} \\ &+ \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)} - \frac{\left\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\right\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)e^{\frac{L_s}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\right] - C\lambda^2 \quad (6)\end{aligned}$$

At $x = 0$ to $x = l$ where $x = L/0$ or $x = (L - l)$ to $x = L$:

$$\emptyset_o(x) = A^1 e^{\frac{x}{\lambda_1}} - B^1 e^{-\frac{x}{\lambda_1}} - C\lambda_1^2 \quad (7)$$

$$\emptyset_o(0) = A^1 - B^1 - C\lambda_1^2$$

$$A^1 = B^1 + \emptyset_o(0) + C\lambda_1^2 \quad (8)$$

And $\emptyset_o(l) = A^1 e^{\frac{l}{\lambda_1}} - B^1 e^{-\frac{l}{\lambda_1}} - C\lambda_1^2$

$$\emptyset_o(l) + C\lambda_1^2 = A^1 e^{\frac{l}{\lambda_1}} - B^1 e^{-\frac{l}{\lambda_1}} \quad (9)$$

$$\emptyset_o(l) + C\lambda_1^2 = \{B^1 + \emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}} - B^1 e^{-\frac{l}{\lambda_1}}$$

$$B^1 = \frac{\emptyset_o(l) + C\lambda_1^2 - (\emptyset_o(0) + C\lambda_1^2)e^{\frac{l}{\lambda_1}}}{e^{\frac{l}{\lambda_1}} - e^{-\frac{l}{\lambda_1}}}$$

$$B^1 = \frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} \quad (10)$$

$$A^1 = \frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}\, e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2 \quad (11)$$

$$\emptyset_o(x) = \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}\, e^{\frac{l}{\lambda_1}}}{2\sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\}e^{\frac{x}{\lambda_1}} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}\, e^{\frac{l}{\lambda_1}}}{2\sinh\left(\frac{l}{\lambda_1}\right)}\right\}e^{-\frac{x}{\lambda_1}} - C\lambda_1^2 \quad (12)$$

Source drain potential modelling:

In Poisson's equation, source drain region can be written as:

$$\frac{d^2\emptyset_o(x)}{dx^2} = -q\frac{N_d}{\in_{Si}} \quad (13)$$

A solution of the above equation can be written as:

$$\emptyset_o(x) = ax^2 + bx + c \quad (14)$$

where $a = -q\frac{N_d}{2\in_{Si}}$, b and c are constants to the boundary conditions.

From [19] at $x = l$ to $x = L - l$,

$$\begin{aligned}\emptyset_{osd}(x) == & -q\frac{N_d}{2\in_{Si}}x^2 \\ & + \left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\left(e^{\frac{x}{\lambda}} - 1\right)\right. \\ & \left. - \frac{\left\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\right\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)e^{\frac{L_s}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\left(e^{-\frac{L_s}{\lambda}} - 1\right) + q\frac{N_d}{2\in_{Si}}L^2\right]\frac{x}{L} \\ & + \left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)} - \frac{\left\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\right\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)e^{\frac{L_s}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}\right)}\right] - C\lambda^2 \end{aligned} \quad (15)$$

Now for raised portion at gate $x = 0$ to $x = l$ or $x = (L - l)$ to $x = L$,

At $x = 0$

$$c_1 = \emptyset_o(0) = \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2\sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2\sinh\left(\frac{l}{\lambda_1}\right)}\right\} - C\lambda_1^2 \quad (16)$$

At $x = l$

$$\begin{aligned}\emptyset_o(x) = & a_1 l^2 + b_1 l + c_1 \\ & = \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\}e^{\frac{l}{\lambda_1}} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\}e^{-\frac{l}{\lambda_1}} \\ & - C\lambda_1^2 \end{aligned} \quad (17)$$

$$\begin{aligned}\emptyset_o(x) = & -q\frac{N_d}{2\in_{Si}}l^2 + b_1 l + \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\} \\ & - C\lambda_1^2 \\ & = \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\}e^{\frac{l}{\lambda_1}} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\}e^{-\frac{l}{\lambda_1}} \\ & - C\lambda_1^2 \end{aligned} \quad (18)$$

$$\begin{aligned}b_1 = & \left[\left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\}e^{\frac{l}{\lambda_1}} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\}e^{-\frac{l}{\lambda_1}}\right. \\ & + \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\} - \left\{\frac{\emptyset_o(l) + C\lambda_1^2 - \{\emptyset_o(0) + C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)} + \emptyset_o(0) + C\lambda_1^2\right\} \\ & \left. + q\frac{N_d}{2\in_{Si}}l^2\right]/l \end{aligned} \quad (19)$$

$$\emptyset_{\text{raised source drain}}(x) = -q\frac{N_d}{2\in_{Si}}x^2 + \left[\left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}+\emptyset_o(0)+C\lambda_1^2\right\}e^{\frac{l}{\lambda_1}} - \left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\}e^{-\frac{l}{\lambda_1}} + \left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\} - \left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}+\emptyset_o(0)+C\lambda_1^2\right\} + q\frac{N_d}{2\in_{Si}}l^2\right]x/l + \left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}+\emptyset_o(0)+C\lambda_1^2\right\} - \left\{\frac{\emptyset_o(l)+C\lambda_1^2-\{\emptyset_o(0)+C\lambda_1^2\}e^{\frac{l}{\lambda_1}}}{2sinh\left(\frac{l}{\lambda_1}\right)}\right\} - C\lambda_1^2 \quad (20)$$

3. RESULTS AND DISCUSSION

This section presents results and discusses the analytical potential model and its comparison with TCAD simulations [27]. The potential distribution is analyzed with respect to variations in dielectric material, dielectric thickness, channel thickness, drain voltage, and gate voltage, considering both longitudinal and transverse directions. The simulations are conducted using the Cogenda Visual TCAD 2D device simulator. Fermi-Dirac statistics, without considering impact ionization, are used for carrier distribution. The source potential is taken as the reference potential throughout the calculations. A uniform doping concentration 10^{19} /cm^3 is maintained in all simulations to ensure sufficient current flow in the ON state. The analysis is based on variations in dielectric material, dielectric thickness, channel thickness, drain voltage, and gate voltage. The longitudinal potential profile along the x-axis at y = 0 is analysed for different parameters. Figure 2 presents the effect of different dielectric materials SiO_2, Si_3N_4, and HfO_2 on the potential distribution. Among these, HfO_2, being a high-k dielectric, offers superior gate control over the channel, effectively reducing short-channel effects and improving electrostatic integrity. In contrast, lower-k materials like SiO_2 and Si_3N_4 exhibit comparatively weaker gate control due to reduced capacitive coupling.

Figure 3 examines the impact of dielectric thickness on the longitudinal potential profile, demonstrating that a reduced dielectric thickness improves electrostatic control and helps mitigate short-channel effects. The analysis considers dielectric thickness values of 2 nm, 3 nm, and 4 nm. Among these, the 2 nm dielectric provides the strongest gate control, effectively suppressing leakage currents and enhancing channel potential modulation. As the dielectric thickness increases to 3 nm and 4 nm, the gate's influence on the channel potential weakens, leading to increased short-channel effects and reduced electrostatic integrity. This highlights the importance of selecting an optimal dielectric thickness for achieving better device performance. Figure 4 explores the influence of channel thickness on the longitudinal potential profile, demonstrating that a thinner channel enhances electrostatic integrity but may lead to higher resistive effects. The analysis considers channel thickness values of 10 nm, 12 nm, and 14 nm. A 10 nm channel provides superior gate control, effectively suppressing short-channel effects and ensuring better electrostatic confinement. However, as the channel becomes thinner, resistance increases, potentially affecting current conduction. With a channel thickness of 12 nm, a balance between electrostatic control and conductivity is achieved, making it a viable option for optimizing device performance. When the channel thickness increases to 14 nm, the gate's control weakens, leading to a higher susceptibility to short-channel effects and a less uniform potential distribution along the channel.

Figure 5 illustrates the longitudinal potential profile along the x-axis at y = 0 for different values of drain voltage, specifically 0.1 V, 0.2 V, and 0.3 V. As the drain voltage increases, the potential gradient along the channel becomes steeper, influencing carrier transport and increasing the electric field across the device. At a low drain voltage of 0.1 V, the potential variation is relatively small, resulting in minimal DIBL and better gate control over the channel. When the drain voltage is raised to 0.2 V, the potential drop across the channel becomes better, slightly shifting the minimum potential towards the source side. At 0.3 V, the effect is further amplified, leading to a more significant reduction in the minimum channel potential and a higher risk of short-channel effects. Increasing the drain voltage affects the electrostatic behavior of the device, emphasizing the need for careful voltage optimization to maintain stable transistor operation. Figure 6 illustrates the longitudinal potential profile along the x-axis at y = 0 for different values of gate voltage, specifically 0 V, 0.5 V, and 1 V. The gate voltage plays a crucial role in modulating the channel potential and controlling carrier transport. At 0 V, the channel remains fully depleted, resulting in a higher potential barrier that restricts current flow. As the gate voltage increases to 0.5 V, the channel begins to accumulate charge carriers, reducing the potential barrier and facilitating conduction. At 1 V, a strong inversion layer

forms, significantly lowering the channel potential and enhancing carrier mobility, leading to improved device performance. The results indicate that higher gate voltages provide better electrostatic control, ensuring efficient switching behaviour while mitigating short-channel effects.

Having analyzed the effect of the longitudinal potential profile and the transverse potential profile along the y-axis at x = 0, is also examined for various parameters. Figure 7 illustrates the effect of different drain voltages, indicating that higher drain voltages lead to increased potential gradients, affecting subthreshold behaviour. Figure 8 presents the transverse potential profile along the y-axis at x = 0 for different dielectric thickness values of 2 nm, 3 nm, and 4 nm. A thinner dielectric, 2 nm, provides stronger gate control, ensuring a more confined potential distribution and reducing the influence of short-channel effects. As the dielectric thickness increases to 3 nm and 4 nm, the gate's electrostatic control weakens, leading to a broader potential spread and higher susceptibility to leakage. Figure 9 explores the transverse potential profile for different channel lengths, demonstrating that longer channels exhibit reduced short-channel effects and more uniform potential distribution. Figure 10 studies the effect of different dielectric materials, revealing that high-k dielectrics enhance electrostatic control and provide better gate modulation. Figure 11 examines the transverse potential profile for different gate voltages, indicating that increasing gate voltage results in stronger gate-induced electric fields, improving carrier confinement in the channel.

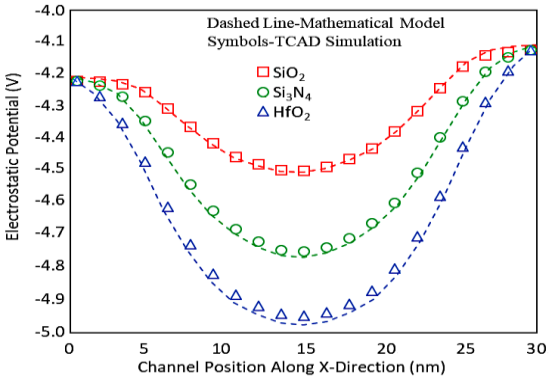

Figure 2. Longitudinal potential profile along the x-axis at y = 0 for different dielectric materials

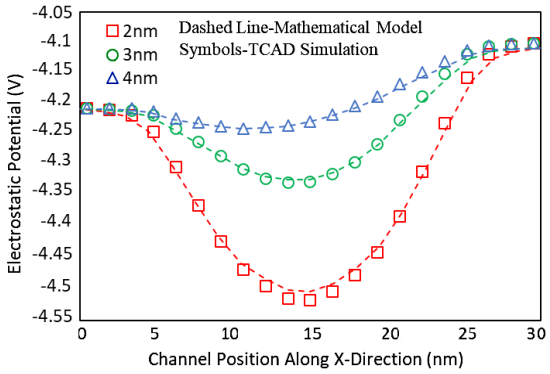

Figure 3. Longitudinal potential profile along the x-axis at y = 0 for different values of dielectric thickness

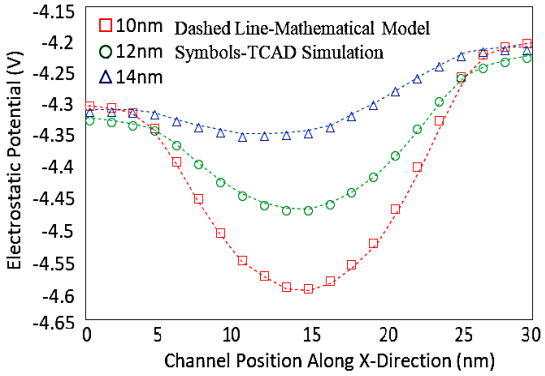

Figure 4. Longitudinal potential profile along the x-axis at y = 0 for different values of channel thickness

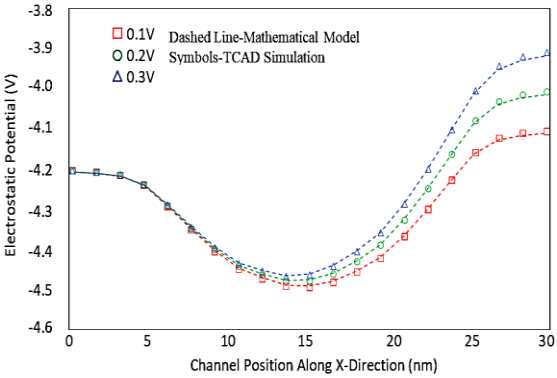

Figure 5. Longitudinal potential profile along the x-axis at y = 0 for different values of drain voltage

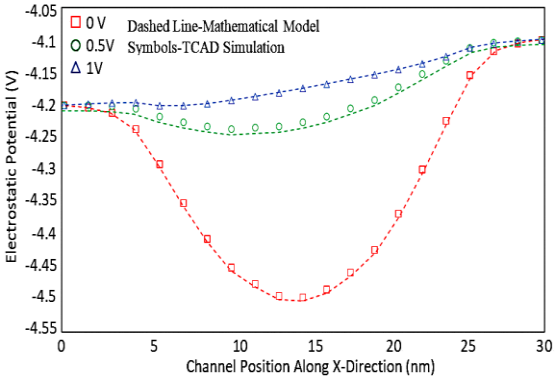

Figure 6. Longitudinal potential profile along the x-axis at y = 0 for different values of gate voltage

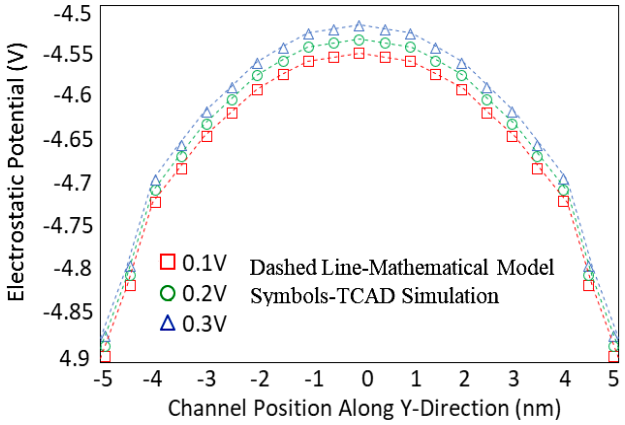

Figure 7. The transverse potential profile along the y-axis at x = 0 for different values of drain voltage

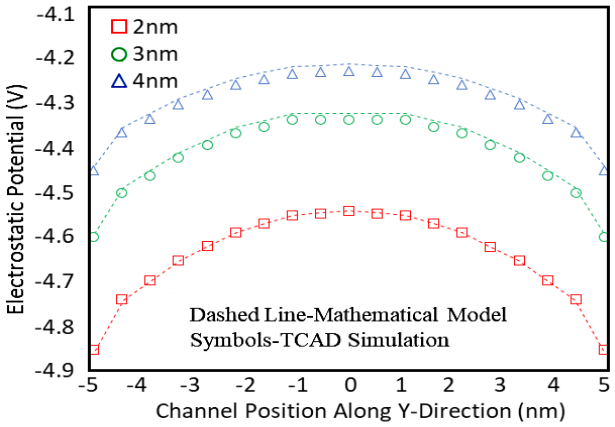

Figure 8. The transverse potential profile along the y-axis at x = 0 for different values of dielectric thickness

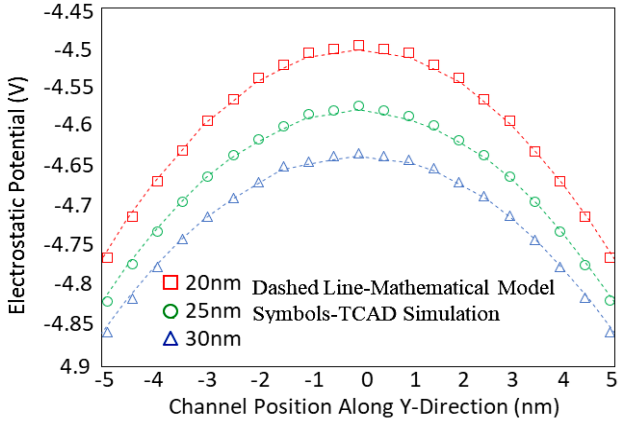

Figure 9. The transverse potential profile along the y-axis at x = 0 for different values of channel length

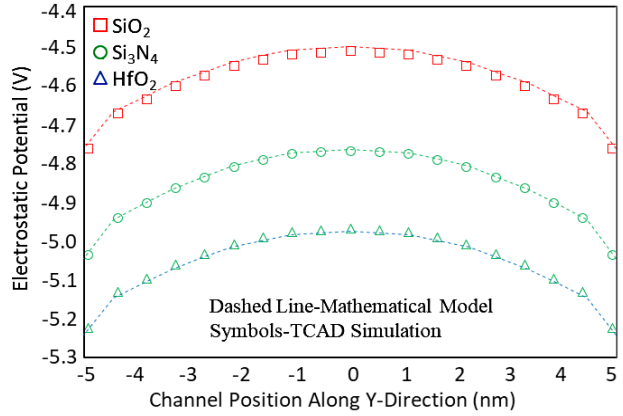

Figure 10. The transverse potential profile along the y-axis at x = 0 for different dielectric materials

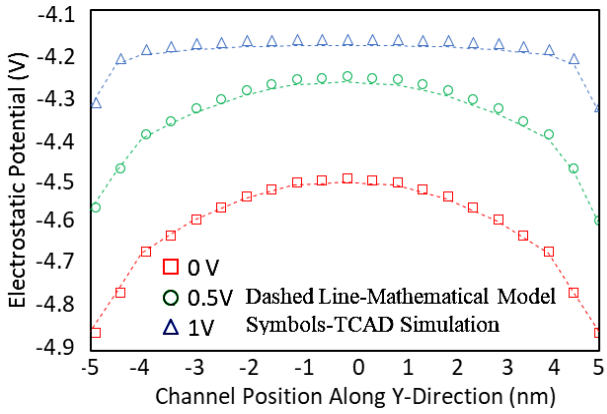

Figure 11. The transverse potential profile along the y-axis at x = 0 for different values of gate voltage

The results indicate that optimizing dielectric properties, channel dimensions, and applied voltages significantly influence the electrostatic behaviour of RSD DG JLFET. These insights are crucial for designing efficient nanoscale devices with improved performance and reduced short-channel effects.

4. CONCLUSION

In this work, the 2D analytical potential distribution for RSD DG JLFET has been developed and validated against TCAD simulations. The results confirm that utilizing high-k dielectric materials and optimizing dielectric and channel thicknesses are crucial for enhancing electrostatic control and suppressing short-channel effects in RSD DG JLFETs. These design strategies are essential for achieving improved device performance and reliability in nanoscale applications. However, a raised source-drain structure can introduce fringing fields that impact the gate control, potentially leading to variations in threshold voltage and increased gate leakage, proper care should be considered in this regard.

AUTHORS CONTRIBUTION

Rikhit Swargiary contributed to conceptualization, simulation, and manuscript writing; Kaushik Chandra Deva Sarma contributed to data analysis, validation, supervision, and final approval.

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DATA AVAILABILITY

Data generated during the research are available in the manuscript itself. No separate data are available related to the research.

DECLARATIONS

Ethics approval and consent to participate: This study did not involve human or animal subjects, and thus, no ethical approval was required.
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REFERENCES

[1] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," *Applied Physics Letters*, vol. 94, no. 5, p. 053511, 2009.

[2] J. P. Colinge *et al.*, "SOI gated resistor: CMOS without junctions," in *2009 IEEE International SOI Conference*, IEEE, 2009, pp. 1–2.

[3] J.-P. Colinge *et al.*, "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.

[4] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the Junctionless Nanowire FET," *IEEE Transactions on Electron Devices*, vol. 58, no. 9, pp. 2903–2910, 2011.

[5] J.-P. Colinge, "Junctionless transistors," in *2012 IEEE International Meeting for Future of Electron Devices, Kansai*, IEEE, 2012, pp. 1–2.

[6] J. P. Colinge *et al.*, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid-State Electronics*, vol. 65–66, pp. 33–37, 2011.

[7] C.-H. Park *et al.*, "Electrical characteristics of 20-nm junctionless Si nanowire transistors," *Solid-State Electronics*, vol. 73, pp. 7–10, 2012.

[8] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, "Analysis of Threshold Voltage Variability Due to Random Dopant Fluctuations in Junctionless FETs," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 336–338, 2012.

[9] Haijun Lou *et al.*, "A Junctionless Nanowire Transistor With a Dual-Material Gate," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1829–1836, 2012.

[10] J.-P. Colinge, "The New Generation of SOI MOSFETs," *Romanian Journal of Information Science and Technology*, vol. 11, no. 1, pp. 3–15, 2008.

[11] R. K. Baruah and R. P. Paily, "A Dual-Material Gate Junctionless Transistor With High-*k* Spacer for Enhanced Analog Performance," *IEEE Transactions on Electron Devices*, vol. 61, no. 1, pp. 123–128, 2014.

[12] J.-P. Raskin *et al.*, "Mobility improvement in nanowire junctionless transistors by uniaxial strain," in *2010 IEEE International SOI Conference (SOI)*, IEEE, 2010, pp. 1–2.

[13] B. Sorée, W. Magnus, and W. Vandenberghe, "Low-field mobility in ultrathin silicon nanowire junctionless transistors," *Applied Physics Letters*, vol. 99, no. 23, p. 233509, 2011.

[14] A. Goel, S. Rewari, S. Verma, and R. S. Gupta, "High-*K* Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for high frequency applications," *Microsystem Technologies*, vol. 26, no. 5, pp. 1697–1705, 2020.

[15] A. K. Raibaruah and K. C. Deva Sarma, "Parallel Gated Junctionless Field Effect Transistor," in *2020 International Conference on Computational Performance Evaluation (ComPE)*, IEEE, 2020, pp. 178–181.

[16] A. K. Raibaruah and K. C. D. Sarma, "A Potential Model for Parallel Gated Junctionless Field Effect Transistor," *Silicon*, vol. 14, no. 2, pp. 711–718, 2022.

[17] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, "Semianalytical Model of the Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 4, pp. 1342–1348, 2013.

[18] A. Rassekh, F. Jazaeri, M. Fathipour, and J.-M. Sallese, "Modeling Interface Charge Traps in Junctionless FETs, Including Temperature Effects," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4653–4659, 2019.

[19] K. Chandra Deva Sarma and S. Sharma, "An approach for complete 2-D analytical potential modelling of fully depleted symmetric double gate junction less transistor," *Journal of Computational Electronics*, vol. 14, no. 3, pp. 717–725, 2015.

[20] K. C. D. Sarma, D. Deka, and R. Swargiary, "A Simulation Study of Raised Source Drain Double Gate Junctionless Field Effect Transistor," in *2023 4th International Conference on Computing and Communication Systems (I3CS)*, IEEE, 2023, pp. 1–3.

[21] R. Swargiary, K. C. D. Sarma, and B. N. Thakur, "A Raised Source Drain DG JLFET for Electric Vehicles: Enhancing Performance and Efficiency," in *2025 Devices for Integrated Circuit (DevIC)*, IEEE, 2025, pp. 556–559.

[22] C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, "Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 521–523, 2011.

[23] H.-B. Chen *et al.*, "Characteristics of Gate-All-Around Junctionless Poly-Si TFTs With an Ultrathin Channel," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 897–899, 2013.

[24] H.-C. Lin, C.-I. Lin, and T.-Y. Huang, "Characteristics of n-Type Junctionless Poly-Si Thin-Film Transistors With an Ultrathin Channel," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 53–55, 2012.

[25] C.-I. Lin, K.-H. Lee, H.-C. Lin, and T.-Y. Huang, "Fabrication of tri-gated junctionless poly-Si transistors with I-line based lithography," *Japanese Journal of Applied Physics*, vol. 53, no. 4S, p. 04EA01, 2014.

[26] T.-Y. Liu, F.-M. Pan, and J.-T. Sheu, "Characteristics of Gate-All-Around Junctionless Polysilicon Nanowire Transistors With Twin 20-nm Gates," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 5, pp. 405–409, 2015.

[27] Cogenda, "VisualTCAD Semiconductor Device Simulator Version 1.7.2; VisualTCAD User's Guide" Cogenda Pte Ltd. Available: http://www.i-vis.co.jp/pdf/cogenda/Quick_Start_Guide.pdf