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Numerical study on thermal stability Performance of 4H-SiC MOSFETs

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ABSTRACT

4H-SiC MOSFETs offer superior performance and reliability in extreme conditions, making them a great option for high-power and high-temperature applications. However, thermal stability issues still hinder device performance improvements, which impact threshold stability, interface quality, and reliability. This work explores the issue by employing a 2D model that collectively integrates and disentangles the roles of electrical, thermal, and structural properties of 4H-SiC MOSFETs using COMSOL Multiphysics. Important electrical metrics are retrieved and examined under various heat conditions. The findings indicate that the V_{th} decreases from 3.05 to 2.80 V with increasing temperatures. On the other hand, the subthreshold slope rises noticeably from 41 mV/dec to 126 mV/dec with temperature. The results support the necessity of thermal control in the operational characteristics of 4H-SiC MOSFETs.

Keywords: *4H-SiC MOSFET, COMSOL Multiphysics, Power electronics, Thermal effects, Threshold voltage, Transconductance*

1. INTRODUCTION

In recent years, 4H-SiC-based semiconductor devices have significantly improved in terms of reliability, efficiency, and stability at high temperatures, thus enabling power semiconductor devices to operate in harsh environments like electric vehicles, renewable energy systems, and industrial drives [1–5]. With the support of conventional silicon-based technology, the 4H-SiC MOSFETs are promising to change the way technology is accomplished. They exhibit a higher critical electric field (8–10 times) than traditional silicon MOSFETs, allowing for improved voltage tolerance and more compact designs with increased efficiency [3, 6]. Additionally, their enhanced heat dissipation (thermal conductivity is about three times that of traditional silicon MOSFETs) prolongs the device's life and reduces the need for complex cooling systems in conditions of elevated power densities [2, 7]. This integration enhances power conversion efficiency by allowing higher switching frequencies and reducing losses, making SiC devices ideal for electric vehicles, renewable energy, and industrial uses [7]. Nevertheless, there are still issues with design and optimization, such as complicated, expensive fabrication processes and possible gate oxide damage [3, 8–10].

SiC MOSFETs are known for their high breakdown voltage, faster switching speeds, and better thermal conductivity compared to silicon-based devices [2, 7, 9, 11, 12]. Researchers indicate that SiC MOSFETs have lower on-resistance than Si MOSFETs, reducing conduction losses and exhibiting higher efficiency and faster switching, which makes them ideal for high-frequency applications [13, 14]. SiC MOSFETs allow for reduced device sizes and decreased conduction losses as they possess considerably lower on-resistance compared to Si MOSFETs [2, 3, 7]. When the temperature ranges from 25°C to 135°C, the on-resistance of SiC MOSFETs increases by just 20%, while the on-resistance of Si MOSFETs increases by 250% [3]. SiC MOSFETs also have greater switching speeds and lower switching losses due to the large bandgap and good critical electric field, which allows higher breakdown voltages and reduced parasitic capacitance [2, 3, 7]. SiC MOSFETs exhibit superior efficiency, leading to enhanced power converter efficiency [15]. However, SiC MOSFETs face challenges such as greater production costs and lower channel mobility compared to Si MOSFETs [3, 7, 9]. Despite these challenges, ongoing research is being conducted to enhance SiC MOSFET performance and manufacturability.

Bachar *et al*. [14] used COMSOL Multiphysics to analyze the effect of temperature change on electrical characteristics and visualize heat distribution throughout the MOSFET. The findings show that Si MOSFETs experience a more severe drop in threshold voltage with increasing temperature, making them less stable at high temperatures compared to SiC. Additionally, the drain current increases with temperature due to reduced charge carrier mobility. Heat distribution and hotspot temperature also differ, with SiC having lower internal temperatures and higher self-heating, leading to reliability issues.

D. Subedi *et al*. [16] also used COMSOL Multiphysics to analyze and visualize the electrical and thermal behavior of

advanced MOSFET structures, including the effects of temperature change on electrical characteristics and heat distribution in devices like the 4H-SiC Power MOSFET. The authors argue that the traditional assumption of a constant temperature profile is no longer valid for small and advanced MOSFET devices as they scale down. The energy-transport model is used instead of the full hydrodynamic model, capturing the impact of temperature gradients on carrier transport. This approach allows for accurate simulation of how temperature changes affect key electrical parameters such as current, threshold voltage, and carrier mobility. Advanced mobility models account for various scattering mechanisms, all of which are functions of temperature. The authors also show that COMSOL Multiphysics, when combined with electrical and thermal simulations, temperature-dependent mobility models, and heat flow visualization, offers a powerful method for optimizing the performance and reliability of advanced MOSFETs, including 4H-SiC power MOSFETs.

This project aims to design and model 4H-SiC power MOSFETs using COMSOL Multiphysics to improve the performance and reliability of the device structure. Parameters considered include gate oxide thickness, gate oxide type, and thermal control mechanisms to provide an effective and reliable MOSFET operating under high power conditions. The focus on designing 4H-SiC power MOSFETs capable of operating under high power conditions will address the need for robust components in high-voltage, high-frequency, and high-temperature applications, pushing the limits of current semiconductor technology. The advancements in SiC MOSFETs will drive technological advancements, enabling the development of next-generation power devices that can handle higher power densities and extreme conditions.

2. ELECTRICAL POTENTIAL SIMULATION

The MOSFET geometry can be configured using COMSOL tools, forming a micrometer-scale model of a MOSFET [16, 17]. The basic structure is a rectangle with a width of 3 μm and a height of 0.7 μm. These coordinates are essential for precisely delineating the region where the metal contact is applied, ensuring accurate assignment of electrical boundary conditions during simulation. Closed-curve polygons are used to define the source, drain, and gate contacts, with a false polygon added to show the endpoint, as shown in Table 1.

Table 1. Polygon coordinates to define the contact terminal

X (μm)	Y (μm)
0	0.67
0	0.70
0.5	0.70
0.7	0.70
2.3	0.70
2.5	0.70
3	0.70
3	0.67

Metal contact is added to the source and drain terminals, using COMSOL Multiphysics' Metal Contact feature, to generate a closed-curve polygon, precisely defining the region where the metal contact (source or drain) is applied [16]. The source terminal is grounded, with a fixed 0 voltage applied by default. The terminal can be designed to link to an external circuit's voltage or current source, like how the drain terminal connects to the drain voltage. The Thin Insulator Gate's boundary condition defines the thin oxide layer and gate contact, which can be adjusted for voltage or charge, allowing for a realistic simulation of gate control [17]. A "false polygon" is used to ensure the polygon closes properly in the simulation environment to avoid rendering or simulation errors.

Table 1's coordinates are crucial for accurately defining the contact terminal geometry in the simulation, ensuring that the electrical boundary conditions (source, drain, gate) are applied to the correct regions of the device and preventing simulation errors by guaranteeing the polygon is closed. The last point (3, 0.67) in COMSOL ensures the polygon is closed, preventing rendering or simulation errors, as the software necessitates contact regions to be defined by closed curves. This precise definition enables robust and reliable electrical potential simulations in COMSOL Multiphysics.

Electrical potential simulation, as shown in Figures 1 and 2, shows that the applied bias is represented by high-potential regions close to the source and drain, while the gate voltage impacts channel creation through a decrease in electrical potential. The device's capacity to operate at high voltage is supported, and regulated current flow is ensured by the progressive potential shift over the drift area. The gate and drain voltages both affect the conduction channel's mode of operation, with the gate voltage controlling the conduction channel's potential.

Figure 1 shows the simulated electrical potential distribution within a MOSFET device at drain and gate voltage (Vd = 0 V). The device's rectangular geometry has a source on the left, a drain on the right, and the gate above the channel region. The potential distribution is symmetric across the channel due to similar potentials between the source and drain regions. The gate voltage induces a dip in the potential just beneath the gate region, indicating the formation of an inversion layer or conduction channel. The channel region under the gate shows a lower potential due to the positive gate bias attracting electrons and forming a conductive path. There is no significant lateral electric field across the channel, meaning no current flows from source to drain. Channel formation occurs when the gate voltage is high enough to invert the surface under the gate, forming a conductive channel between source and drain.

Figure 2 shows the simulated electrical potential distribution within a MOSFET device at drain and gate voltage (Vd = 5 V). High-potential regions are indicated by red near the drain terminal, while the leftmost section is at a lower potential, corresponding to the source terminal. These regions confirm the application of external bias voltages. The central blue region shows channel formation

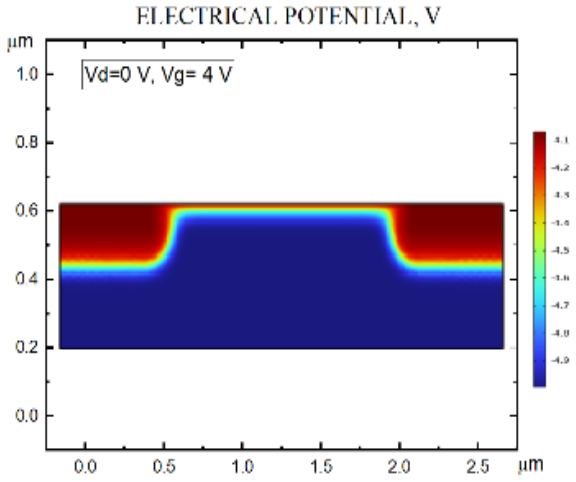

Figure 1. Electrical potential on Vg-Vd characteristics at Vd = 0 V

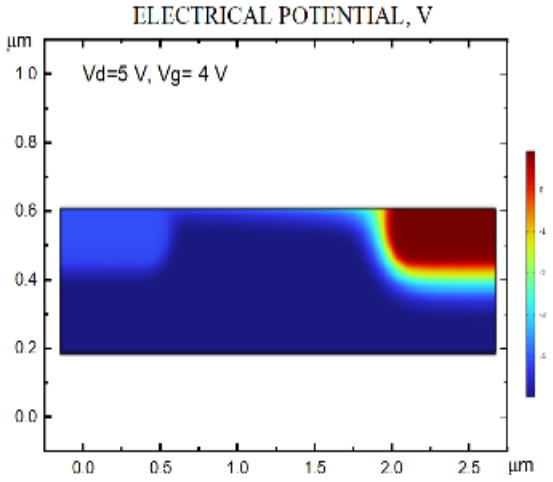

Figure 2. Electrical potential on Vg-Vd characteristics at Vd = 5 V

and gate control, with a lower electrical potential indicating a conductive path controlled by the gate voltage. The transition from blue to red is smooth, reflecting the gradual potential drop across the channel and drift region. The gate voltage modulates the potential in this channel, controlling its width and conductivity. A higher gate voltage enhances channel formation, lowering the potential barrier and allowing more current flow. The simulation demonstrates the device's ability to sustain high drain voltages without abrupt potential changes, demonstrating robust high-voltage operation.

3. RESULTS AND DISCUSSION

The range and the optimum for input power, output power, and efficiency for both Class E and Class D can be analyzed using the data presented in Figures 3, 4 and 5.

3.1. Threshold Voltage and Temperature

The transfer characteristic curve in Figure 3 illustrates the relationship between drain current and gate voltage at different temperatures ranging from 0°C to 300°C. The curves represent different temperatures, with higher temperatures corresponding to progressively shifted curves to the left. As temperature increases, the threshold voltage of a MOSFET typically decreases, allowing the MOSFET to turn on at a lower gate voltage, leading to a significantly higher drain current at lower gate voltages. This behaviour is due to temperature-induced changes in the semiconductor material's properties, specifically carrier mobility and energy bandgap. At elevated temperatures, the bandgap of the semiconductor material narrows, leading to an increase in the number of charge carriers in the conduction band, which increases current for a given gate voltage. While carrier mobility typically decreases with rising temperatures, the increase in the number of free carriers due to thermal excitation compensates for this effect, resulting in higher current at higher temperatures.

It also highlights a key difference between 4H-SiC power MOSFETs and silicon-based devices. In silicon MOSFETs, transfer characteristics often overlap or cross as temperature increases due to the negative temperature dependence of the threshold voltage, leading to instability and unpredictable switching behaviour at high temperatures. However, 4H-SiC MOSFETs exhibit transfer characteristics that shift in parallel with increasing temperature and avoid crossover. This enhances their stability and reliability at high temperatures by minimizing the risk of failure due to temperature-induced parameter shifts.

The positive temperature coefficient in 4H-SiC MOSFETs is attributed to the reduced carrier concentration at the interface and the unique band structure of SiC, which is less sensitive to temperature-induced changes in intrinsic carrier concentration compared to silicon. This lowers the threshold voltage, allowing the device to turn on more easily at higher temperatures. The negative temperature coefficient can lead to thermal runaway, a significant reliability concern for high-temperature or high-power applications. In contrast, 4H-SiC MOSFETs inherently stabilize the device against thermal runaway, as the drain current does not increase uncontrollably with temperature.

As shown in Figure 4, the threshold voltage decreases gradually from 3.05 V at 0 °C to 2.8 V at 300 °C, with a nearly linear and negative relationship between the two, with a total reduction of about 0.25 V over the 300°C range. This reduction is due to bandgap narrowing at higher

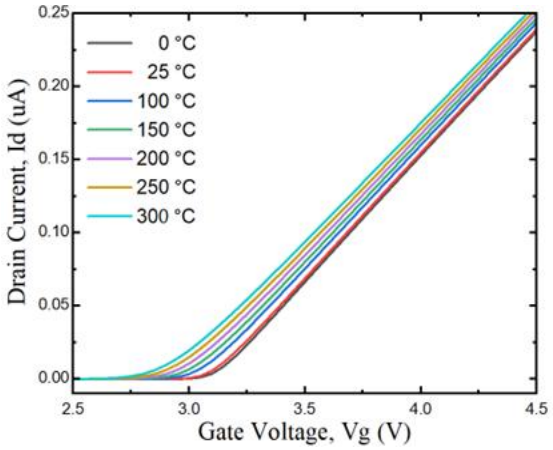

Figure 3. 4H-SiC MOSFET threshold voltage on temperature

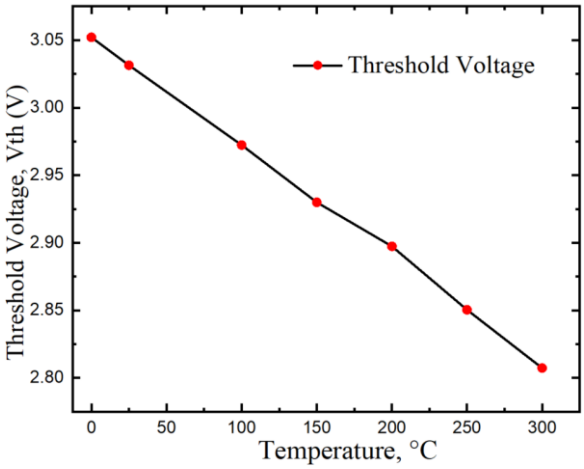

Figure 4. 4H-SiC MOSFET Threshold voltage with elevated temperature

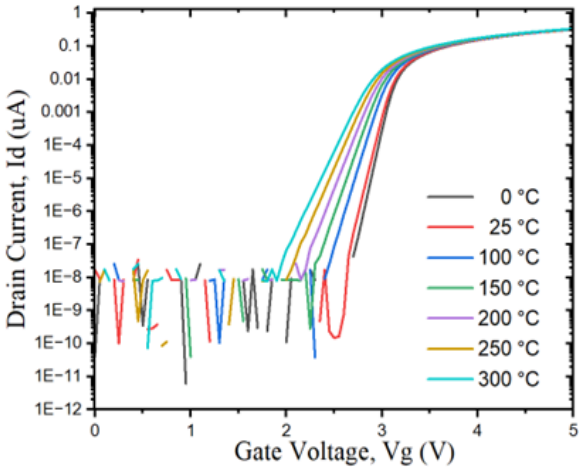

Figure 5. Logarithmic transfer characteristics curve of the 4H-SiC MOSFET

temperatures. As temperature increases, the energy gap between the valence and conduction bands in a semiconductor decreases, reducing the energy required for electrons to move from the valence band to the conduction band, making it easier for the device to turn on.

Other physical mechanisms behind the decrease include Fermi level shifts, reduced energy barrier, increased carrier density, and competing effects like mobility degradation and charge trapping at the oxide interface. Increased thermal energy allows more electrons to transition from the valence band to the conduction band, shifting the Fermi level closer to the conduction band. This shift occurs because the intrinsic carrier concentration rises with temperature, making it easier to achieve inversion in the MOSFET channel and further reducing V_{th}. As a result, the effective bandgap decreases, requiring less energy to reach the threshold voltage. However, the higher conduction band electron density also contributes to increasing the threshold voltage due to factors like depletion charge or interface traps. Daves, W. *et al*. [18] demonstrates that higher doping (increased depletion charge) and interface/fixed oxide charges both increase the threshold voltage by requiring more gate voltage to achieve channel inversion.

Understanding these effects is crucial for optimizing 4H-SiC power electronics for high-temperature environments, making them ideal for extreme conditions.

3.2. Sub-threshold Slope and Temperature

The sub-threshold graph in Figure 5 depicts the drain current, Id, on a logarithmic scale as a function of gate voltage, Vg, across a range of temperatures (0 °C to 300 °C), showcasing the behaviors of a 4H-SiC MOSFET in the sub-threshold and transition regions. The graph demonstrates a sharp increase in drain current (Id) as gate voltage (Vg) approaches and exceeds threshold voltage. In the sub-threshold region, thermally activated processes influence the current more, and as temperature increases, so does thedrain current. This is due to increased thermal energy, allowing more electrons to overcome the energy barrier and contribute to the current, even when the gate voltage is below threshold. This further leads to higher leakage currents when the temperature is high. Li, Y. [19] provides both theoretical background and practical analysis showing that high temperatures increase leakage currents in SiC MOSFETs due to bandgap narrowing, reduced energy barriers, and increased carrier generation, all of which impact device reliability and stability.

The graph also shows that the threshold voltage decreases with the increase in temperature, which is because there is a narrowing of the bandgap, and the intrinsic carrier concentration increases. This decrease in bandgap makes it easier for electrons to be thermally excited into the conduction band. This is one of the ways that the temperature characteristics of the MOSFET are reflected, and it also indicates that threshold voltage shifts should be considered while modeling circuits and systems that operate at elevated temperatures. The logarithmic scale also aids in showing weak inversion and leakage behaviors, highlighting the exponential nature of sub-threshold current and the importance of accounting for temperature-dependent threshold voltage shifts and leakage in high-temperature circuit design.

Figure 6 illustrates the sub-threshold slope (SS) of a 4H-SiC MOSFET, which changes with temperature from 0°C to 300°C. The sub-threshold slope (SS) measures the gate voltage change needed to increase the drain current by one order of magnitude (a decade) in the sub-threshold (weak inversion) region. The SS is plotted in millivolts per decade (mV/dec) of drain current versus gate voltage, which quantifies how sharply the device transitions from the off-state (low current) to the on-state (high current) in the sub-threshold region.

The sub-threshold slope (SS) is a key parameter that quantifies the drain current increase as the gate voltage approaches and exceeds the threshold voltage in the sub-threshold region. Lower SS values indicate more efficient switching between off and on states, minimizing leakage current and power loss, making it desirable for efficient switching. As temperature increases from 0°C to 300°C,

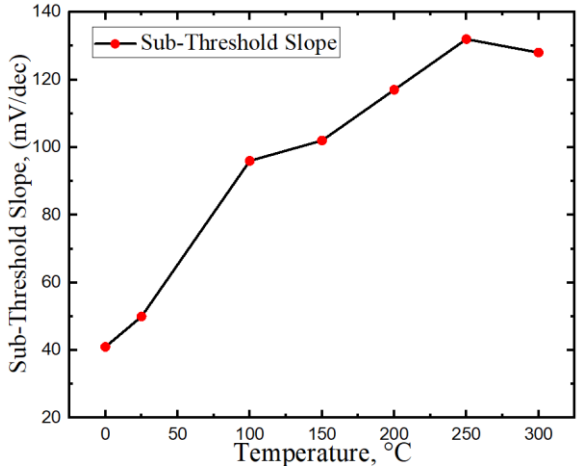

Figure 6. Measured sub-threshold slope with elevated temperature of the 4H-SiC MOSFET

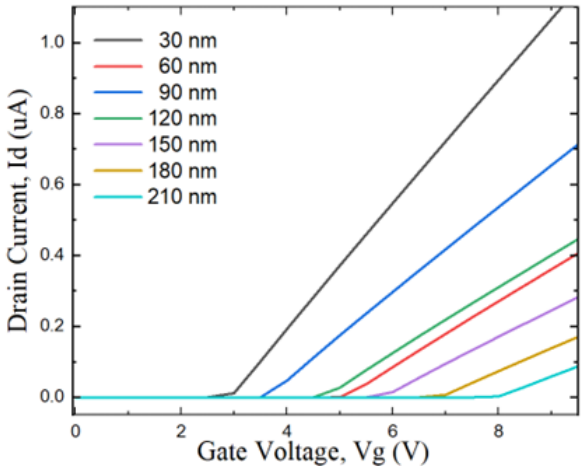

Figure 7. I_D-V_G characteristics with varying gate oxide thickness of the 4H-SiC MOSFET

the SS increases from about 30 mV/dec to a peak of ~132 mV/dec at 250°C, then slightly decreases at 300°C.The trend shows that at low temperatures, the SS is lowest, indicating a sharp, efficient transition. As the temperature rises, more carriers are thermally excited, increasing the sub-threshold current for a given gate voltage. This makes the device less sensitive to changes in Vg, resulting in a higher SS. Interface traps and oxide defects in SiC devices can further degrade the SS, especially at high temperatures. The increase in SS with temperature is due to enhanced carrier diffusion and reduced control of the gate over the channel, which is a universal behaviour in MOSFETs but is more pronounced in wide-bandgap materials like SiC. Higher values of SS indicate a shallower, which means more gate voltage is needed for the same current change, reducing switching efficiency and increasing power consumption.

There is a mild change in the slope at higher temperatures, which affects the sub-threshold slope (as shown in Figure 6), and this is detrimental to the switching efficiency of the device. However, even when the temperature is at 300°C, the 4H-SiC MOSFET remains stable during high-temperature and high-power applications, confirming its efficiency.

3.3. Effect of Gate Oxide Thickness on Threshold Voltage

Figure 7 illustrates the drain current Id versus gate voltage Vg characteristics of a SiC MOSFET for different gate oxide thicknesses, highlighting the impact of oxide thickness on the threshold voltage V_{th}.

As gate oxide thickness increases from 30 nm to 210 nm, threshold voltage shifts to higher values, requiring higher gate voltage to activate the MOSFET and allow significant drain current flow. This behaviour occurs because the gate oxide thickness (t_{ox}) directly influences the gate capacitance (C_{ox}), where ϵox is the permittivity of the gate oxide material (as shown in Equation 1). Thinner oxide layers result in a higher gate oxide capacitance, indicating stronger electrostatic control over the channel, which leads to stronger gate control, lower threshold voltage, and higher drain current for the same gate voltage.

The gate oxide capacitance per unit area C_{ox} is calculated using the formula Amirtharajah, R. *et al.* [20]:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (1)$$

where ϵ_{ox} is the permittivity of the oxide material and *tox* is the oxide thickness.

Conversely, thicker oxides reduce the weakening of the gate control, increasing the threshold voltage and lowering the drain current, requiring a higher gate voltage to induce conduction. The observed shift in the Id-Vg curves to the right with increasing oxide thickness demonstrates this relationship, emphasizing how thinner oxides improve device performance by enabling lower threshold voltages and stronger conduction, while thicker oxides lead to higher threshold voltages and reduced current conduction for the same applied gate voltage. This fundamental relationship is critical in 4H-SiC MOSFET design for optimizing switching performance and power efficiency.

4. CONCLUSION

In conclusion, the 4H-SiC MOSFET was developed and designed in COMSOL Multiphysics Semiconductor software, which provides an extensive platform for testing its electrical and thermal characteristics. The device's planar design enabled a thorough assessment of essential parameters such as threshold voltage V_{th} and subthreshold swing (SS) under different thermal and electrical stress conditions. This simulation technique offered a wide observation and analysis of the operation of the MOSFET in real-world scenarios and facilitated the optimization of its design parameters.

The 4H-SiC MOSFET was modeled at 0°C to derive the threshold voltage V_{th}. It was determined to be 3.05 V, which was consistent with the theoretical prediction of 3.05 V ± 0.05 V, resulting in a variance of only 0.1 V. A voltage that is

required for the junction to conduct is referred to as the threshold voltage and is also one of the critical parameters defining the MOSFET operating voltages. A rise in temperature causes a drop in V_{th} due to the narrowing of bandgaps that thermally motivate electron excitation alongside alterations to the energy band structure.

The lower sub-threshold slope value of 41 mV/dec is obtained at 0°C for the device, which increased progressively to reach 128 mV/dec at 300°C. Moreover, the project simulates and investigates how device performance varies with different gate oxide thicknesses and materials. Gate oxide thickness shows that thinner oxides yield lower V_{th} and higher drain current for a given gate voltage. Thicker oxides shift V_{th} higher and reduce drain current due to decreased gate capacitance, weakening gate control over the channel. Thinner oxides are beneficial for fast switching but increase the risk of dielectric breakdown, requiring careful trade-offs in design. High-k dielectrics can improve device performance by increasing C_{ox} without the reliability concerns of ultra-thin SiO_2, enhancing thermal stability and reducing threshold voltage shifts. While thicker gate oxide materials appeared to have the potential to improve thermal stability. Proper engineering of the gate stack can minimize interface trap density, improving channel mobility and subthreshold behaviour.

The study emphasizes the importance of passive thermal management for maintaining device reliability in high-power, high-temperature environments. Integrating robust thermal management mitigates performance degradation and extends device lifespan under extreme conditions. The simulation framework allows for iterative optimization of device parameters, balancing electrical performance with reliability and manufacturability. Overall, this research provides insights into 4H-SiC MOSFET behaviors and offers guidelines for optimizing design in extreme conditions.

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