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Electrical Performance Evaluation Based on Design Parameters of Silicon Nanowire Gate-All-Around (GAA) TFET

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ABSTRACT

The silicon nanowire gate-all-around (SiNW GAA) is one of the technologies with potential for improved short-channel behavior and gate control over conductivity. This work investigates the impact of various geometrical sizes on the electrical properties of SiNW GAA tunneling field-effect transistor (TFET). The gate oxide thickness (T_{OX}), channel radius, type of dielectric, gate metal work function, with low or high drain voltage are varied to analyze the electrical characteristics of SiNW GAA TFET. The electrical characteristics studied in this work consist of subthreshold slope (SS), current ratio, and threshold voltage (Vth). The findings indicate that an oxide thickness of 3 nm, a channel radius ranging from 10 nm to 18 nm, and the use of SiO_2 as a dielectric material are optimal for achieving superior characteristics in SiNW GAA TFETs.. The gate metal TiN exhibits a work function that, in conjunction with a drain voltage of 0.5 V, optimally enhances device performance. This study highlights the potential of GAA nanowire TFETs to drive innovation in semiconductor technology through superior electrical performance.

Keywords: *SiNW GAA TFET; gate oxide thickness TOX; channel radius; dielectric material; gate metal work function; drain biased; Subthreshold Slope (SS); I_{ON}/I_{OFF} current ratio; Threshold Voltage (V_{th})*

1. INTRODUCTION

Metal-oxide-semiconductor field-effect transistor (MOSFET) has been scaled to follow Moore's predicted trends, which leads to extending complementary metal-oxide-semiconductor (CMOS) technology to increasingly smaller technological nodes. However, due to basic physical and technical restrictions, CMOS scaling has deviated from Moore's predicted trends and Dennard scaling's principles [1]. The quantity of transistors on a chip doubles according to Moore's Law [2]. The scaling faces several challenges, including leakage current, static power dissipation, performance limitations due to the subthreshold slope (SS), threshold voltage (Vth) issues, and other related short-channel effects (SCE) [3], [4].

Heat dissipation, leakage current, and channel length modulation have all become significant concerns, which will eventually slow down CMOS scaling as the technology approaches the atomic dimension [5], [6]. Hence, new semiconductor technologies are urgently needed to address challenges such as cost, speed, reliability, and power dissipation. A significant amount of effort has been invested based on nano-electronic-based devices and materials research and development, involving the replacement of existing silicon-based technology, to support the continuous CMOS scaling [7].

In recent decades, bottom-up semiconductor nanowires and their derived field-effect transistors (FETs) have been extensively explored as essential building blocks for the development of advanced devices and circuits. One of the technologies is the smaller channel of a nanowire structure with a higher surface-to-volume ratio than planar devices made of bulk materials. Furthermore, the gate surrounding or gate all around (GAA) structure, which was developed with the nanowire FETs, provides good electrostatic gate control over the nanowire channel. This GAA-based FET technology exhibits excellent resistance to SCE, high packing density, enhanced drain current drivability, and superior overall performance [8].

Silicon nanowire (SiNW) FETs were listed as one of the most promising emerging logic devices and are ideal for ultra-low-power logic circuit integration. However, the configuration has limited reliability, and detailed research needs to be conducted to assess the reliability and performance concerns of these Si-based MOSFETs [9]. In addition to their limitations in fabrication and scaling for threshold voltages, gate oxide thicknesses, and leakage currents, the occurrence of SCEs, such as subthreshold slope (SS) and gate current leakage in the transistor, complicates the scaling process.

On the other hand, further study is required to overcome these problems, and the cylindrical GAA MOSFET is considered a promising device for CMOS technology. Studies in [10] indicate that the GAA FET exhibits superior performance compared to other devices in terms of scaling of SCEs such as SS, threshold voltages (Vth), and I_{ON}/I_{OFF} current ratio. Hence, the cylindrical GAA MOSFET becomes one of the choices to enhance the performance of the nanoscale CMOS development.

This work focuses on analyzing the SiNW FET SCE's device performance based on different design parameters and improving its reliability by optimizing these parameters. The device used in this research study is a cylindrical SiNW GAA TFET, modeled in Silvaco TCAD. This paper also aims to measure the effects of different dielectric materials, various radius ranges, oxide thicknesses, gate metal work functions, as well as different drain biases on the performance of electrical characteristics.

2. METHODOLOGY

2.1. Simulation and Modelling of Si-NW GAA TFET

The Silvaco TCAD suite is employed to model and simulate a silicon nanowire gate-all-around tunneling field-effect transistor (SiNW GAA TFET). Device fabrication is emulated using the Athena process simulator, while Atlas will extract data to investigate the transistor's electrical characteristics, including DC, AC, and transient responses, in both 2D and 3D simulation environments. DeckBuild serves as the primary simulation interface, and TonyPlot is utilized for the visualization and analysis of the output data. The study focuses on an n-type TFET (nTFET), which operates under positive gate and drain bias conditions. The device structure employs cylindrical GAA geometry, implemented through a tailored meshing scheme to ensure enhanced electrostatic control and improved current modulation relative to planar counterparts. This work employed advanced physical models, including non-local band-to-band tunneling, Shockley–Read–Hall (SRH) recombination, and Auger recombination to accurately capture carrier transport and generation-recombination mechanisms. Material definitions and contact configurations are specified within Atlas prior to simulation, and the resulting electrical behavior is evaluated using TonyPlot. Critical geometrical and material parameters—including oxide thickness (T_{OX}), channel radius, dielectric material, as well as gate metal work function are systematically varied to assess their impact on device performance.

2.2. Flowchart

To model the flowchart in Figure 1, the material parameters of the SiNW must be obtained and added to Silvaco's material library. Immediately after adding the material, the software is ready for use in creating the transistor design, then analysing the characteristics of the SiNW transistor. The modelling device used for simulation is SiNW GAA TFET. The designed TFET was studied with various design sizes of channel range radius (R), gate oxide thickness (T_{ox}), dielectric materials, gate metal work function, and drain voltage. These variations were used to evaluate the transistor's electrical performance and analyze parameter variation effects, which consist of SS, V_{TH}, and current ratio. All these design parameters are inputs to the build deck of the Silvaco ATLAS tools.

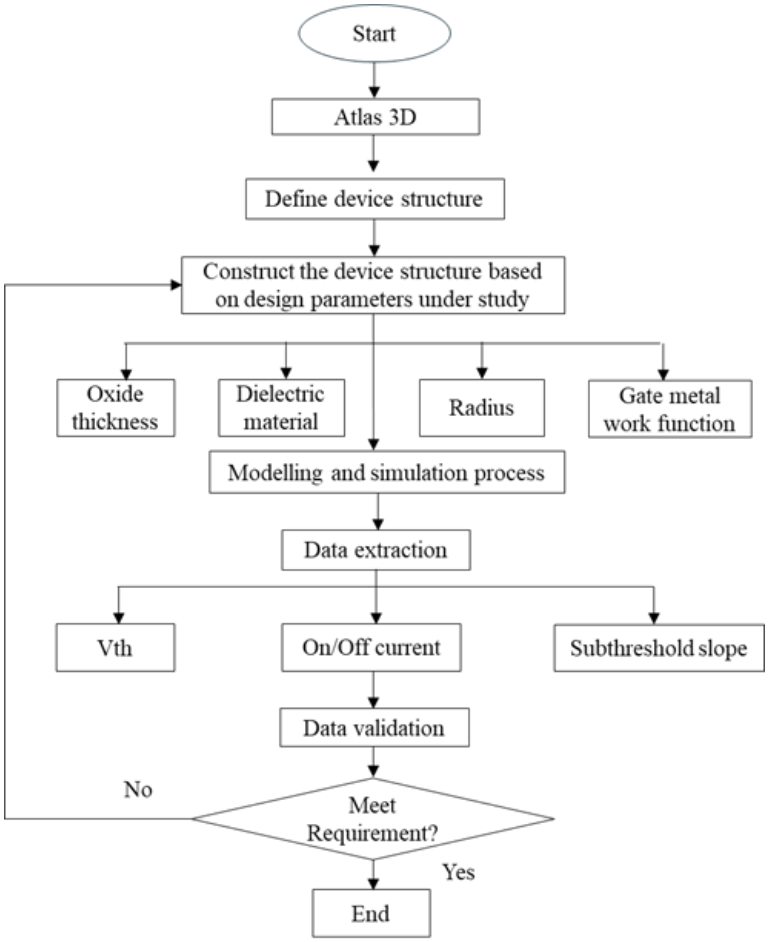

Figure 1. The flowchart of Si-NW GAA TFET modelling using Silvaco TCAD.

2.3. Transistor Parameter and Design Details

The cylindrical GAA MOSFET schematic used for modeling and simulation is shown in Figure 2, with the cross-sectional area of the device highlighted in Figure 3, where the structure was created using Atlas Tools in Silvaco TCAD simulation. This simulation demonstrates the capability of TCAD for SiNW GAA TFET. The TFET operates as a gated p-i-n diode. The source and drain regions are heavily doped. The gate regulates band-to-band tunnelling between the i-channel region and the p+ or n+ region by bending the energy bands within the i-channel region. [1] as in Figure 4. This analysis aims to investigate the electrical performance of SiNW-GAA-TFET at room temperature with applied drain voltages of 1.5 V [11].

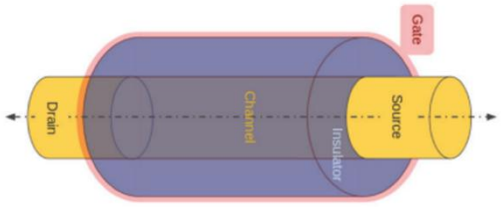

Figure 2. The schematic diagram of the cylindrical SiNW GAA demonstrating the source, drain, gate, and channel [2].

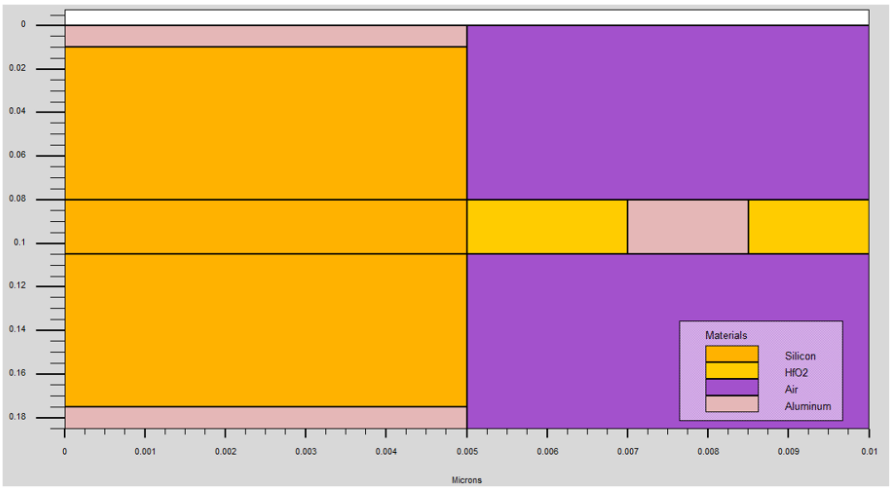

Figure 3. The simulated structure of the SiNW GAA TFET.

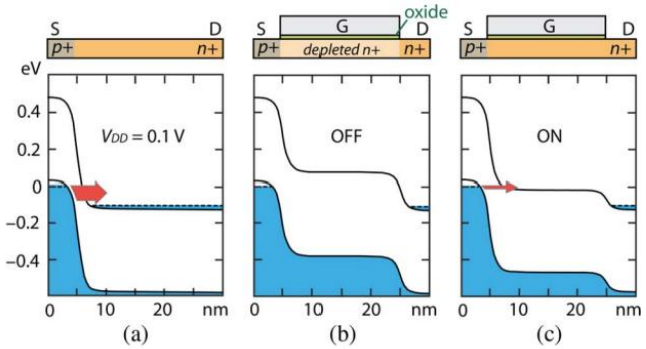

Figure 4. Energy band diagram and structure for TFET (a) Zener tunneling p^+ n^+ channel (b) Gate fully depletes the channel, creating a normally off device. (c) The channel turns on with a positive gate voltage [12].

In this work, the design parameters, including channel radius, dielectric material, thickness of oxide, gate metal work function, and drain bias, were varied to characterize and evaluate the device's performance comprehensively. Specifically, the design parameters are varied based on the details stated in Table 1. Table 2 presents the fixed parameter values when the respective design parameters are varied accordingly. The source and drain of the device are uniformly doped with a concentration of ND = 1×10^{19} cm^{-3}, featuring a channel length of 25 nm, a constant oxide thickness of 2 nm, and a radius of 5 nm. Moreover, HfO_2 has been used as a gate oxide dielectric, and the metal gate work function simulated for the device is $\varphi_M = 4$ eV.

Table 1 Design Parameters of SiNW GAA TFET Model

Parameters	Values	Reference
Channel Radius (R)	5 nm,10 nm, and 18 nm	[13]
Dielectric Material	SiO_2, HfO_2, Al_3O_2	[14], [15], [16]
Oxide Thickness (T_{OX})	2 nm,3 nm, and 4 nm	[3] [13]
Gate Metal Work Function (φ_M)	TaN, TiN, and Au	[17], [18]
Drain Voltage (V_D)	0.5 V, 1.5 V, and 2.5 V	[11][19], [20]

Table 2 Constant Parameters Of SiNW GAA TFET Simulation

Parameters	Values
Channel Radius (R)	5 nm
Dielectric Material	HfO_2
Oxide Thickness (T_{OX})	2 nm
Channel Length (Lg)	25 nm
Source/Drain Doping	1×10^{19} cm^{-3}
Gate Metal Work Function	4
Drain and Source Length	80 nm
Gate Voltage (V_G)	0 to 1 V
Drain Voltage (V_D)	1.5 V
Nanowire Material	Silicon

2.4. Extraction of Electrical Characteristics

2.4.1. Subthreshold Slope (SS)

Subthreshold Slope (SS) quantifies the responsiveness of the drain current to the gate voltage inside the subthreshold zone. The ideal value is 70 mV/dec at room temperature, as stated in [21], which is typically obtained in long-channel devices. The SS reciprocal value, called subthreshold swing, is defined as:

$$S\,s\text{–}\,th = ln\,(10)\,\frac{kt}{q} + (1 + \frac{Cd}{Cox}). \quad (1)$$

2.4.2. I_{ON}/I_{OFF} Current Ratio

The measurement of the current ratio would be made at the I_D–V_G curve line. The I_{ON} would be the current achieved at a logical "high" gate voltage or saturated current mode. The same applies to I_{OFF}, where it represents the drain current with a logical low gate voltage or at 0 V. Both of these curves were measured at a constant drain-source voltage.

2.4.3. Threshold Voltage, V_{TH}

The threshold voltage is a critical electrical property of MOSFETs. It signifies the activation threshold and delineates the subthreshold region from the strong inversion region. Additionally, the threshold voltage is also used to monitor the charge of oxides. Threshold voltage is defined as the gate voltage derived from the linear section of the Ids-Vgs curve, extending from the maximum slope to the point of zero drain current [22]. The drain current of an ideal MOSFET in the linear area is stated by the following:

$$I_D = \frac{\mu CoxW}{L}\,(V_{gs} - V_T - \frac{Vds}{2})\,V_{ds}, \quad (2)$$

where μ denotes the carrier mobility, Cox represents the oxide capacitance, W signifies the channel width, L indicates the channel length, V_{GS} refers to the gate-to-source voltage, V_{DS} pertains to the drain-to-source voltage, and V_{TH} is the threshold voltage.

3. RESULT AND DISCUSSION

The influence of key design parameters—such as oxide thickness, T_{OX}, nanowire radius, and gate dielectric material on the electrical characteristics of SiNW GAA TFETs is analyzed in this part. The evaluation focuses on critical electrical characteristics such as V_{TH}, SS, and the current ratio.

3.1. Effects of Different Oxide Thickness

The thickness of the oxide correlates with the oxide capacitance, as delineated in Equation 3:

$$C_{OX} = \varepsilon_{ox} / T_{OX}, \quad (3)$$

Cox represents the oxide capacitance per unit area, εox denotes the permittivity of the gate dielectric, and Tox indicates the oxide thickness. Figure 5 illustrates the performance of SS due to the variation of oxide thicknesses. The radius is maintained at 5 nm, with HfO_2 as the dielectric material [13][15][23]. Figure 5 illustrates that at a reduced oxide thickness of Tox = 2 nm, the TFET displays maximum subthreshold swing characteristics and also achieves an enhanced subthreshold swing value of 78.3 mV/V at Tox = 4 nm. Improving the SS while increasing the gate oxide thickness has also been proven in [13].

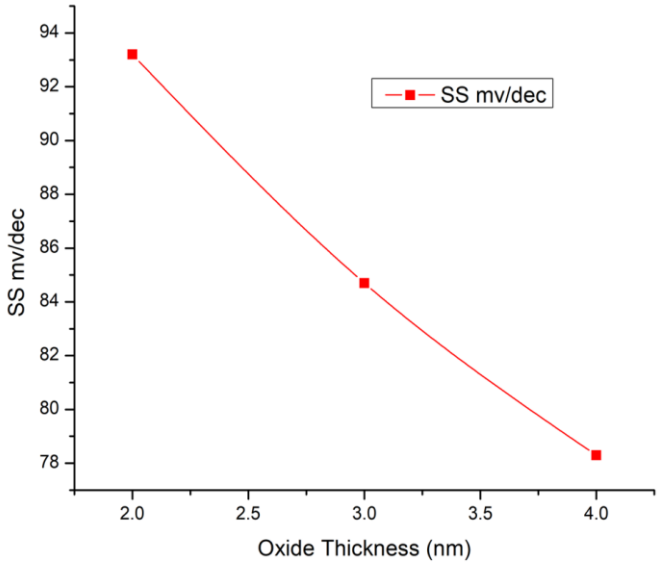

Figure 5. Subthreshold slope with different oxide thicknesses: 2 nm, 3 nm, and 4 nm.

Figure 6 shows the current ratio and V_{TH} values for different oxide thicknesses. The current ratio, $I_{ON}/I_{OFF,}$ where I_{ON} is extracted at V_{gs} = Vdd, and the leakage current, $I_{OFF,}$ is observed at V_{gs} = 0 V [19]. The minimum I_{ON}/I_{OFF} ratio, with V_D = 1 V, was determined to be $0.01x10^3$ at a minimum T_{OX} of 2 nm, subsequently enhanced to $0.10x10^3$ at T_{OX} of 4 nm. Figure 6 illustrates that a gate oxide thickness of 2 nm produces the lowest threshold voltage, whereas an increase in gate oxide thickness elevates the threshold voltage, hence enhancing device performance.

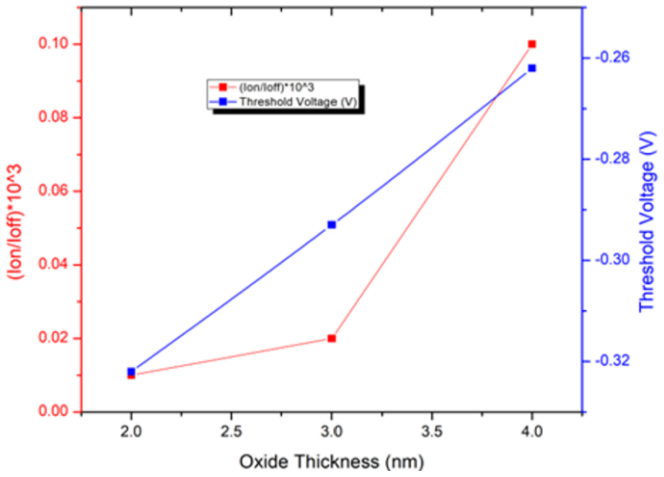

Figure 6. Current ratio and threshold voltage with varying oxide thickness.

3.2. Effects of Different Radius

This section discusses the impact of channel radius on the performance of electrical properties.. The values of radius (R) varied at 5 nm, 10 nm, and 18 nm, while the constant parameters, T_{OX} and dielectric, were measured at 5nm and $HfO_{2,}$ respectively [12][14][22].

Figure 7 illustrates the performance of the SS as a function of the changing channel radius (R). It demonstrates the degradation of SS and high leakage current, which occurred at R = 5 nm, with a slope of 93.2 mV/dec. In comparison, the SS demonstrated significant improvement at R = 10 nm and R = 18 nm, with slopes of 76.9 mV/dec and 75.9 mV/dec, respectively. These values indicate that the SS approaches its ideal value of 70 mV/dec, as also demonstrated in [12].

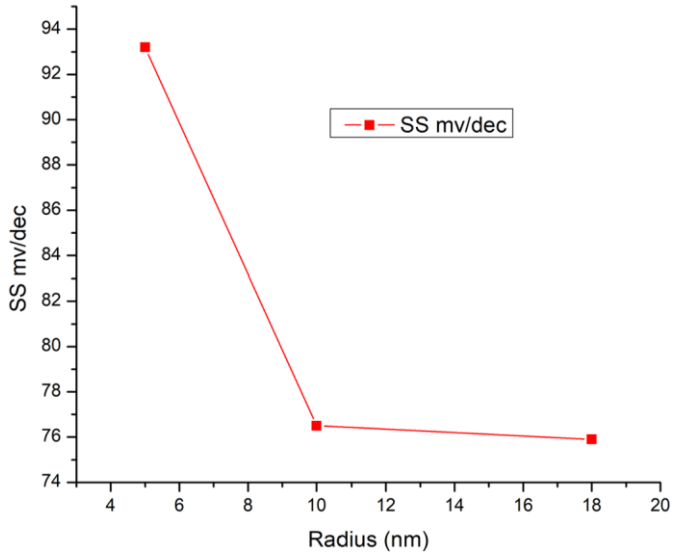

Figure 7. Subthreshold slope with different radius, 5 nm, 10 nm, 18 nm.

Figure 8 illustrates the electrical characteristics of the ION/IOFF ratio and threshold voltage as a function of the varying channel radius.. These two electrical characteristics are proportionally increased with increasing channel radius. It stated that a channel radius higher than 10 nm would improve the I_{ON}/I_{OFF} ratio, where at R = 10 nm, the current ratio value is $0.04*10^3$. At R = 18 nm, the output current ratio reached its optimal value of $0.15*10^3$. However, at the lowest channel radius of 5 nm, the I_{ON}/I_{OFF} ratio decreases to $0.01x10^3$. Additionally, the impact of increasing the channel radius is illustrated, revealing a decrease in the threshold voltage, which fell to -0.32 V at R = 5 nm. The value is slightly improved at R = 10 nm, where the voltage is -0.29 V. The highest channel radius, which is 18 nm, rapidly increases the value at a threshold voltage of -0.11 V.

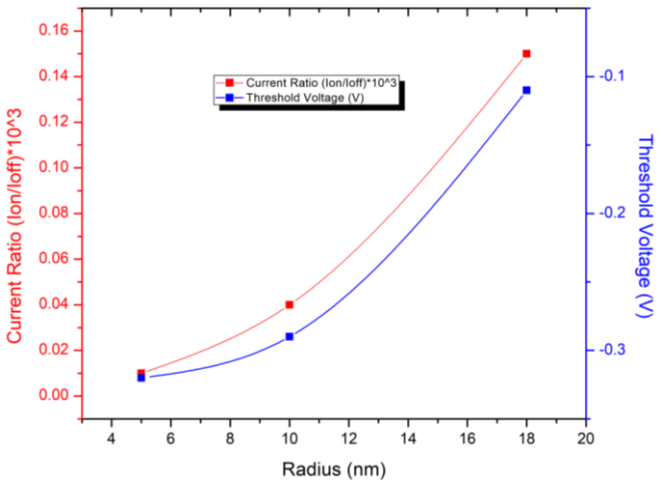

Figure 8. Current ratio and threshold voltage with different radius, 5 nm, 10 nm, 18 nm.

3.3. Effects of Different Types of Dielectric

The electrical characteristics, including the variation of SS, I_{ON}/I_{OFF} ratio, and threshold voltage, are illustrated in Figures 9 and 10. As for the simulation of the different types of dielectric, the various dielectric materials are SiO_2, Al_2O_3, and HfO_2. Figure 9 demonstrates the enhancement of the SS value with the use of superior gate dielectrics in SiNW GAA TFET. The plot demonstrates that SiO_2 and Al_2O_3 have lower SS compared to HfO_2, implying that HfO_2 has inferior SS characteristics compared to these two dielectrics. With a SiO_2 SS value of 57.3 mV/dec, it almost achieves the ideal value of 70 mV/dec.

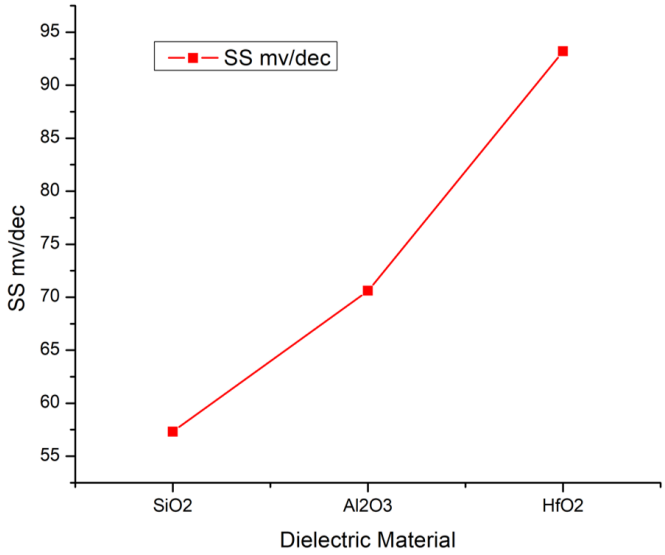

Figure 9. Subthreshold slope with different dielectric materials, SiO_2, AlO_2O_3, and HfO_2.

Figure 10 illustrates the current ratio for different types of dielectric materials. The plot illustrates that the current ratio enhances with the relative dielectric constant of the gate oxide in SiNW GAA TFET, suggesting that SiO2 outperforms Al2O3 and HfO2 as a dielectric material.. This is due to SiO_2 exhibiting significantly lower I_{OFF} current compared to Al_2O_3 and HfO_2, despite having a slightly lower I_{ON} current than both dielectrics. Conversely, regarding the threshold voltage, it further indicates that SiO_2 outperforms Al_2O_3 and HfO_2, consistent with the findings in [23], as HfO_2 exhibits better characteristic performance. Higher k-values are typically associated with a greater density of interfacial trap charges, which can contribute to performance reduction in high-k dielectric devices [24].

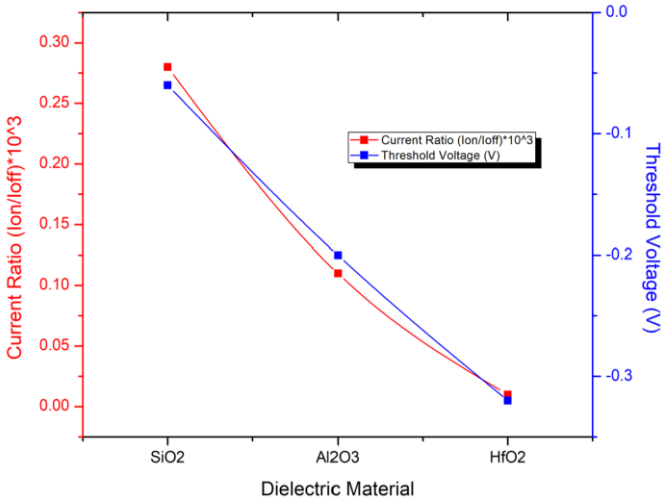

Figure 10. Current ratio and threshold voltage with different dielectric materials, SiO_2, AlO_2O_3, and HfO_2.

3.4. Effects of Different Gate Metal Work Functions

This section simulates the SiNW GAA TFET using three distinct gate metal work functions: 4 eV for TaN, 4.4 eV for TiN, and 4.8 eV for Au. Figures 11 and 12 exhibit the electrical properties of various gate metal work functions.

Figure 11 demonstrates that an increase in the work function of the gate metal correlates with an enhancement in the value of the subthreshold swing (SS). It demonstrates that 4.4 eV TiN and 4.8 eV Au obtain slightly better than the ideal value of 70 mV/dec.

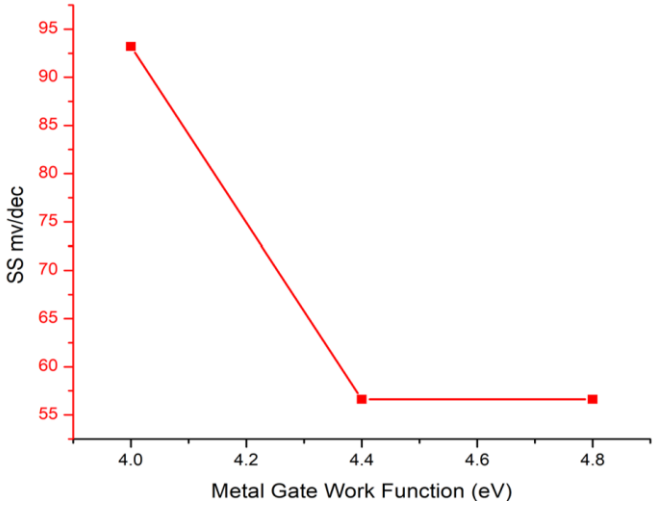

Figure 11. Subthreshold slope with different gate metal work function.

Figure 12 illustrates the variations in current ratio and threshold voltage according to various gate metal work functions. From the results, it is concluded that the 4.8 eV Au has the least current ratio, while the 4.4 eV TiN has the best performance in terms of current ratio, being slightly better than the 4.4 eV TaN. As the metal gate's work function grows, the threshold voltage values correspondingly rise. The findings of the three performance characteristics indicate that the work function of 4.4 eV TiN is the most optimal and stable gate metal, as demonstrated in [25]. The optimal work function is 4.5 eV, as it has the ideal SS, and acceptable values of current ratio and threshold voltage. Additionally, TiN is an ideal metal gate material for advanced MOSFETs due to its wide work function tunability (4.52–4.03 eV), along with excellent thermal and chemical stability, rendering it perfectly suited for low-power, low-voltage functionality [26].

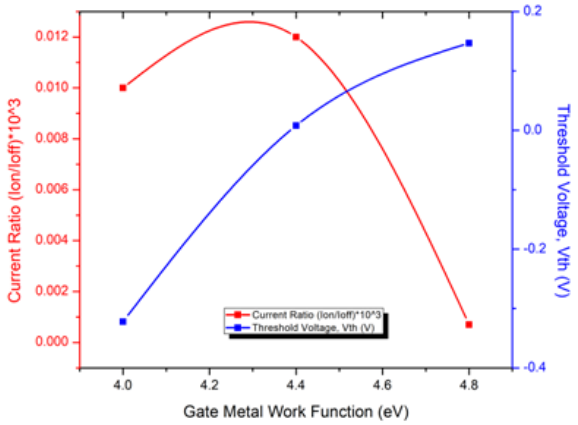

Figure 12. Current ratio and threshold voltage with gate metal work function.

3.5. Effects Of Different Drain Voltages

The effect of different drain voltages has been simulated for the studied device, with drain voltage variations of 0.5 V, 1.5 V, and 2.5 V. Figure 13 depicts the performance of the SS in relation to variations in drain voltage. It demonstrates that the degradation of SS occurs at 0.5 V and 1.5 V, where the two-drain voltage values are almost the same in terms of their SS. In contrast, the increasing drain voltage at 2.5 V results in improved performance of the SS, where it nearly reaches the 50 mV/dec, resulting in a low leakage current. However, it decreases in performance, as illustrated in Figure 14, where studies in [20] demonstrate that increasing the supply voltage would lead the device to suffer from high SCEs.

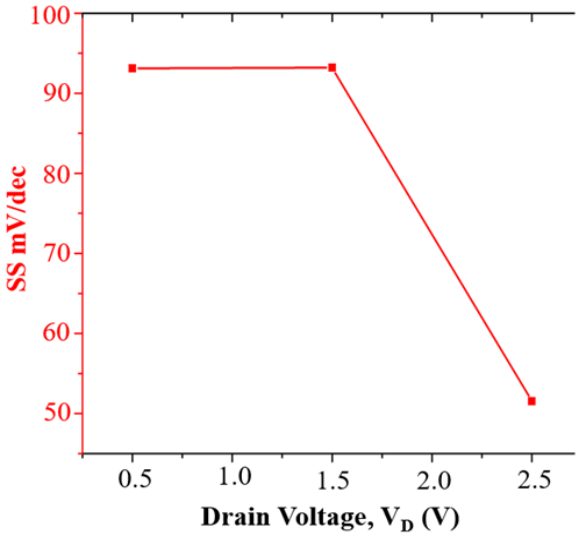

Figure 13. Subthreshold slope with different drain voltage, 0.5 V, 1.5 V, and 2.5 V (V_D).

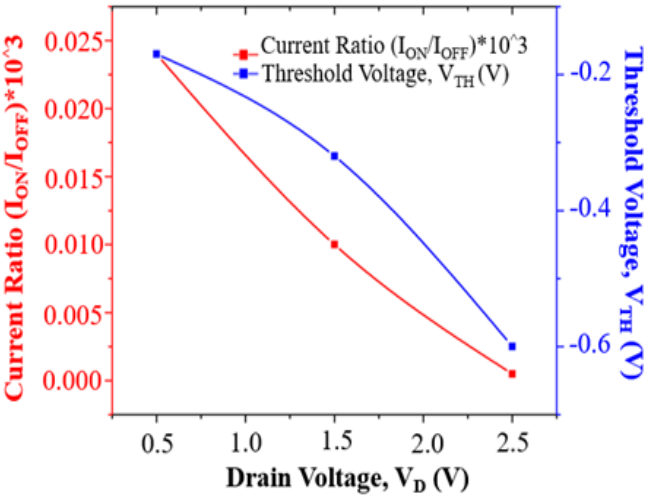

Figure 14. Current ratio and threshold voltage with different drain voltage (V_D).

Figure 14 presents the subsequent results, demonstrating the variation of I_{ON}/I_{OFF} and threshold voltage across three different values of drain voltage, where the characteristics' performance indicates a similar response. As the drain voltage rises, both the current ratio and threshold voltage drop. Therefore, the results show that the device performs best when the drain voltage is set to 0.5 V because it can stabilise the SCEs, as described in [19].

4. CONCLUSION

Various simulation results for the SiNW GAA TFET structure are presented in this research paper. The study indicates that variations in oxide thickness, channel radius, dielectric material, gate metal work function, and drain voltage significantly influence the performance of the device. These factors affect key parameters, including subthreshold slope (SS), the ION/IOFF current ratio, and threshold voltage. The findings indicate that the optimal oxide thickness, which exhibits superior parameter characteristics, is 4 nm. This thickness results in an acceptable value for subthreshold swing (SS), the ION/IOFF current ratio, and threshold voltage. The optimal channel radius for achieving satisfactory performance characteristics is between 10 nm and 18 nm. Additionally, the change in dielectric material from SiO_2 to Al_2O_3 and HfO_2 demonstrates that the SiO_2 dielectric yields the best characteristics for this device modelling. Notably, 4.4 eV which is the work function of TiN is the most suitable gate metal with its stability in characterization of the simulation, while the effective value of drain voltage for the SiNW GAA TFET is at 0.5 V. These findings provide a foundation for future experimental validation through fabrication and characterization of SiNW GAA TFET prototypes, which would help verify the simulation outcomes and assess their applicability under real-world conditions.

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