International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

A modified feed-forward linearization of a unique Kapu optimizer CMOS LNA

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Received 29 December 2024, Revised 26 February 2025, Accepted 15 April 2025

ABSTRACT

This study handles the challenges of RF amplifiers at the sub-nanometer scale in 5G systems by developing a high-performance Low Noise Amplifier (LNA) utilizing 45nm CMOS technology. A modified Feed-forward Distortion Cancellation Technique (FFDCT) improves linearity using the Cadence AWR Design Environment, Version 22.1. The design achieves an ultra-low noise figure through three techniques: cascode Inductive Source Degeneration (ISD), optimized by a unique Kapu optimizer, and a modified FFDCT, which enhances the third-order intercept point and minimizes distortion within noise cancellation parameters. A mathematical approach is presented to design the proposed LNA and the modified FFDCT. Thus, the optimized cascode ISD LNA demonstrates favorable tradeoffs among gain, linearity, noise figure, and power consumption. The proposed LNA design demonstrates a nearly flat gain of 27.9dB, an ultra-low noise figure of 0.025dB at 5GHz, and an IIP3 of -14.66 dBm while consuming 1.224 mW of power. As a result of the proposed FFDCT, both NF cancellation and distortion cancellation transpired, which exhibits a minimum noise figure of 0.554dB and an enhanced third-order input intercept (IIP3) of 14.36dB, with a power dissipation of 2.448mW, achieved through the utilization of an auxiliary low-noise amplifier under a 0.6V power supply, which is suitable for wireless applications.

Keywords: *Feed-forward linearization, IIP3, Inductive source degeneration, Kapu optimizer, LNA, Wireless communication.*

1. INTRODUCTION

The expansion of 5G technology is currently in its middle stage, growing faster than previous generations [1]. The development of low-noise amplifiers (LNAs) in the 5G/6G context is critical for achieving high gain and low Noise Figure (NF) [2]. However, implementing broadband LNAs using CMOS technology faces challenges due to parasitic effects and a lower quality factor of passive components, which increases NF. Overcoming these challenges is essential for advancing CMOS-based LNAs, which are important for mobile communication and radar systems. Analog circuit design involves trade-offs among various parameters, such as conversion gain, noise, linearity, supply voltage, and power consumption. The common source (CS) topology is a widely used LNA configuration, despite the inherent trade-offs in LNA design [3, 4]. Table 1 presents a comparison of various LNA topologies [5]. The common source (CS) topology is the most frequently employed configuration for LNA design among the available choices [6, 7].

Table 1. Comparison of LNA Topologies.

Topology	Bandwidth	Gain	NF	P_{dc}	Linearity
Resistive Feedback	High	Moderate	Low	High	Better
Common Gate	High	Low	High	Moderate	Best
Common Source	Low	High	Low	Low	Good
Cascode CS	High	High	Low	Moderate	Best
Current reuse	Low	High	High	Low	Good

- **INDUCTIVE SOURCE DEGENERATION (ISD)**

The common-source (CS) configuration is a fundamental component of the low-noise amplifier (LNA), providing initial amplification. It consists of a transistor with its source connected to the ground through an inductor, known as inductive degeneration. This setup helps stabilize the input impedance, enhance linearity by reducing distortion, and improve noise performance by generating less thermal noise compared to resistive degeneration [8]. The cascode configuration, which adds a second transistor on top of the CS stage, further improves performance by increasing gain, reducing the Miller effect (feedback capacitance), and minimizing parasitic capacitances, thereby enhancing bandwidth. An input-matching network, typically composed of inductors and capacitors, adjusts the antenna's impedance (usually 50 ohms) to match the LNA's input impedance [6]. A self-biased active inductor with shunt peaking was utilized to achieve a compact and wideband response. A cross-coupled capacitor introduces a

feedforward path, enhancing bandwidth (BW) by compensating gain reduction and generating negative capacitance to counteract parasitic effects, which is a widely used topology in millimeter-wave applications [9]. The approach enhances input matching bandwidth by utilizing a dual-resonant S11 and increases gain bandwidth through a transformer-based second-order bandpass output network. A 27–46 GHz LNA prototype, fabricated in the GlobalFoundries 45-nm CMOS SOI process [10]. To improve low noise amplifiers (LNAs). The proposed LNA is designed for mid-band 5G (3- 4 GHz) wireless receivers and is based on a cascode topology. An auxiliary transistor provides a feedforward correction path for third-order intermodulation (IM3) cancellation. The effects of the second harmonic on the IM3 are also considered in the modeling [11]. By employing an active feedforward stage in the main path, the current dissipation and the thermal noise are effectively suppressed, while the noise and distortion cancellation properties of CG-CS topology are preserved. Moreover, no extra noise is introduced since the additional gm-boost amplifier follows the same noise-canceling (NC) principle as the CG amplifier, and its noise can be fully canceled at the output theoretically. Thus, the proposed LNA benefits from the gm-boosting and NC technique simultaneously to obtain a good tradeoff between gain, noise figure (NF), and power consumption [12]. Another paper presents the optimization of a Variable Gain Low-Noise Amplifier (VG-LNA) using Particle Swarm Optimization (PSO), Firefly Algorithm (FA), and Genetic Algorithm (GA). Among these, FA outperforms GA and PSO, achieving optimal performance in a CCG-VGA-based design with Gm-boosted gain and current-reuse power efficiency [13].

Similarly, the output matching network aligns the LNA's output impedance with the next stage in the RF chain for efficient power transfer [6, 14]. By combining inductive source degeneration (ISD) with the cascode CS configuration, this LNA design achieves a balanced performance, making it suitable for various high-frequency applications. These include wireless communication technologies like mobile phones, Wi-Fi, Bluetooth, and satellite systems, as well as radar systems, radio astronomy, military systems, and medical imaging, where enhancing signal reception and sensitivity is crucial. For high-frequency applications, an ISD, as depicted in Figure 1, is employed. By selecting the source inductance L_s in this configuration, it is feasible to alter the inductive source degeneration and enhance the input impedance by adjusting the real component of the input impedance [5].

● FEED-FORWARD DISTORTION CANCELLATION TECHNIQUE (FFDCT)

Linearization strategies for improving both second- and third-order intercept points (IIP2 and IIP3) in low-noise amplifiers (LNAs) are categorized into five groups: (a) Feedback, (b) Feed-forward (FF), (c) Complementary Derivative Superposition (CDS), (d) Noise/Distortion Cancellation, and (e) Post Distortion (PD) [15]. The FF technique, which has gained renewed interest, is particularly effective in RF applications where signal integrity is crucial. It works by generating a corrective signal that mitigates distortion caused by amplifier nonlinearities, ensuring a more accurate output signal [16]. In the case of a weakly nonlinear amplifier, the nonlinearity of MOS transistors causes the LNA built-in CMOS to exhibit nonlinearity. The relationship between its input and output can be expressed as

$$Y = g_1X + g_2X^2 + g_3X^3 \quad (1)$$

The primary goal of linearization is to minimize the second and third-order nonlinearity coefficients (g_2 and g_3) in the relationship between the input and output signals, retaining primarily the linear component (g_1). This reduces distortion and maintains signal fidelity. Key forms of distortion in communication systems include intermodulation distortion, where non-linearities cause interactions between signals at different frequencies, producing new frequency components. Third-order intermodulation products (IM3), arising from combinations like $2f_1 - f_2$ and $2f_2 - f_1$, are particularly significant in affecting signal quality [3]. The FF technique, while focusing on maintaining linearity, must also ensure that it does not significantly degrade the noise figure (NF). It is highly suitable for high-performance RF, wireless communication, satellite communication, and military and aerospace applications [7]. Double feedforward and noise and distortion cancellation balun LNA, this LNA consists of a common gate followed by a common source stage, where instead of resistive loads around the transistors, the transistors themselves are biased near saturation. This enables low supply voltage, without loss of gain. The feed-forward method proposed increases the gain of the LNA and decreases the NF [17]. A straightforward feed-forward distortion circuit (FDC) was proposed based on an ac-coupled diode-connected NMOS of proper size. The circuit is a feed-forward element that introduces feed-forward meta-distortion components since it has no feedback path. The 3rd-order nonlinearity of the cascode pair partially canceled out these distortion components, thereby enhancing the overall linearity of the LNA [18]. In this paper, a wideband LNA is based on the reused topology from the current proposal. A structure further commonly used for input impedance matching uses the common source with inductive degeneration and RC shunt feedback. The inductive series peaking technique is used to broaden the bandwidth. Then, in the second stage, two complementary linear structures are used, which have a high gain without consuming significant power. Moreover, the power consumption is decreased further using self-forward-body-bias (SFBB) when controlling using the supply voltage [19]. An LNA of a wideband linearization technique for third-order intercept point improvement in low noise amplifiers. The LNA was proposed as a cascade-based architecture targeting mid-band (3- 4GHz) 5G wireless receivers. A feed-forward correction path for third-order intermodulation cancellation is provided by an auxiliary transistor. The impact of the second harmonic on IM3 is also taken into account in modeling [11]. In an X-band linearization technique, low-frequency second-order intermodulation is generated and injected to suppress third-order intermodulation. An RF receiver front-end (RFE) based on a linearization technique is presented,

where a low-noise amplifier and a down-conversion mixer are linearized, operating at a frequency of 900 MHz [20].

This work uses 45nm technologies via Cadence AWR Design Environment, Version 22.1, to construct an LNA for the RF front end with high gain, low noise figure, low consumption power, and excellent input and output impedance matching. LNA's main challenge is delivering superior performance and comparing cascode LNA in 5G wireless applications. This essay's LNA design considerations are included in Section 2. The proposed design of Feed-forward Linearization Strategies for IM3 Distortion suppression and its analysis are presented in Section 3, and the simulation results of the proposed designs and discussion are presented in Section 4. The job is finally concluded in the last section.

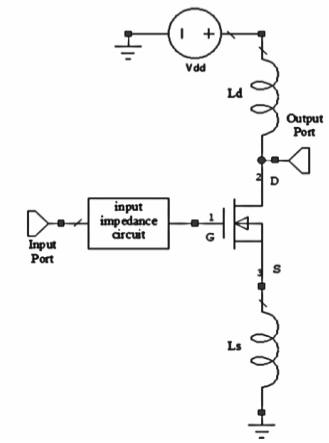

Figure 1. The basic schematic of ISD topology.

2. DESIGN ANALYSIS OF PROPOSED LNA

The ISD topology has a narrowband characteristic as a result of the resonance of the input matching circuit. This circuit consists of the source inductance (L_s) and the gate-to-source capacitance (C_{gs}) at a certain frequency. The ISD LNA is commonly used in narrowband systems because of its advantageous features, such as low NF and high gain with good input matching. Equation (2) describes the input impedance of the stage, but equation (3) pertains to another characteristic of the stage.

$$z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \quad (2)$$

$$Z_{in} \approx \omega_T L_s \ (at\ resonance) \quad (3)$$

where: L_g: Gate inductance,

g_m: Transconductance of the device,

and $\omega_T = 2\pi f_T$, where f_T is the unity gain frequency of the transistor.

In Figure 2, an ISD has a circuit displayed to determine the input impedance [3, 21]. This indicates that the input impedance of the ISD circuit is directly proportional to L_s. As pure reactance is devoid of noise, this enhancement led to an improvement in noise performance. Nevertheless, the disadvantage of this design is that the inductor is located off-chip at low frequencies, which makes it most suitable for narrowband applications [3].

Equation (2) establishes a direct relationship between the input impedance of the inductive degeneration circuit and the value of L_s. The enhanced noise performance was achieved due to the absence of thermal noise in L_s, as pure reactance is noiseless. It is essential to ensure that the input impedance is set to 50Ω by matching the real impedance. Therefore, while in resonance, the resulting impedance is equal to the source resistor (R_s) as determined by

$$ReZ_{in} = g_m \frac{L_s}{C_{gs}} = R_s = 50\Omega \quad (4)[21]$$

Figure 2 illustrates a CS LNA that incorporates ISD and utilizes only one active component. The 50 Ohm resistor R_s is connected to the input terminal of the LNA, resulting in input matching. The amplifier's bandwidth is extensive and determined by the transistor M1's C_{gs}. By connecting the inductance L_g to the gate of NMOS, the capacitance C_{gs} of M1 is eliminated at the resonant frequency. As a result, the impedance at the input of NMOS becomes entirely resistive, particularly known as the input resistance R_{in}.

When choosing an IC foundry and processing, the device length of MOSFETs is significant because it directly affects the total area of the IC die, affecting cost, performance speed, current drain, maximum data rate, and other factors. The rationale is straightforward: digital IC circuit design requires hundreds or even thousands of transistors. Decreasing the device length substantially reduces the total area of the IC die and, hence, the cost. Scientists and engineers at IC have diligently reduced the size of transistors, which are currently reaching minimal dimensions. Most MOS IC foundries commonly find device lengths of 0.25, 0.18, 0.13, 0.11, 0.09, 0.045, and even 0.028 μm [7, 22].

The subsequent text will outline a design technique for a degeneration CS LNA; some transistor parameters for 45nm technology are:

T_{ox}= 1 nm, μ_n=130 cm^2/V-s for a gate length of L = 45 nm. The drain current is I_d=0.1 mA, V_{dd} = 0.6 V.

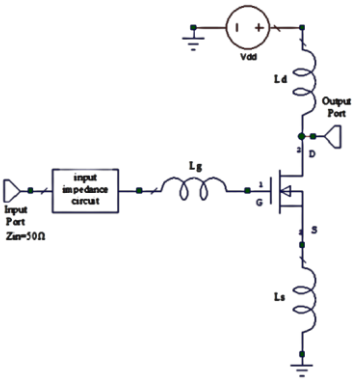

Figure 2. ISD LNA with L_g.

Theoretically, anticipating low noise levels results in a more rational choice of the device's dimensions in an LNA design. Power consumption needs to be taken into account to determine the ideal width (W) of a device for the NF.

$$W = \frac{1}{3w_o L C_{ox} R_s} \quad \text{nm} \tag{5}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d} \qquad \frac{A}{V} \tag{6}$$

Equation (5) demonstrates that g_m increases in direct proportion to the square root of the ratio W/L. An increase in g_m is equivalent to a rise in the W/L ratio. ω_o is the resonance frequency, specifically set at 5GHz. C_{ox} refers to the oxide capacitance, while T_{ox} represents the gate oxide thickness and $\varepsilon_{ox}=3.9\varepsilon_o$ for SiO_2. Lastly, μ_n indicates the mobility of charge carriers. The designer is mindful of the initial two parameters, ω_o and R_S. The IC foundry provides a variety of options and provides the last two parameters, C_{ox} and L. The IC foundry data enables the computation of the values of W using expression (5).

$$C_{gst} = \frac{g_m L_S}{R_S} \qquad F \tag{7}$$

The C_{gst} represents the total capacitance between the gate and the source of the input transistor. However, this transistor already has junction overlap parasitic capacitances called $C_{gs\text{-}mos}$, which may be calculated as,

$$C_{gs-mos} = \frac{2}{3} W L C_{ox} \qquad F \tag{8}$$

Thus, to compensate for the extra C_{gs}, an external capacitance has to be connected.

$$C_{gs-ext} = C_{gst} - C_{gs-mos} \quad F \tag{9}$$

L_s is 0.5 nH [7, 22, 23].

$$L_g = \frac{1}{w_o^2 C_{gst}} - L_s \qquad H \tag{10}$$

Computing the threshold voltage (V_{th}) is the second stage in developing the NMOS.

$$V_{Th} = \varphi_{MS} + 2\,\varphi_F + \frac{Q_{dep}}{C_{ox}} \tag{11}$$

where φ_{MS} is the difference between the work functions of the polysilicon gate and the minimal silicon substrate, approaching zero, $\varphi_F = (kT/q)\ \ln(N_{sub}/n_i)$, k is Boltzmann's constant, q is the electron charge, N_{sub} is the doping density of the substrate ($1*10^{15}$), n_i is the density of electrons in undoped silicon ($145*10^8$), Q_{dep} is the charge in the depletion region. From pn junction theory, $Q_{dep} = \sqrt{4q\varepsilon_{si}|\varphi_F|N_{Sub}}$ where ε_{si} denotes the dielectric constant of silicon ($11.7\varepsilon_o$). The doping density impacts the NF of the LNA by affecting the thermal noise. Higher inherent noise is generally observed when the doping densities are lower due to the increased channel resistance. In the context of low noise figure designs, particularly in advanced technology nodes such as 45nm, having an excessively low doping density might have a detrimental effect on the NF. The V_{th}, decreases when the doping density decreases, typically leading to a decrease in the threshold voltage, which can be advantageous for minimizing power consumption and enhancing g_m. Nevertheless, it can also impact the device's linearity and leakage currents. Thorough analysis and fine-tuning of the design parameters are essential to attain the desired performance while effectively addressing any possible downsides related to this doping density [22].

An inductor is a superior option for a circuit compared to resistance, as resistance limits circuit performance and is incapable of achieving the intended results. Utilizing L as a load in amplifier design eliminates the limitations observed in circuits employing resistance as a load. Using LC as a load produces better results since the inductor used in the circuit is assumed to be a genuine inductor [10].

$$R_1 = \frac{A_v}{g_m} \qquad \Omega \tag{12}$$

$$L_d = \frac{1}{\omega_o Q} \qquad H \tag{13}$$

$$C_d = \frac{1}{\omega_o^2 L_d} \qquad F \tag{14}$$

The voltage gain is represented by Av, whereas the quality factor is denoted as Q, with a value of 3.858.

An LC filter is employed at the input of the bandpass filter techniques to provide input impedance matching and reduce return loss. It offers restricted bandwidth. Figure 3 shows the configuration of a bandpass filter. The parallel inductor and series capacitors are incorporated to enhance the input-matching impedance of the entire circuit. On the other hand, the capacitors C_b serve as blocking capacitors with a high capacitance value, resulting in an impedance close to zero at their respective operating frequencies.

The problem of stability is of great importance when it comes to LNA. Undesired fluctuations will be generated if a portion of the output power is reflected to the input. Afterward, the LNA will display instability. The Rollett factor is a standardized metric used to evaluate the stability of the LNA [3, 22].

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+\Delta^2}{2|S_{12}S_{21}|} \tag{15}$$

where $\Delta = S_{11}\,S_{22} - S_{12}\,S_{21}$. The LNA exhibits unconditional stability when the value of K is greater than 1.

The cascode amplifier with ISD, as shown in Figure 4, is a frequently employed technique for the creation of LNAs. The CS stage is crucial in the building of the cascode amplifier since the amplifier's NF relies on this stage to get optimal performance. The gate-to-source voltage (V_{gs}) and gate width (W) of the CS stage transistor are manipulated to optimize its performance. The cascode topology exhibits enhanced gain as a result of the amplified output impedance. The cascode transistor mitigates the impact of the Miller capacitance on the reverse isolation. Reducing the parasitic capacitance of the input transistor enhances the amplifier's high-frequency performance [5, 22]. The lower

transistor, M1, acts as a CS amplifier, whereas the upper transistor, M2, functions in the common gate (CG) arrangement and acts as an isolated output node from the input [3, 6]. The noise figure is computed by performing a calculation [6, 23]:

$$NF = 1 + \frac{g_m R_S \gamma}{R_1}\left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_S}{R_1}\left(\frac{\omega_o}{\omega_T}\right)^2 \quad (16)$$

γ represents the parameter that defines the bulk effect.

3. KAPU OPTIMIZATION

AWR is unique in using Kapu optimizer, so there is no research on designing and optimizing ISD LNA.

Kapu optimization for a cascode ISD (LNA) involves fine-tuning the input impedance, power gain, and noise performance parameters to achieve an optimal balance between linearity, gain, NF, and stability. Here's a detailed approach for optimizing Kapu in the context of a cascode ISD LNA:

- **Impedance Matching (Input and Output):** Ensure the LNA input impedance matches the source impedance (typically 50 Ω) to minimize reflections and maximize power transfer.
- **Transistor Sizing (W/L):** changing the W to improve g_m and maintain a balance to prevent excessive parasitic capacitances (C_{gs} and C_{gd}), which degrade gain and bandwidth.
- **Inductive Source Degeneration:** Choose the value of the L_s to stabilize the input impedance. Optimize the inductance for the operating frequency using equation (2)
- **Biasing Conditions:** Optimize V_{gs} and V_{ds} to ensure the transistor operates in the saturation region, which maximizes gain and linearity, besides selecting an appropriate V_{ds} to achieve high reverse isolation and prevent excessive power consumption.
- **Threshold Voltage:** can be advantageous for minimizing power consumption and enhancing g_m.

Table 2. Comparison between the calculated and optimized elements.

Element	Calculation	Optimized
W1 (μm)	164	179
W2 (μm)	164	176
$V_{th}1$ (V)	0.19	0.182
$V_{th}2$ (V)	0.19	0.117
L_s (nH)	0.5	0.3
L_g (nH)	5.64	5.532
$C_{gs\text{-}ext}$ (pF)	0.024	0.03
L (impedance matching)	10.21411842	9.518999
C (impedance matching)	0.087083255	0.089199

3.1. STEPS FOR KAPU OPTIMIZATION

1. **Input Matching Optimization**
✓ Select an appropriate L_g and L_s to ensure equation (4).
✓ Simulate the input return loss (S11) to confirm optimal matching (< -10 dB).
2. **Noise Figure (NF) Minimization**
✓ Reduce NF by optimizing the transistor dimensions and using high-quality inductors.
3. **Gain Maximization**
✓ Ensure high g_m through proper transistor sizing and biasing.
✓ Use cascode topology to suppress the Miller effect and enhance gain
✓ Verify gain using S-parameters (S21 > 20 dB).
4. **Stability Analysis**
✓ Check the Rollett stability factor (K) to ensure unconditional stability in equation (15).
5. **Power Consumption**
✓ Minimize power consumption by selecting an optimal bias voltage and scaling the transistor sizes.
✓ Ensure power dissipation is within the acceptable range for the application.
6. **Simulation and Optimization**
✓ Perform iterative simulations using Cadence AWR.
✓ Analyze S-parameters, NF, and IIP3 to ensure all design goals are met.

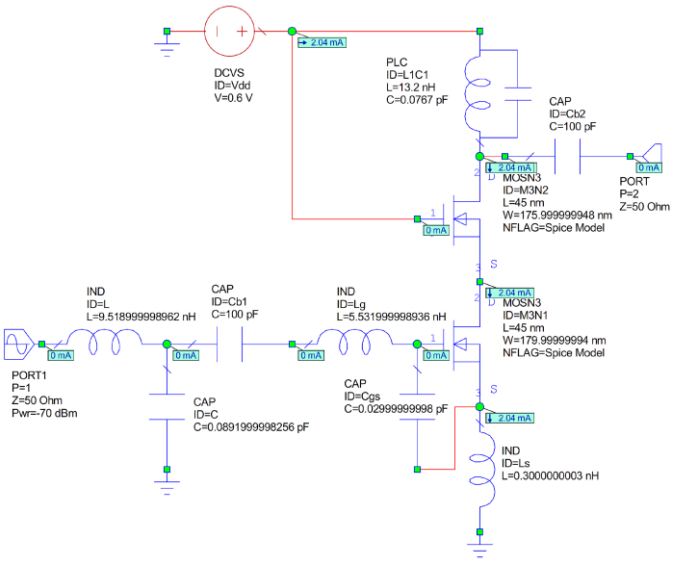

Figure 3. The proposed cascode ISD LNA.

4. THE PROPOSED DESIGN OF MODIFIED FEED-FORWARD DISTORTION CANCELATION STRATEGIES FOR IM3 AND IM5 DISTORTION SUPPRESSION

The architecture of the modified FFDCT is shown in Figure 4. The essential processing steps are:

The primary signal suppression loop has been designed to eliminate the main signal and retrieve the error signal from the main amplifier (MA). The output signal V_P of the MA system consists of a portion of the initial signal V_i that has

been amplified linearly, together with a non-linear distortion part V_d. It can be delivered as:

$$V_p = V_i 10^{\frac{G_1+G_2}{20}} e^{j(\phi_1+\phi_2)} + V_d \quad (17)$$

The output signal of the amplifier is transmitted through a coupler to transfer a portion of the power. The magnitude of the connected signal V_C is precisely equal to that of the reference signal. The input signal V_i goes through a delayer D_1, leading to an output signal V_i' that is not in phase with V_C.

The two V_i' and V_C are input into the power combiner of the main signal suppression loop. The operation of this loop can be described by the following equations.

$$V_c = V_p 10^{\frac{G_3}{20}} e^{j\phi_3} \quad (18)$$

$$V_i' = V_i 10^{\frac{G_1+G_4}{20}} e^{j(\phi_1+\phi_4)} \quad (19)$$

$$V_e = (V_c + V_i') 10^{\frac{G_5}{20}} e^{j\phi_5} \quad (20)$$

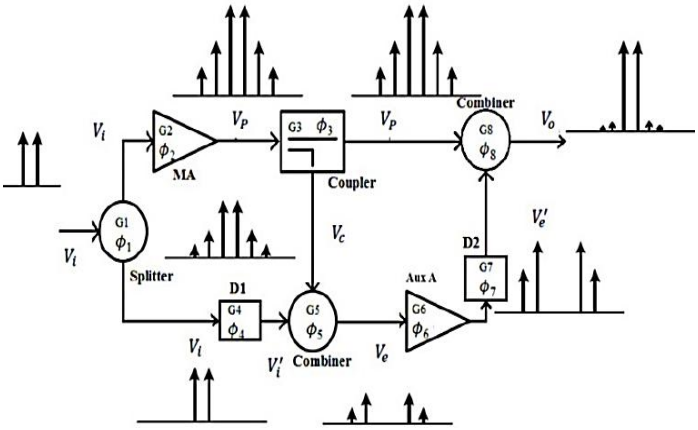

Figure 4. The structure of the modified FFDCT with each item identified by gain (G) and phase ($\boldsymbol{\phi}$).

Due to the phase difference between ϕ_2 and ϕ_4, they exhibit destructive interference, resulting in their cancellation. The splitter, coupler, and power combiner exhibit no phase shifts. As a consequence, ϕ_1, ϕ_3, and ϕ_5 are all equal to zero. Furthermore, it should be noted that the splitter, delayer, and power combiner all possess a gain of zero, denoted as $G_1=G_4=G_5=0$. Therefore, the representation of V_e can be simplified to

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$$V_e = V_d 10^{\frac{G_3}{20}} \quad (21)$$

The error cancellation loop depicted in Figure 5 is specifically designed for amplifying the error signal through the auxiliary amplifier (Aux A), which is the proposed LNA. This amplified signal is then reintroduced into the output power combiner as $-V_d$. This can be accomplished in the following manner.

$$V_e' = V_d 10^{\frac{G_3+G_6+G_7}{20}} e^{j(\phi_6+\phi_7)} \quad (22)$$

Given that V_e' is injected into the output combiner as $-V_d$, the sum of G_3, G_6, and G_7 should be set to zero, and the sum of ϕ_6 and ϕ_7 should be set to $\pm\pi$. Given that the delay line has no amplification, it follows that $G_7=0$ and $G_6=-G_3$. Ultimately, the expression of V_e' is reduced to

$$V_e' = V_d e^{\pm j\pi} \quad (23)$$

The error loop output is integrated into the primary signal channel, thus eliminating the distortion products generated by the main amplifier. The overall output of the amplifier, denoted as V_o, can be expressed as

$$V_o = \left(V_p + V_e'\right) 10^{\frac{G_8}{20}} e^{j\phi_8} \quad (24)$$

Considering that the output combiner has zero gain and zero phase shift, $G_8=0$ and $\phi_8=0$. Finally, Equation (24) is reduced to

$$V_o = V_i 10^{\frac{G_2}{20}} e^{j\phi_2} \quad (25)$$

Once the distortion is eliminated, the FF amplifier will produce a linearly amplified signal that matches the original input signal.

FFDC is a technique used in electronic systems, particularly in RF and microwave amplifiers, to reduce distortion and improve signal quality. Here are some advantages of modified FFDCT over other techniques: High Linearity Improvement, Broadband Performance, Stability, Preservation of Bandwidth, Compatibility with Digital and Analog Signals, and Flexibility in Design.

5. SIMULATION RESULTS OF THE PROPOSED DESIGN AND DISCUSSION

The optimized cascode ISD LNA is simulated using 45 nm NMOS technology with a 0.6V power supply. All the experiments are carried out under the Cadence AWR Design Environment, Version 22.1.

The main purpose of this research is to provide low power consumption, a low noise figure, high linearity, and significant gain, making it an excellent choice for high-performance systems. The combination of these parameters ensures that the LNA can effectively amplify weak signals while maintaining low noise and high linearity, which is essential for applications such as 5G communication and radar systems. Figure 3 illustrates the proposed design of the LNA.

The LNA's sensitivity and capability to amplify extremely weak signals are demonstrated by its ability to handle input

power as low as -70 dBm (0.1 mV). This is crucial for 5GHz communication systems. In Figure 6, S21 indicates the amplification level, which is very high (27.9 dB), while S12 indicates the level of reverse isolation, which is very low (-65.8 dB). S11 is a pretty good indication of the input match (-52.4 dB), and S22 indicates the output match, which is excellent (-0.111 dB).

The optimized cascode ISD LNA score's NF of 0.0255 dB is remarkably low, as shown in Figure 7, representing exceptional noise performance, and the LNA's minimum noise figure (NFmin) is $9.8*10^{-8}$ dB, which is exceptionally low and suggests that it introduces minimal noise under optimal circumstances.

Two tones have been applied to the proposed modified FFDCT 4.8GHz and 5.2GHz; Figure 8 shows, at each node of the FFDCT structure according to the test point location, NF and IIP3 of the optimized cascode ISD LNA with modified FFDCT that have been shown in Figure 5, which indicate -14.6 dB for the proposed LNA give unsatisfactory linearity while providing 14.36 dB IIP3 after applying modified FFDCT that the LNA can handle relatively strong signals without significant distortion and specify good linearity. The red line shows the NF after applying the modified FFDCT with the same S21.

As indicated, Figures 3 and 9 show the bias current, which is 2.04 mA, which means the consumption power of the LNA is 1.224 mW, even when used twice in a modified FFDCT application (total power consumption of 2.448 mW), which is suitable for various applications that require low power consumption, high linearity, and good noise performance.

When applying two tones (4.8 GHz and 5.2 GHz) with higher input power, the cancellation of the IM3 and IM5 is extremely evident, as shown in Figure 10. The comparison table provides a detailed analysis of various LNA designs and their performance metrics, demonstrating significant advancements in this work. Notably, the S21 in this work reaches 27.9 dB, which is a considerable improvement over earlier designs that varied between 5 dB and 23.5 dB. The NF is drastically reduced to 0.025 dB, which is an exceptional improvement in minimizing noise compared to other designs, which range from 1 to 5.5 dB. Additionally, the power dissipation (Pdc) is minimized to 2.448 mW, showcasing an efficient design with lower power consumption compared to previous works, where power dissipation varied from 4.1 mW to 45 mW. This design also achieves a suitable IIP3 of 14.36 dBm for low power levels, indicating improved linearity and signal handling capabilities over earlier designs, which had values ranging from -14 dBm to 18 dBm. These enhancements in gain, noise figure, power efficiency, and linearity highlight the substantial progress made in this LNA design, optimizing performance for modern applications.

Optimization Tips are: Trade-off is prepared to compromise between NF, gain, and power consumption based on application needs. Advanced techniques incorporate feedforward and cascode ISD mechanisms for better linearity and distortion cancellation. By following this methodology, Kapu optimization for a cascode ISD LNA can be achieved effectively, resulting in a high-performance amplifier for 5 GHz applications.

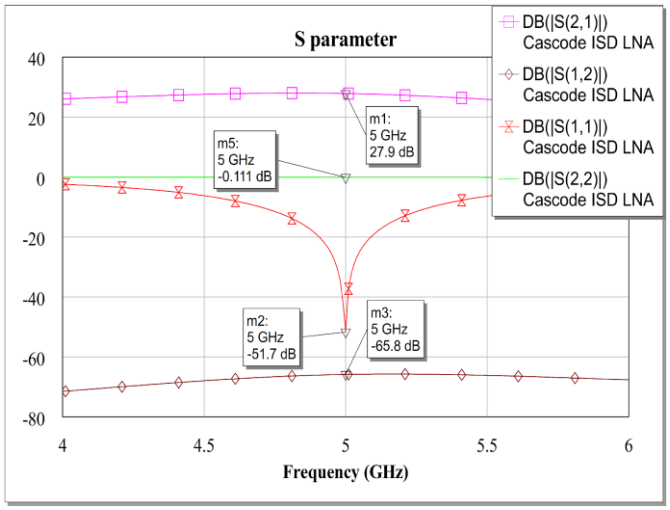

Figure 6. The S-parameter of the proposed cascode ISD LNA at 5 GHz center frequency.

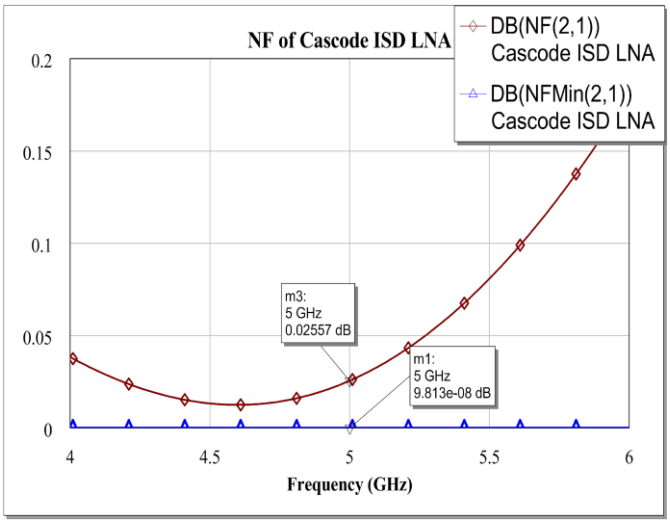

Figure 7. NF and NFmin of the proposed cascode ISD LNA at 5 GHz center frequency.

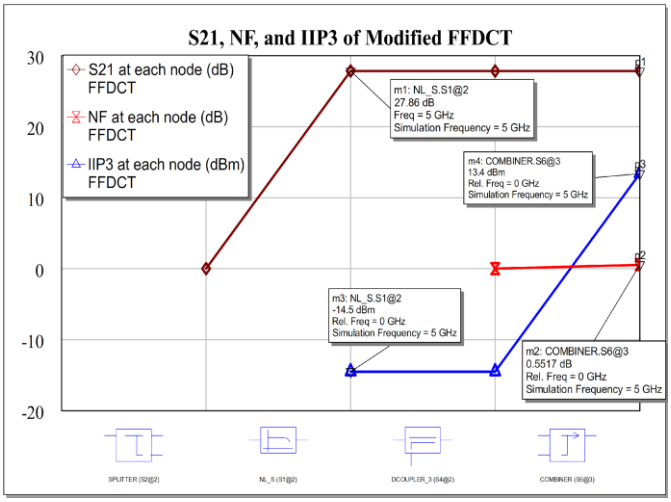

Figure 8. The IM3 and IIP3 of modified FFDCT LNA.

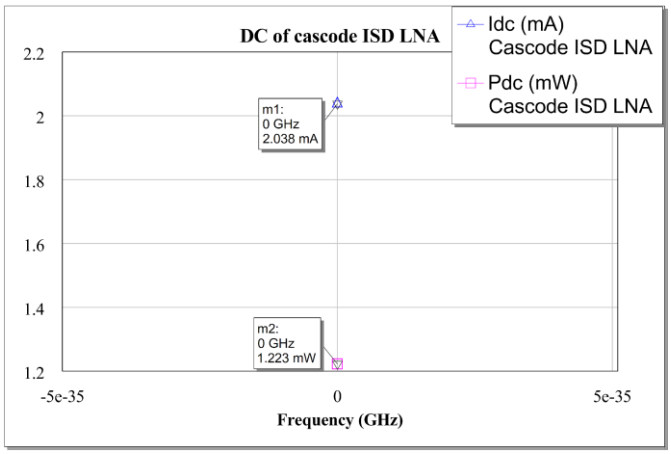

Figure 9. Bias current and consumption power of the optimized cascode ISD LNA at 5 GHz center frequency.

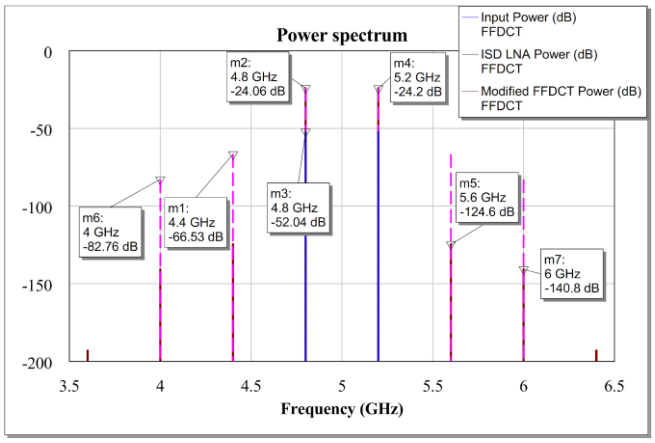

Figure 10: RF power spectrum at 5 GHz center frequency.

Table 3. Summary of the performance of the proposed cascode ISD LNA with and without the modified FFDCT and its comparison with previously published studies.

Ref.	[16]		[21]	[24]	[25]	[12]	This work	
	LNA	LNA with linearity	LNA with linearity	LNA with linearity	LNA with linearity	LNA with linearity	LNA	LNA with linearity
Technology (nm)	350		130	130	180	40	45	
Frequency (GHz)	0.9		3.1–10.6	0.6-3	0.32-1	1-11	5	
S21 (dB)	5	-	19.5	48-42	18-23.5	14-17	27.9	
S12 (dB)	-		-70.6	-	-	-	-65.8	-
S11 (dB)	-	-	<-5	<-8	10	<-10	-51.7	-
S22 (dB)	-	-	-10.9	-	-	-	-0.111	-
NF (dB)	2.6	2.8	1-3.9	3	2.2-2.7	3.5-5.5	0.025	0.554
Power Supply (v)	3		0.6	1.2	1.8	1.2	0.6	
Pdc (mW)	22.5	45	4.1	30	15.5	9	1.224	2.448
IIP3 (dBm)	5	18	4.56	-14	0	-2.6	-14.66	14.36

6. CONCLUSION AND PERSPECTIVES

This research focuses on optimizing cascode ISD LNA design using the Kapu optimizer, employing feed-forward linearization strategies to suppress IM3 distortion at 5GHz in 45nm technology. The results indicate that while the modified FFDCT increases power consumption, it substantially enhances the linearity of the LNA, making it suitable for applications that require high linearity and low noise at 5 GHz. The specifications indicate a low noise figure, low power consumption, high linearity, and significant gain, making it an excellent choice for high-performance wireless systems. The combination of these parameters ensures that the LNA can effectively amplify weak signals while maintaining low noise and high linearity, which is essential for applications such as 5G communication and radar systems. This research will prove extremely valuable for the advancement of future wireless communication systems, where achieving optimal performance and minimizing power consumption are of the greatest significance. Its improved linearity and low noise properties also make it suitable for use in radar systems, satellite communications, and other advanced RF applications.

The design could be extended to support higher frequency bands, such as millimeter-wave and terahertz, to meet the demands of 5G/6G and emerging wireless technologies. Scaling the circuit to deeper process nodes (e.g., 22 nm or 7 nm) could enhance performance, provided process variations are properly addressed. Additionally, integration with front-end modules like mixers and filters could enable fully integrated 5G receiver systems, while adaptive low-power techniques could improve energy efficiency without compromising performance. Experimental fabrication and testing would validate simulation results and provide deeper insights into the design's feasibility.

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