International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

A full range fully analytical drain current model of double gate junctionless field effect transistor with triangle shaped spacer

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Received 13 August 2024, Revised 09 October 2024, Accepted 12 October 2024

ABSTRACT

A full range and fully analytical model for the drain current of a symmetric double gate junctionless field effect transistor with a spacer of triangular shape is presented in the paper. The model is valid in the complete range of operation of the device, i.e., all four modes of operation namely- subthreshold, bulk current, flatband and accumulation modes. The approach to obtain the model is channel resistance based. The resistance of the channel of the device has been obtained from charge enclosed within it. The resistances of the model vary in different modes. Therefore, four expressions are obtained for four different modes of operation namely sub threshold, bulk current, flatband and accumulation. The model is said to be analytical in nature as each mode is represented by one single expression without the involvement of any numerical integration. Quantum confinement effect has also been considered in the model. The model has been validated with the help of simulation results from Technology Computer Aided Design (TCAD) device simulator. For the purpose of validation, the model is compared with simulation results as well as experimental results from existing literature. The average deviation from experimental results is 1.425% and the maximum deviation is 1.7%.

Keywords: *Drain current, JLFET, Triangle shaped, Spacer*

1. INTRODUCTION

The present world is dominated by solid-state devices, mostly Metal Oxide Semiconductor (MOS) based devices due to its low switching loss, high controllability and ultra-miniaturization capability. However, basic MOS structure is no longer in use in this Very Large Scale Integration (VLSI) era. A good number of advanced semiconductor devices entered the field of VLSI. Among many advanced MOS based technologies one of the promising technologies is Junctionless Field Effect Transistor (JLFET) [1-4]. Its on-off operation is controlled by the workfunction of the gate material. In an N-channel JLFET, if the workfunction of the gate is higher than the channel, a depletion region is created which may be extended throughout the thickness of the channel if the channel is thin. In this way the JLFET is turned off without the p-n junction. Application of a positive gate voltage will convert the depletion region into neutral semiconductor region to accomplish turn on of the device. JLFET shows many benefits over the other MOS based devices in terms of short channel effect. In fact, it has the lowest on-state loss as compared to any device with a p-n junction. Hence, this makes it suitable for power electronics applications [5]. However, it may suffer from higher off-state loss if the channel thickness is increased. Thicker channel is a need for power electronics applications to have sufficient drive current. Placing an insulator inside the channel [6] significantly reduces the off-state current. However, this technique may also reduce the on current. Another way to overcome this drawback and enhance the analog performance of the device is the use of high K spacers which can effectively reduce the off-state leakage current with the fringing field effect [7]. A spacer is a dielectric material placed over the source drain region adjacent to the gate. Generally, a high-K dielectric material is used for spacers. The purpose of placing a spacer is to create a fringing field. This extends the gate controlling region which helps in reducing the drain-induced barrier lowering (DIBL). This enhances off characteristics of the device reducing the leakage current. High-K material results in higher capacitive coupling between the gate and the channel resulting in higher controllability of the gate. For optimum reduction of off-state leakage current the spacer should extend up to the ohmic contact region. However, this may also cause a reduction in on current. Gate controllability reduces in the direction towards the edges of the source drain region as electric field reduces with distance. Therefore, to use the fringing field effect more effectively the shape of the spacer region is changed from rectangular to triangle [8]. In triangle shaped spacer the thickness of the spacer reduces towards source drain edges. With the lower thickness of the dielectric the gate capacitance increases thereby increasing gate controllability. Thus, this technique will compensate for the reduction in gate electric field with distance and maintain the gate controllability throughout the source drain region.

The most important parameter in the design of a device is the drain current of the device. Therefore, an analytical model for the drain current has been developed and

presented in this paper. Various drain current models of JLFET have been reported in [9-13]. The approach to obtain the model is channel resistance based. The drain current has been obtained from channel potential model and channel resistance. In this paper n-type JLFET is considered. The novelty of the paper lies on modelling of the drain current of the double gate (DG) JLFET with triangle shaped spacer as drain current for the structure is not yet developed.

2. MATHEMATICAL MODEL

Figure 1. shows the cross-sectional view of Double Gate JLFET with a triangular shaped spacer where, L_s and L_D are source and drain length and L is the gate length.

A JLFET has four modes of operation:

i. Sub threshold mode ($V_{gs} \leq V_{th}$)
ii. Bulk current mode ($V_{fb} \leq V_{gs} \leq V_{th}$)
iii. Flat band mode ($V_{gs} = V_{fb}$)
iv. Accumulation mode ($V_{gs} \geq V_{fb}$)

V_{gs} is the gate to source voltage, V_{th} is the threshold voltage and V_{fb} is the flatband voltage.

Figure 2 shows different modes of operation of a JLFET. In JLFET the work function of the gate material is selected such that its work function is higher than the body material. This difference in work function creates an internal gate electric field which creates a depletion layer under the gate. In the subthreshold mode the gate voltage (V_{gs}) is lower than the threshold voltage (V_{th}). In this condition, the internal gate electric field due to the work function difference is sufficiently higher than the applied gate electric field to keep the region underneath the gate fully depleted. This is the off-state (cut off) of the device.

As applied gate voltage (V_{gs}) passes the threshold voltage the applied electric field is higher than the internal electric field. The depletion layer underneath the gate starts converting into its original neutral semiconductor form and flow of drain current begins with applied drain voltage at this stage. This mode is called bulk current mode.

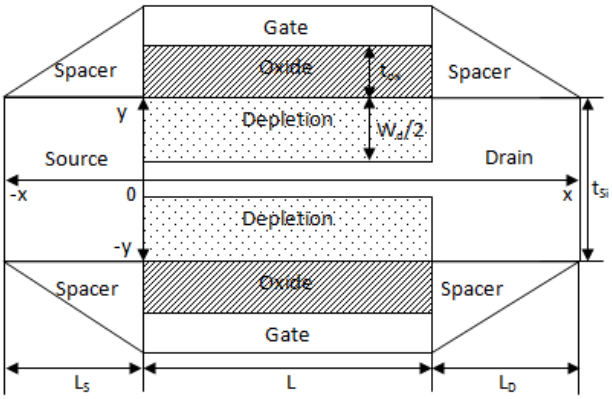

Figure 1. Schematic view of Double Gate JLFET with a triangular shaped spacer [8]

If the applied gate voltage is kept on increasing at one point, there will be no more depletion, and the complete body of the device is simply a layer of a neutral semiconductor. At this stage a large current flow through it as the whole body is conducting, which reduces the resistance of the body to a significantly low value. This point of operation of the device is called flatband mode. The device in this mode can be considered to be attained saturation.

Beyond flatband mode another mode may also present. In this mode the gate voltage exceeds the flatband voltage value and some additional charge carriers are accumulated near the surface which results in a further increase in drain current. This mode is called accumulation mode.

As the device has different layers in different modes, therefore the four modes have different channel resistances. In order to determine the drain current of the device the resistances of the modes need to be determined separately.

In the accumulation mode the channel consists of a neutral semiconductor layer at the centre and two accumulation layers are on the top and bottom of the neutral layer. Therefore, the resistance of the channel in accumulation mode is according to Equation (1):

$$R_1 = \left(\frac{(L+L_S+L_D)}{WW_{acc}}\rho_{acc}\right) \| \left(\frac{(L+L_S+L_D)}{(t_{Si}-W_{acc})W}\rho_{neutral}\right) \quad (1)$$

where resistivity in accumulation is given as Equation (2):

$$\rho_{acc} = \frac{1}{\mu_{eff}Q_{acc}} \quad (2)$$

For a JLFET charge in the accumulation layer will be as Equation (3) [14]:

$$Q_{acc} = \epsilon_{Si}\frac{\sqrt{2}}{L_D}\frac{kT}{q}\sqrt{exp\left(-\frac{q\phi_S(x)}{2kT}\right)-1} \quad (3)$$

The thickness of accumulation layer can be given as Equation (4) using Debye length, L_D as Equation (5) [14]:

$$W_{acc} = \sqrt{2}L_D\left[\frac{t_{Si}}{2\sqrt{2}L_D} + cos^{-1}\left\{exp\left(\frac{q\phi_S(x)}{2kT}\right)\right\}\right] \quad (4)$$

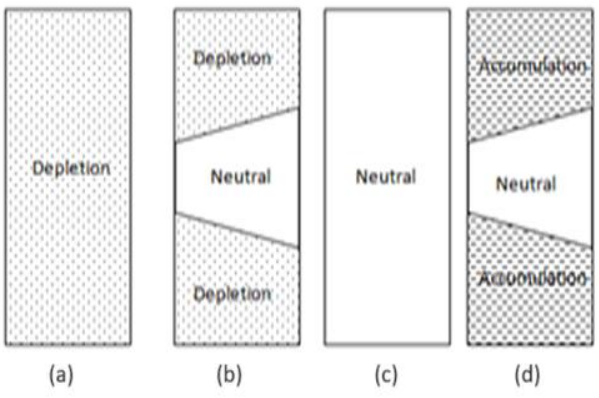

Figure 2. Different modes of operation of a Double gate JLFET (a) Subthreshold (b) Bulk current (c) Flat band (d) Accumulation

$$L_D = \sqrt{\frac{\epsilon_{Si} kT}{q^2 N_d}} \quad (5)$$

where, q is charge of a carrier, ϵ_{Si} is the permittivity of silicon, t_{Si} is the channel thickness, k is Boltzman's constant, T is temperature, N_d is donor doping concentration, and $\phi_S(x)$ is the surface potential which can be determined as follows.

The channel potential in a JLFET is given as Equation (6) [15-16]:

$$\phi(x,y) = \phi_0(x) + \frac{\epsilon_{ox}}{t_{Si}\epsilon_{Si}t_{ox1}}\left(V_{gs} - \phi_S\right)y^2 \quad (6)$$

where ϵ_{ox} is the permittivity of gate oxide and t_{ox1} is the effective gate oxide thickness which will be different in the three regions: source, drain and channel.

(i) In the source region, t_{ox1} is according to Equation (7) with Equation (8):

$$t_{ox1} = \frac{t_{ox}}{cos\theta(x)} \quad (7)$$

$$\theta(x) = tan^{-1}\left(\frac{x}{t_{ox}}\right) \quad (8)$$

where t_{ox} is the physical gate oxide thickness and $x = 0$ to $-L_S$.

(ii) In the drain region, t_{ox1} is according to Equation (7) with Equation (9):

$$\theta(x) = tan^{-1}\left(\frac{x-L}{t_{ox}}\right) \quad (9)$$

where $x = 0$ to L_d.

(iii) In the channel region, t_{ox1} is according to Equation (10):

$$t_{ox1} = t_{ox} \quad (10)$$

where $x = 0$ to L.

At y = $t_{Si}/2$, the potential is given as Equations (11):

$$\phi(x,y) = \phi_s(x) = \phi_0(x) + \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox1}}\left(V_{gs} - \phi_s(x)\right) \quad (11)$$

where $\phi_0(x)$ is based on Equation (12):

$$\phi_0(x) = \phi_s(x) - \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox1}}\left(V_{gs} - \phi_s(x)\right) \quad (12)$$

Therefore, Equation (11) can be written as Equation (13):

$$\phi(x,y) = \phi_s(x) - \frac{\epsilon_{ox}t_{Si}}{4\epsilon_{Si}t_{ox1}}\left(V_{gs} - \phi_s(x)\right) + \frac{\epsilon_{ox}}{t_{Si}\epsilon_{Si}t_{ox1}}\left(V_{gs} - \phi_s(x)\right)y^2 \quad (13)$$

Inserting $\phi(x,y)$ in Poisson's equation and considering y = $t_{Si}/2$ forms Equation (14):

$$\frac{d^2\phi_S(x)}{dx^2} + \frac{1}{\lambda^2}(V_{gs} - \phi_s(x)) = -\frac{qN_D}{\epsilon_{Si}} \quad (14)$$

where λ is according to Equation (15):

$$\lambda = \sqrt{\frac{t_{Si}\epsilon_{Si}t_{ox1}}{2\epsilon_{ox}}} \quad (15)$$

Solving Equation (14), the surface potential in the channel and source-drain region can be obtained as Equations (16) and (17), respectively [17]:

$$\phi_{Sch}(x) = \frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)}e^{\frac{x}{\lambda}} - \frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}\}e^{-2\frac{L_S}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}})e^{\frac{L_S}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)}e^{-\frac{x}{\lambda}} - C\lambda^2 \quad (16)$$

$$\phi_{Ssd}(x) = -\frac{qN_d}{2\epsilon_{Si}}x^2 + \left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)}\left(e^{\frac{L}{\lambda}} - 1\right) - \frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}\}e^{-2\frac{L_S}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}})e^{\frac{L_S}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)}\left(e^{-\frac{L}{\lambda}} - 1\right) + \frac{qN_d}{2\epsilon_{Si}}L^2\right]\frac{x}{L} + \frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)} - \frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_S}{\lambda}}}\}e^{-2\frac{L_S}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}})e^{\frac{L_S}{\lambda}}}{\left(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_S}{\lambda}}\right)} - C\lambda^2 \quad (17)$$

The effective mobility considering the velocity saturation effect can be written as Equation (18) [18]:

$$\mu_{eff} = \frac{\mu}{\left[1+\left(\frac{\mu V_{ds,eff}}{v_{sat}L}\right)^{\beta}\right]^{\frac{1}{\beta}}} \quad (18)$$

where N_d is the donor doping concentration, n_i is the intrinsic carrier concentration, $V_{ds,eff}$ is the effective drain to source voltage, v_{sat} is the saturation velocity of carriers, and L is the gate length.

In the flatband mode the whole body or channel is neutral semiconductor. Therefore, the channel resistance is given as Equation (19):

$$R_2 = \frac{(L+L_S+L_D)}{t_{Si}W}\rho_{neutral} \quad (19)$$

where the charge density of the neutral semiconductor region is given as Equation (20):

$$\rho_{neutral} = \frac{1}{en\mu_{eff}} \quad (20)$$

where the carrier density in the neutral semiconductor is given as Equation (21):

$$n = \frac{N_d}{2} + \sqrt{\frac{{N_d}^2}{4} + {n_i}^2} \quad (21)$$

In the bulk current mode, the center of the body is a neutral semiconductor layer with depletion layers on both sides as can be seen from Figure 2. Therefore, the resistance of the channel in this mode will be as Equation (22):

$$R_3 = \frac{(L+L_D+L_S)}{(t_{Si}-W_D)W}\rho_{neutral} \parallel \frac{(L+L_D+L_S)}{W_D W}\rho_{depletion} \quad (22)$$

where W_D is the depletion width.

The depletion width of N-channel double gate JLFET with triangle shaped spacer can be written in a similar way as for conventional double gate JLFET as Equation (23) [19],

$$W_d = t_{Si} - \sqrt{\frac{4t_{Si}\epsilon_{Si}t_{ox1}qN_d + \epsilon_{ox}{t_{Si}}^2 qN_d + 8\epsilon_{ox}\epsilon_{si}\left(\phi_{gs}-\phi_0(x)\right)}{\epsilon_{ox}qN_d}} \quad (23)$$

Considering quantum confinement effect, ϕ_{gs} is replaced with ϕ'_{gs}, as Equation (24):

$$\phi'_{gs} = \phi_{gs} - \Delta V_{th} \quad (24)$$

where, ΔV_{th} is the threshold voltage shift due to quantum effects given as in Equation (25) [20]:

$$V_{th} = \frac{kT}{q} ln \frac{\alpha Erf(\frac{t_{Si}}{2}\sqrt{\frac{q^2 N_d}{2\epsilon_{Si}kT}}}{\frac{4\pi kTN_d}{h^2\ N_c}[2m^*_{d,1}\sum_n e^{-E_{1,n}/kT} + 4m^*_{d,2}\sum_n e^{-E_{2,n}/kT}]} \quad (25)$$

In the subthreshold mode only depletion layer is present. Therefore, the resistance of the channel in the subthreshold mode is give as Equation (26):

$$R_4 = \frac{(L+L_S+L_D)}{t_{Si}W}\rho_{depletion} \quad (26)$$

where, $(L+L_s+L_d)$ is the total length of the body, W is the width, t_{Si} is the thickness and the resitivity of the channel $\rho_{depletion}$ is given as Equation (27):

$$\rho_{depletion} = \frac{1}{ep\mu_{eff}} \quad (27)$$

where, e is the charge of one carrier = 1.6×10^{-19} C, the carrier density of the depleted region for n-type semiconductor is given as Equation (28):

$$p = \frac{{n_i}^2}{\frac{N_d}{2} + \sqrt{\frac{{N_d}^2}{4} + {n_i}^2}} \quad (28)$$

The drain current expression can be written as Equation (29) [6]:

$$I_d = \frac{\phi(L+L_D) - \phi(-L_S)}{R} \quad (29)$$

where, R = R_1 for accumulation mode, R = R_2 for flatband mode, R = R_3 for bulk current mode, R = R_4 for super threshold mode, and Equation (30):

$$\phi(x) = \frac{V_{ds} + \frac{qN_d}{2\epsilon_{si}}\{(L+L_d)^2 - {L_s}^2\}}{(L+L_d+L_s)}L_s + \frac{qN_d}{2\epsilon_{si}}{L_s}^2 + \frac{V_{ds} + \frac{qN_d}{2\epsilon_{si}}\{(L+L_d)^2 - {L_s}^2\}}{(L+L_d+L_s)}x - \frac{qN_d}{2\epsilon_{si}}x^2 \quad (30)$$

3. RESULTS AND DISCUSSION

The validation of the model obtained above is done using TCAD device simulator by comparing the transfer and output characteristics of the device obtained from the mathematical expressions to those obtained from simulating the device on TCAD.

Figures 3 and 4 show the transfer characteristics and output characteristics for various gate dielectrics, SiO_2 (K = 3.9), Si_3N_4 (K = 6.9), HfO_2 (K = 22). With high K dielectric the gate capacitance is higher. Therefore, better controllability with reduced DIBL can be seen in the characteristics. However,

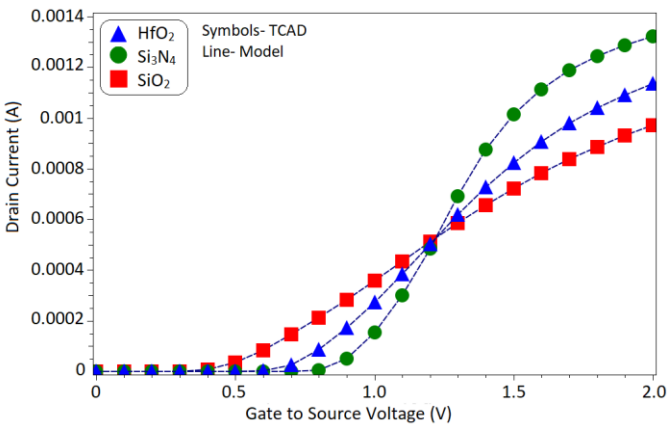

Figure 3. Transfer characteristics for various gate dielectrics: SiO_2 (K = 3.9), Si_3N_4 (K = 6.9), HfO_2 (K = 22)

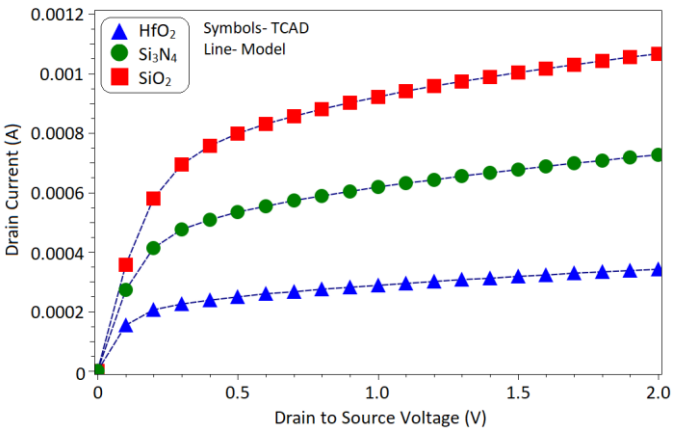

Figure 4. Output characteristics for various gate dielectrics: SiO_2 (K = 3.9), Si_3N_4 (K = 6.9), HfO_2 (K = 22)

higher K dielectric may cause the depletion layer to become stronger causing a reduction in on current.

Figures 5 and 6 show the transfer characteristics and output characteristics for different doping concentration- (N_d =10^{19}/cm^3, 5x10^{18}/cm^3, 10^{18}/cm^3). Higher doping concentration results in higher charge density. Therefore, the current both in on and off-state will be higher and threshold voltage will be lower for higher doping concentration.

Figures 7 and 8 show the transfer characteristics and output characteristics for various gate dielectric thickness, t_{ox} = 2 nm,3 nm,4 nm. With thinner gate dielectric, the gate capacitance is higher. Therefore, better controllability with reduced DIBL can be seen in the characteristics for thinner gate dielectric. However, thinner gate dielectric may cause the depletion layer to become stronger causing a reduction in on current.

Figures 9 and 10 show the transfer characteristics and output characteristics for various drain to source voltages, V_{ds} = 0.1 V, 0.2 V, 0.3 V and various gate to source voltages, V_{gs} = 0 V, 0.5 V, 1 V. With higher drain voltage DIBL is higher and as it is the biasing voltage current will also be higher. Lower gate voltage implies thicker depletion layer and reduced current as can be seen from the output characteristics.

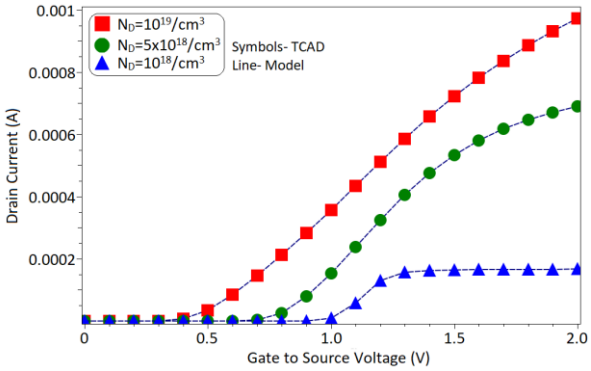

Figure 5. Transfer characteristics for different doping concentration (N_d = 10^{19}/cm^3, 5 × 10^{18}/cm^3, 10^{18}/cm^3)

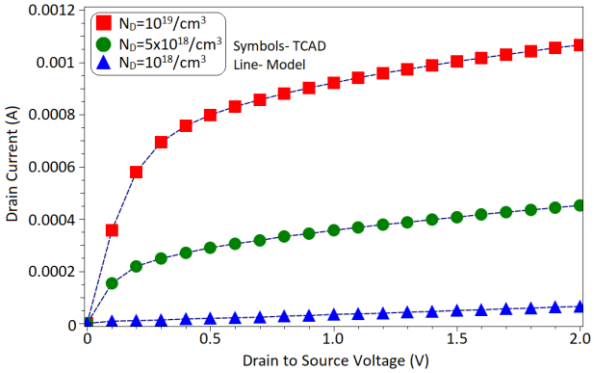

Figure 6. Output characteristics for different doping concentration (N_d = 10^{19}/cm^3, 5 × 10^{18}/cm^3, 10^{18}/cm^3)

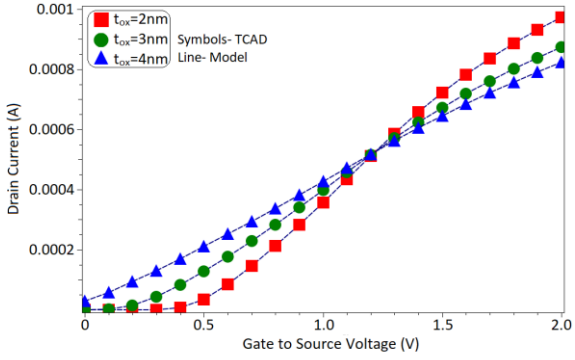

Figure 7. Transfer characteristics for various gate dielectric thickness, t_{ox} = 2 nm, 3 nm, 4 nm

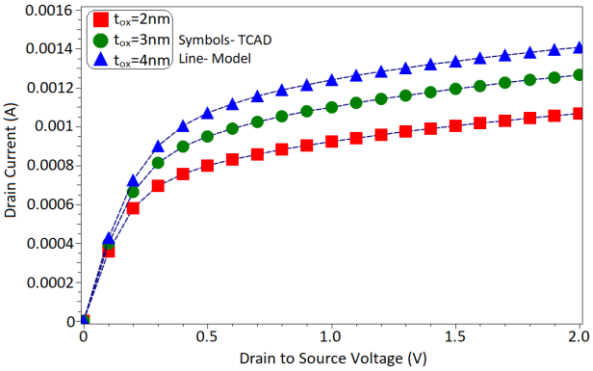

Figure 8. Output characteristics for various gate dielectric thickness, t_{ox} = 2 nm, 3 nm, 4 nm

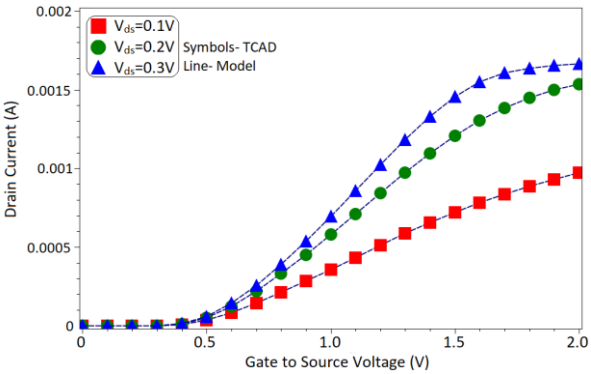

Figure 9. Transfer characteristics for various drain to source voltages, V_{ds} = 0.1 V, 0.2 V, 0.3 V

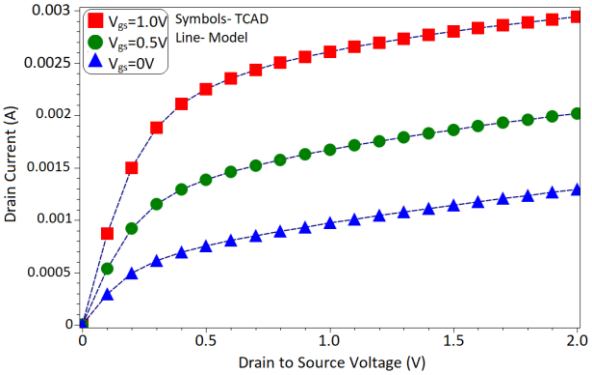

Figure 10. Output characteristics for various gate to source voltages, V_{gs} = 0 V, 0.5 V, 1 V

Figures 11 and 12 show the transfer characteristics and output characteristics for various gate work function, Ψ_M = 5.4 eV, 5.2 eV and 5.0 e. With high work function gate internal electric field responsible depleting the channel is higher. Therefore, higher channel resistance occurs if the work function of the gate is higher causing the current to reduce.

In all cases it can be seen that the plots obtained from the mathematical model and the TCAD are very close to each other. This ensures the validity of the model on simulation level.

Figure 13 shows the subthreshold slope variation with channel length of the device. Comparison of the results obtained from model and simulation has been done with experimental results extracted from existing literature [20]. The subthreshold slope reduces with increasing channel length due to reduced DIBL. The experimental results are close to the simulated and analytical model results. The closeness of the model with the experimental result validates the model. However, the experimental results available are for normal spacer based JLFET. Therefore, to compare with the experimental results the model presented here is modified to normal spacer based JLFET where, effective gate oxide thickness remains constant throughout the source drain lengths.

Figures 14, 15 and 16 show subthreshold swing variation with dielectric constant of spacer. As the dielectric constant

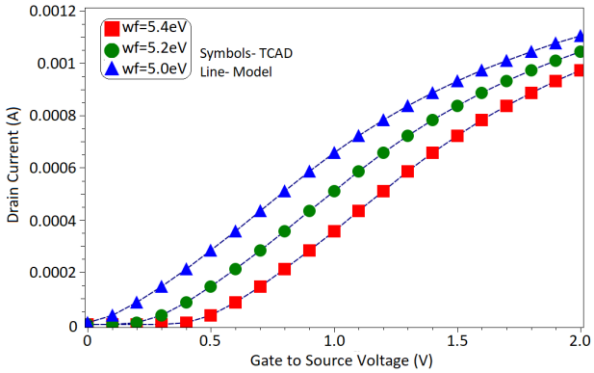

Figure 11. Transfer characteristics for various gate work function, Ψ_M = 5.4 eV, 5.2 eV and 5.0 eV

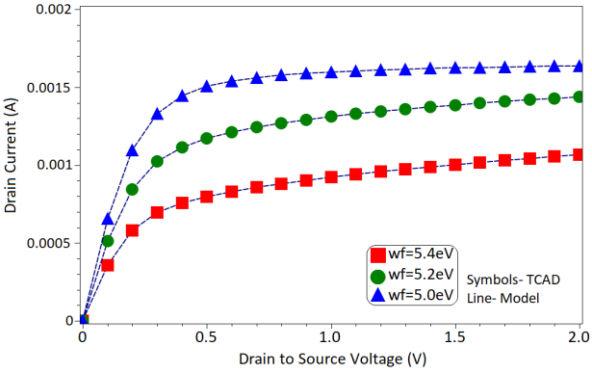

Figure 12. Output characteristics for various gate work function, Ψ_M = 5.4 eV, 5.2 eV and 5.0 eV

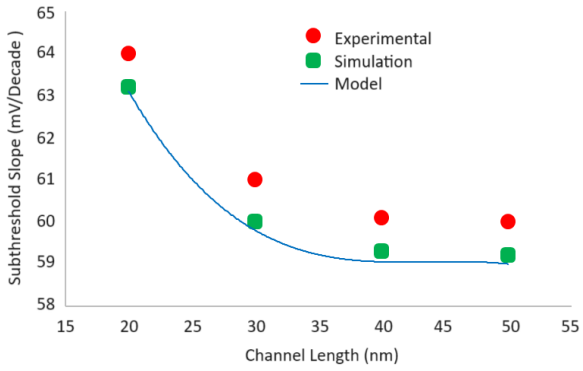

Figure 13. Subthreshold Slope Variation with Channel Length [21]

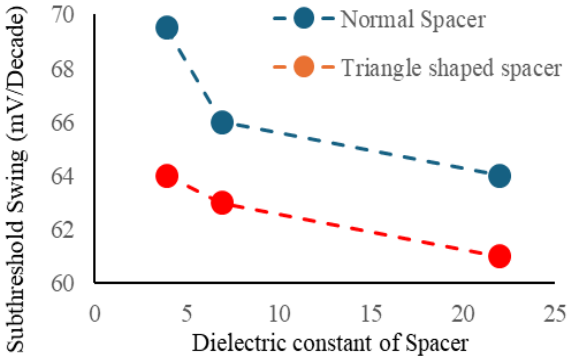

Figure 14. Subthreshold swing variation with dielectric constant of spacer for SiO_2 gate dielectric

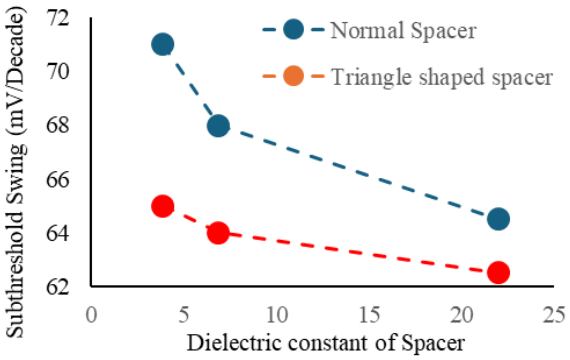

Figure 15. Subthreshold swing variation with dielectric constant of spacer for Si_3N_4 gate dielectric

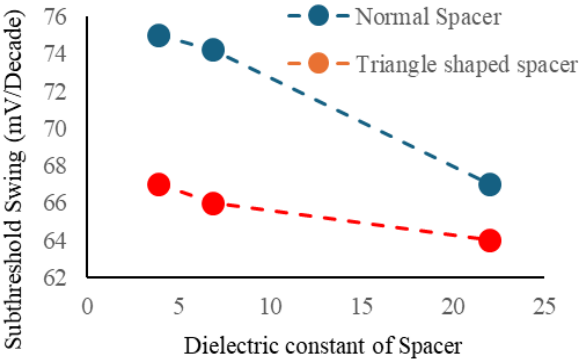

Figure 16. Subthreshold swing variation with dielectric constant of spacer for HfO_2 gate dielectric

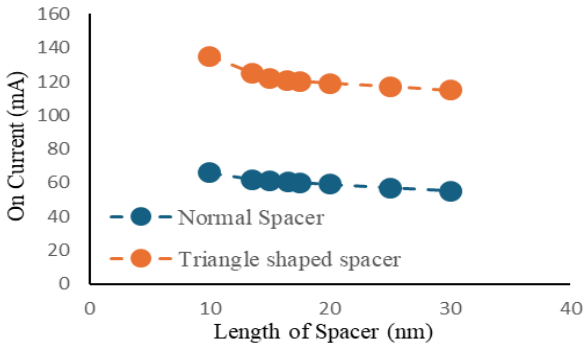

Figure 17. On Current variation with length of spacer

of spacer increases the subthreshold swing reduces due to increased fringing field and capacitive coupling. The subthreshold swing for the triangle shaped spacer structure is lower than a normal spacer structure. Figure 17 shows the on current variation with spacer length. Longer spacer implies higher channel resistance. The triangle shaped spacer JLFET has higher on current due to lower effective oxide thickness than normal spacer JLFET.

4. CONCLUSIONS

Mathematical model for drain current of a double gate JLFET with triangular shaped spacer is presented along with the validation at simulation level. Transfer characteristics and output characteristics of the device obtained from the model and TCAD simulator have been compared for various gate dielectrics, doping concentration, gate dielectric thickness, drain to source voltages, gate to source voltages and work function of the gate. Plots obtained from both sources closely match with each other which ensures the validity of the mathematical model at simulation level. The structure with triangle spaced spacer shows lower subthreshold swing and higher on current compared to a normal spacer-based device and device without spacer. Although the study shows that the DGJLFET with triangle shaped spacer has better electrical characteristics compared to without spacer or normal spacer, the fabrication of the device is quite complex.

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