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A 25 GHz Voltage-controlled oscillator (VCO) for automotive collision avoidance radar

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ABSTRACT

This paper presents the design and implementation of a 25 GHz voltage-controlled oscillator (VCO) tailored for automotive collision avoidance radar systems. The VCO, a crucial component of the synthesizer, is essential for generating variable frequencies. This study focuses on addressing the challenges of high-power consumption and phase noise, which are critical factors in the performance of radar systems. The simulations were conducted using LTspice to evaluate the VCO's performance in terms of phase noise and power consumption, utilizing 0.18 µm CMOS technology. The proposed VCO employs a modified current-reuse configuration to enhance power efficiency and incorporates resistive and inductive source degeneration techniques to minimize phase noise. The results demonstrate that the VCO achieves a tuning range of 25.34–25.94 GHz, with an impressive phase noise of -156.61 dBc/Hz at a 1 MHz offset and -157.43 dBc/Hz at a 10 MHz offset for the resistive degeneration configuration. The inductive degeneration configuration shows a phase noise of -156.562 dBc/Hz at a 1 MHz offset and -157.431 dBc/Hz at a 10 MHz offset. Additionally, the power consumption is measured at 207.4 mW for the resistive configuration and 208.39 mW for the inductive configuration. These findings indicate that the proposed VCO design meets the stringent requirements of low power consumption and low phase noise and provides a reliable solution for implementing efficient radar systems in automotive applications.

Keywords: *Voltage-controlled oscillator (VCO), Automotive radar, Phase noise, CMOS technology, Source degeneration*

1. INTRODUCTION

The International Energy Agency predicts a significant increase in electric vehicle sales by 2022, suggesting a potential shift from petrol to electric vehicles [1]. However, with this transition, safety measures become crucial as vehicle collisions may rise with the growing number of automobile users. The Advanced Driver Assistance System (ADAS) aims to mitigate collisions through various sensors, processors, and interfaces, enhancing driving safety by maintaining safe distances, providing intelligent speed assistance, cruise control, and controlling speeding [2], [3]. ADAS technologies integrate with a vehicle's command and management systems and address challenges associated with deploying these technologies in EVs. ADAS technologies provide drivers with enhanced situational awareness and vehicle control by incorporating various features such as adaptive cruise control, lane departure warning, and automatic emergency braking [2]. Integrating ADAS technologies, including radar, is expected to be crucial in enhancing vehicle safety and providing a more comfortable driving experience. These systems utilize contemporary technologies and algorithms to anticipate the vehicle's surroundings and provide advanced alerts to the driver or take action when necessary [4]. ADAS implementation in EVs begins with sensing the environment using cameras, radar, and LiDAR sensors [5]. These sensors provide real-time information about the vehicle's surroundings, enhancing safety and effectiveness. LiDAR sensors use laser light to measure distances and create detailed 3D maps, while radar sensors detect and analyze data to support decision-making and navigation [6]. Figure 1 shows the detection capabilities of radar, where the ego vehicle's radar detects the lead car, displaying the intensity of the radar's output as a dot on display. These radar systems enable advanced driver assistance features, such as adaptive cruise control, collision warning, and blind spot detection, essential for improving road safety [7], [8].

Central to the ADAS radar system is the VCO, which adjusts the output signal frequency based on the input voltage [10], [11]. Figure 2 shows a simplified radar system involving a VCO, a branch-line coupler, a mixer, and an antenna array. This VCO is essential for minimizing power dissipation and phase noise. Considerable research has been conducted on VCOs in automotive radar applications, focusing on their design, performance, and integration into complete radar systems [12]. However, designing a VCO that can meet the stringent requirements of low power consumption and low phase noise is a significant challenge, mainly when

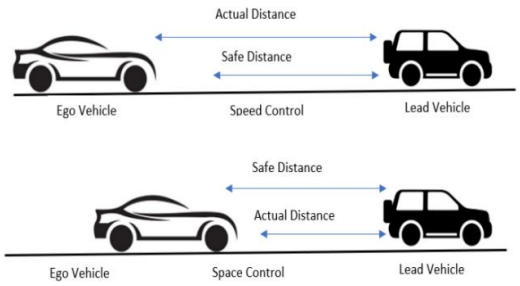

Figure 1. Adaptive cruise control system [9]

operating at high frequencies like 25 GHz [13]. Overcoming these design challenges is crucial for developing efficient and reliable radar systems that can be seamlessly integrated into modern automotive applications.

Previous research on low-power and low-phase noise VCOs provides a foundation for this study, showcasing the evolution of radar technology and the challenges in achieving low power consumption and high precision. Table 1 summarizes various VCO designs used in automotive radar applications, highlighting their technology, frequency range, tuning range, supply voltage (Vdd), phase noise, and power consumption.

Table 1 shows a comparative analysis of various VCO designs employed in automotive radar applications. The data highlights the trade-offs inherent in VCO design, balancing the pursuit of low phase noise and efficient power management across a range of technology nodes, from 65nm to 180nm. This table provides a valuable resource highlighting the design considerations and performance compromises engineers must navigate when developing VCOs for automotive radar applications. Therefore, this paper presents the design and implementation of a 25 GHz VCO that addresses the power consumption and phase noise limitations typically encountered in high-frequency radar systems. The proposed VCO employs a modified current-reuse configuration to enhance power efficiency, and it integrates both resistive and inductive source degeneration techniques to minimize phase noise.

2. METHODOLOGY

This section details the design procedure, component selection, and circuit topology for the VCO used in the radar system for electric vehicles (EVs). The VCO design is simulated using LTSpice. The simulation involves creating a circuit schematic and repeating it through various configurations to achieve the desired performance. The output waveforms and frequency responses are analyzed to meet the design criteria. Figure 3 shows the VCO circuit design reference from [13], and Figure 4 is the VCO circuit design using LTspice with 0.18 µm technology. This circuit is subjected to further analysis by changing the source degenerative and obtained waveform to verify differences between both circuits in power, phase noise, and voltage differential.

Table 1. Summary of VCO designs for automotive radar applications

Reference	[14]	[15]	[1]	[16]	[17]
Technology	65 nm	65 nm	28 nm	40 nm	180 nm
Frequency range (GHz)	19.3-24.8	24 & 77	77/79	1.55-1.67	4.68-5.36
Tuning range (%)	26.9	50	13.3	1	13.6
Vdd (V)	1.2	1.3	1.8	0.6	1.8
Phase noise @1MHz (dBc/Hz)	-90.4	-120/-108	-113.8	-118.6	-110.74
Power consumption (mW)	10.62	52/60	90	-	16.2

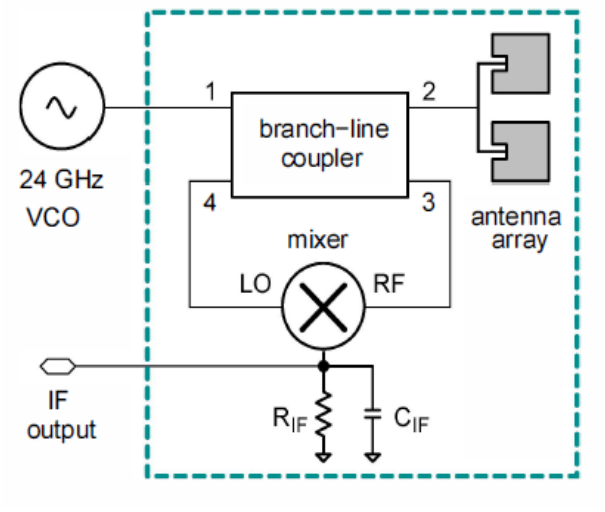

Figure 2. Block diagram of the radar front-end [18]

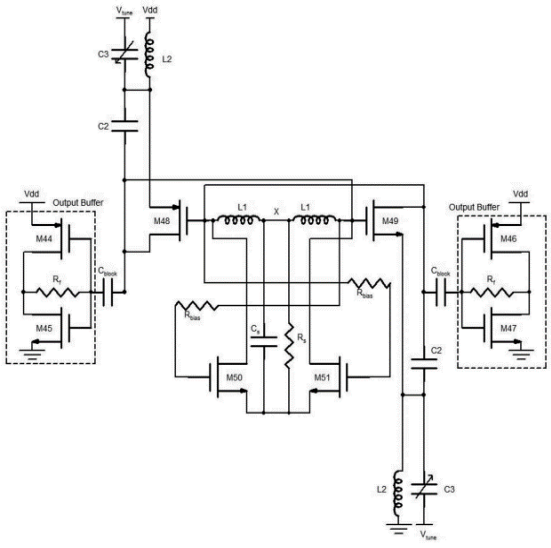

Figure 3. Proposed VCO design [13]

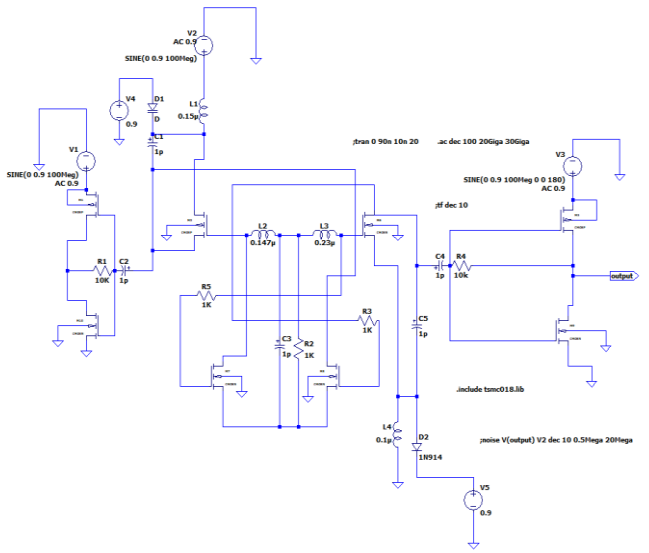

Figure 4. VCO circuit design using LTspice

Figure 4 shows that C3 blocks the DC current; it is necessary to parallel a resistor (R2) with this capacitor to provide the DC path required for biasing the N-type Metal-Oxide-Semiconductor (NMOS) transistors. The value of the biasing resistor must be several times larger than the impedance of C3 yet small enough to provide the necessary DC to achieve the required transconductance (gm). This is essential for compensating for the loss of the LC tank at frequencies where the negative resistance circuits effectively mitigate the loss of on-chip inductors. A capacitive feedback circuit with capacitors C1 and MOS varactor C2 is employed to enhance the amplitude range and frequency tuning of an LC VCO. This design eliminates the tail current source transistor and utilizes inductor L2 to reduce voltage headroom and phase noise. Differential mode operation with a virtual ground is achieved by biasing the N-type/P-type Metal-Oxide-Semiconductor (N/PMOS) cross-coupled transistors in the subthreshold region. This virtual ground connects to the capacitive source-degraded terminal of cascaded NMOS cross-coupled transistors, effectively compensating for on-chip inductor losses. Replacing tail current shaping transistors with an inductor source tuning method further reduces power consumption and phase noise. The capacitive feedback mechanism, leveraging on-chip inductors and capacitors, induces the drain and source voltage oscillation. At the same time, varactors in a parallel arrangement significantly adjust the tuning frequency with minimal voltage changes, thus improving phase noise performance in the VCO.

2.1. Phase Noise Reduction Modification

Two modifications to the VCO were explored and assessed to mitigate the phase noise performance. The first modification involved inductive source degeneration to enhance stability and decrease phase noise. The second modification incorporated resistive source degeneration to assess its effect on the same parameters. Each adjustment was applied separately to the VCO, and the resulting outputs were analyzed meticulously. The comparison of these

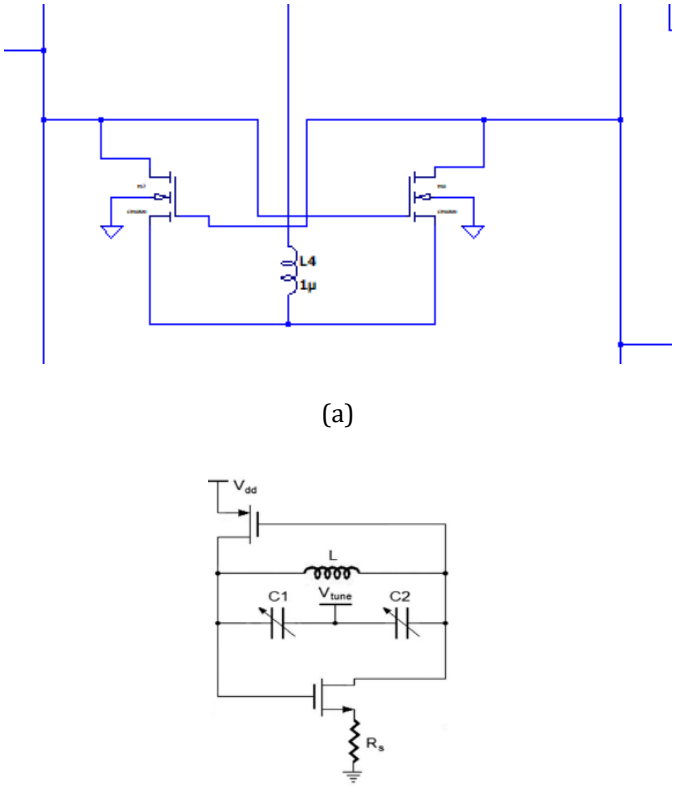

Figure 5. (a) Inductive source degeneration and (b) Resistive source degeneration

modifications focused on criteria such as stability and overall performance to determine the most effective configuration for minimizing phase noise in the proposed VCO design. This thorough evaluation ensures an informed decision on the optimal approach for phase noise reduction. Figure 5 illustrates (a) inductive source degeneration and (b) resistive source degeneration. While both circuits are similar, (a) uses an inductor in the cross-coupled transistors (PMOS/NMOS), and (b) uses a resistor and capacitor. The results from both revisions were carefully examined to identify the most appropriate configuration for minimizing phase noise.

Table 2 details the values of the key components in the VCO. The PMOS and NMOS transistors, each with a size of 0.18 µm, are critical for the VCO's functionality. The deliberate selection of these components ensures that the VCO meets the desired frequency generation and adjustability performance criteria, resulting in a well-balanced and efficient VCO configuration.

Table 2. Main components and values used in the proposed VCO

Element	Value
Transistor (PMOS, NMOS)	0.18 µm
L1	0.147 nH
L2	0.230 nH
Ls	0.136 nH
C1	1.00 pF
C2	0.48 pF-0.18 pF

3. RESULT

This section presents the simulation results of the proposed VCO circuit, simulated using LTspice with 0.18 µm technology. VCOs are crucial in frequency synthesizers due to their power and phase noise characteristics. Understanding and improving these parameters can significantly enhance signal integrity and spectral purity. The results discussed in this section are obtained through thorough experiments and theoretical analysis, providing valuable insights into the relationship between circuit design, operating conditions, and power/phase noise performance.

3.1. Phase Noise

Figures 6, 7, 8, and 9 showed the phase noise graph simulated in LTspice software under noise analysis. Two analyses were done by modifying the circuit into inductive and resistive base circuits. Phase noise is a critical parameter in VCOs, as it affects the stability and purity of the output signal. In this study, phase noise is measured in terms of dBc/Hz at offset frequencies of 1 MHz and 10 MHz. In LTSpice, noise is initially simulated in $nV/Hz^{1/2}$. To convert this to the more commonly used -dBc/Hz, the formula $20\log(nV/Hz^{1/2})$/input voltage is applied.

For the VCO with source degeneration, the phase noise at a 1 MHz offset is -156.61 dBc/Hz, and at a 10 MHz offset, it is -157.43 dBc/Hz. Conversely, for the VCO without source degeneration, the phase noise is -158.1 dBc/Hz at both 1 MHz and 10 MHz offsets. This comparison reveals that the implementation of source degeneration slightly degrades the phase noise at a 1 MHz offset but shows a minor improvement at a 10 MHz offset. Despite the slight degradation at 1 MHz, the source degeneration technique overall helps in achieving a more stable output signal with reduced noise at higher offsets.

The phase noise performance is a critical consideration for high-frequency applications, such as radar and communication systems, where signal integrity and spectral purity are paramount. The slight improvement in phase noise with source degeneration at higher offsets suggests that this technique can be beneficial in environments where high-frequency stability is essential. These results underscore the importance of optimizing circuit design to balance phase noise performance across different offset frequencies, ultimately enhancing the reliability and efficiency of the VCO in practical applications.

3.2. Power Consumption

Figures 10 and 11 display the power consumption graphs for the proposed VCO circuit under both resistive and inductive degeneration, simulated with a voltage input of 0.9V. The power consumption for the resistive degeneration circuit is 207.4 mV, while for the inductive degeneration circuit, it is 208.39 mV. Although these values indicate relatively high-power consumption, they are consistent with expectations given the design parameters. The primary factor influencing this power consumption is the transistor size used in the circuit. With a 0.18 µm technology, the transistor size significantly affects power usage, as smaller transistor sizes typically result in lower power consumption. Despite the higher power consumption, the proposed VCO demonstrates excellent phase noise performance. However, there is room for improvement in power efficiency, particularly when compared to modern nanometer-scale technologies.

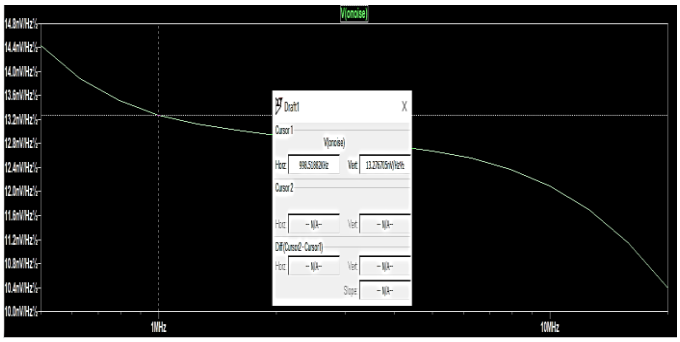

Figure 6. Phase noise of resistive degeneration @1MHz

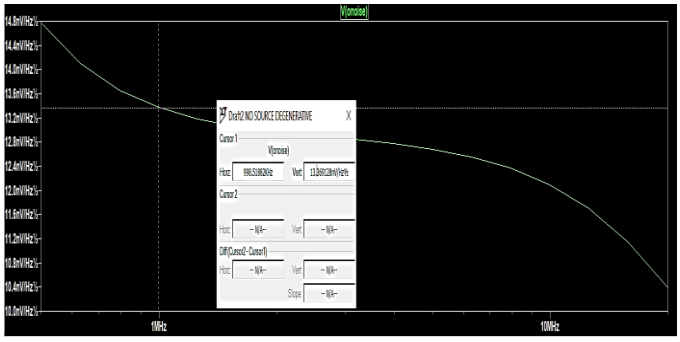

Figure 7. Phase noise of inductive degeneration @1MHz

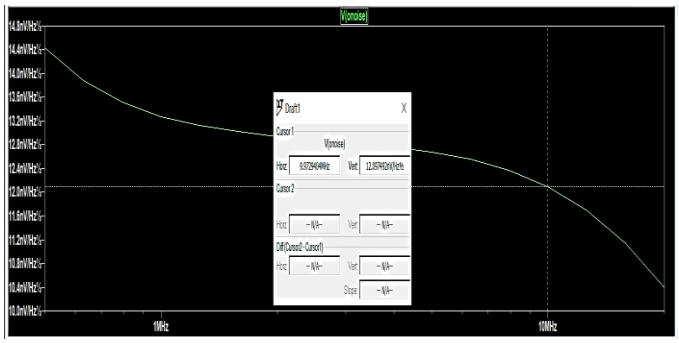

Figure 8. Phase noise of resistive degeneration @10MHz

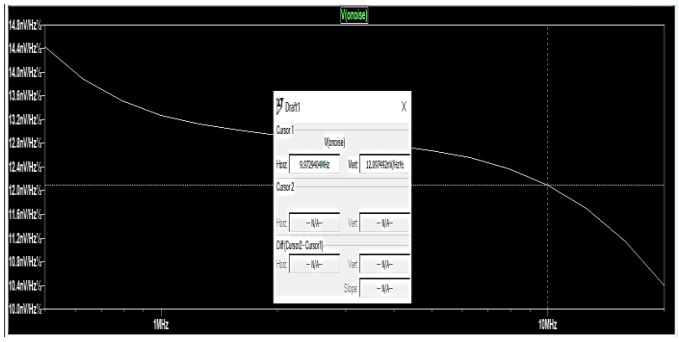

Figure 9. Phase noise of inductive degeneration @10MHz

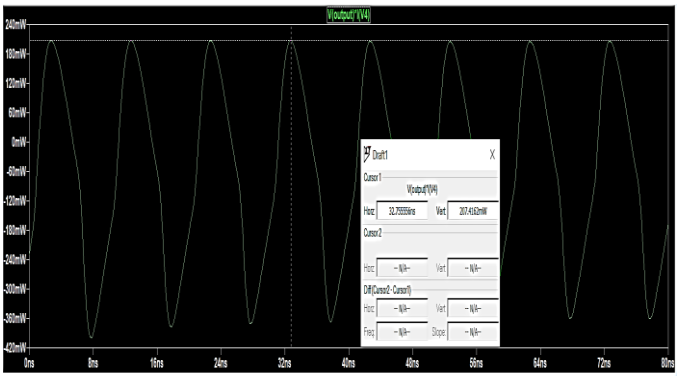

Figure 10. Power consumption resistive degeneration

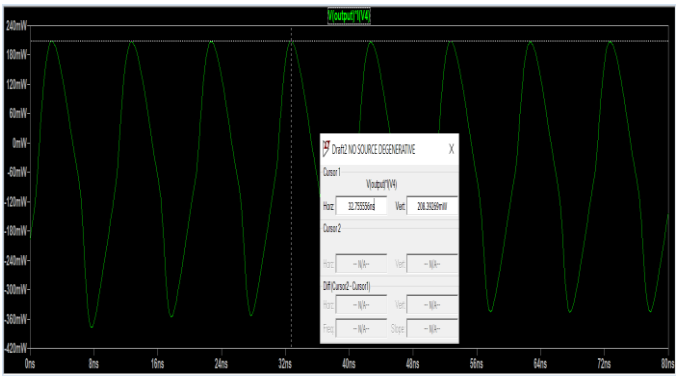

Figure 11. Power consumption inductive degeneration

The higher power consumption observed in inductor source degeneration VCOs compared to resistive degeneration VCOs can be attributed to several factors. Inductors generally exhibit lower quality factors (Q) compared to resistors, resulting in higher energy dissipation and the need for increased power to sustain oscillations. Additionally, parasitic losses, such as intrinsic resistances, contribute to the overall power consumption. Inductors also need to handle higher currents to produce equivalent voltage fluctuations as resistors, leading to greater power dissipation.

Furthermore, the biasing networks in inductive degeneration circuits often require higher bias currents to ensure optimal operation, thereby contributing to increased power consumption. These combined factors result in the higher power consumption observed in VCOs with inductor source degeneration. While the phase noise performance of the proposed VCO is commendable, future work could focus on optimizing the design to reduce power consumption, potentially through the use of smaller transistor sizes or alternative degeneration techniques.

3.3. Voltage and Frequency

Figures 12 and 13 compare the differential amplifier voltage in resistive and inductive source degeneration circuits, respectively. The larger differential voltage observed in the inductive source degeneration circuit can be primarily attributed to the distinct characteristics of inductors and resistors.

Inductors exhibit a reactance that increases with frequency ($X_L = 2\pi fL$), resulting in greater impedance at higher frequencies, which in turn leads to a larger voltage drop across the inductor. However, using inductors instead of resistors also comes with certain trade-offs. Inductive degeneration circuits may experience a slight increase in power consumption due to lower quality (Q) factors and parasitic losses. Additionally, inductors are typically larger and more complex to integrate into circuits, particularly in integrated circuit designs. These circuits may also be more sensitive to variations in inductance values, requiring more precise tuning compared to resistive designs. While inductive source degeneration offers the advantage of increased differential voltage, it also presents challenges related to power consumption, size, and design stability. The symmetrical output waveforms displayed in Figure 14 confirm the successful operation of the VCO in producing undistorted signals at 25 GHz.

This success is attributed to two key design techniques incorporated within the VCO. Firstly, the implementation of a current-reuse circuit optimizes power usage by efficiently recycling currents within the oscillator. This not only enhances overall efficiency but also ensures the generation of balanced output signals, which is crucial for maintaining signal integrity. Secondly, the integration of negative resistance techniques addresses losses and impedance inconsistencies within the circuit, thereby stabilizing frequency output. By countering these inherent challenges, the VCO reliably produces accurate signals at the desired frequency of 25 GHz.

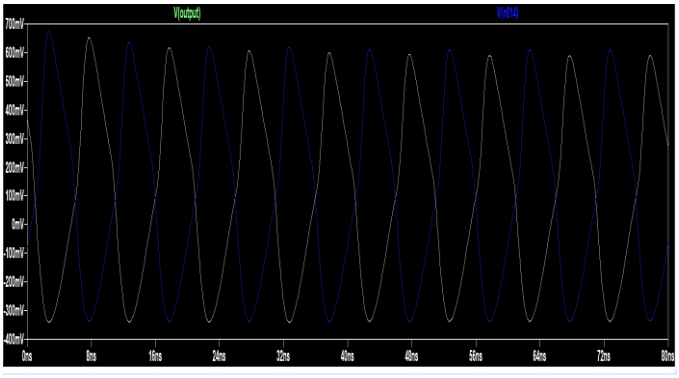

Figure 12. Differential amplifier voltage resistive degenerative

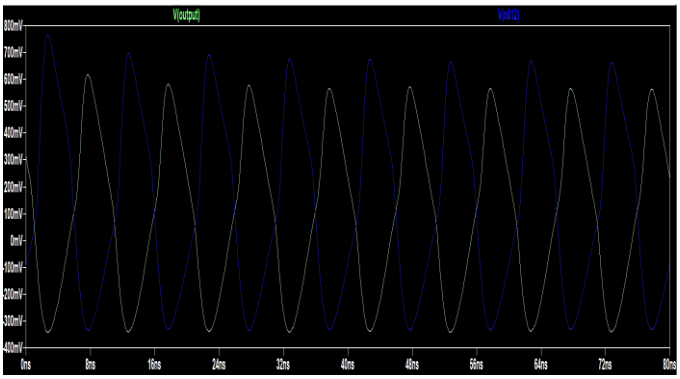

Figure 13. Differential amplifier voltage inductive degenerative

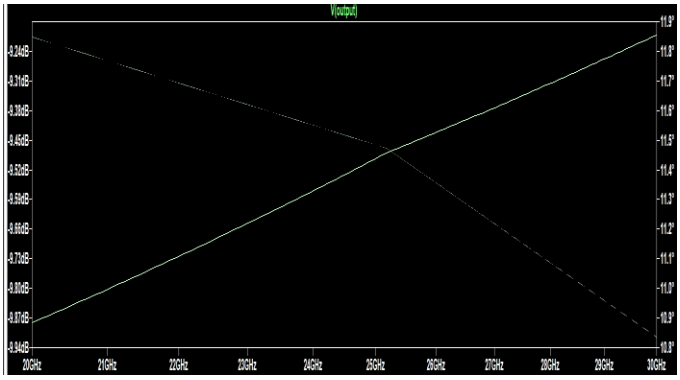

Figure 14. Frequency response

4. DISCUSSION

This section presents a comparative analysis of the proposed and reference VCO designs, focusing on key parameters such as power consumption, phase noise, frequency response, and transistor size. The study highlights significant differences between the two designs. It explores the trade-offs involved in optimizing VCO performance for automotive collision avoidance radar.

Table 3 highlights the differences between the proposed and reference results of a VCO circuit. Several critical parameters, such as power consumption, phase noise, frequency response, and transistor size, are compared, revealing significant differences between the two designs.

The proposed VCO design, utilizing 0.18 µm transistors, demonstrates enhanced phase noise performance, achieving 156 to 158 dBc/Hz compared to the reference design with 65 nm transistors, which achieves 104 to 128 dBc/Hz. This improvement is attributed to reduced flicker noise, enhanced linearity, and increased transconductance of the larger transistors. However, this enhancement comes with a trade-off in significantly higher power consumption, with the proposed design consuming 207 to 209 mW compared to the reference design's 3.4 mW. This is due to the higher gate capacitance and supply voltage requirements of the 0.18 µm transistors. Both designs exhibit comparable frequency responses, with the proposed design ranging from 24 to 25.8 GHz and the reference design ranging from 25.34 to 25.91 GHz. The trade-offs between transistor size, power consumption, and noise performance highlight the importance of selecting appropriate transistor sizes based on specific application needs and balancing noise performance with power efficiency.

Table 3. Comparison of the proposed and reference results

Parameter	This Work	Ref. [13]
Power Consumption (mW)	207-209	3.4
Phase Noise (dBc/Hz)	156-158	104-128
Frequency (GHz)	24.0-25.8	25.34-25.91
Transistor Size	65 nm	0.18 µm

5. CONCLUSION

This paper presents a detailed analysis and comparison of a 25 GHz VCO designed for automotive collision avoidance radar applications. The proposed VCO design, utilizing 0.18 µm transistors, demonstrates significant improvements in phase noise performance, achieving a range of 156-158 dBc/Hz compared to the 104-128 dBc/Hz observed in the reference design, which employs 65 nm transistors. This enhanced phase noise performance can be attributed to the larger transistor size, which reduces flicker noise, improves linearity, and increases transconductance, thereby enhancing signal amplification and minimizing noise.

However, the proposed design exhibits a higher power consumption, ranging from 207 to 209 mW, in contrast to the 3.4 mW recorded in the reference design. The increased power consumption is primarily due to the larger dimensions and higher gate capacitance of the 0.18 µm transistors, which require more charge for switching and operate at higher supply voltages. Despite this limitation, the proposed design maintains a comparable frequency response range of 24 to 25.8 GHz to the reference design's range of 25.34 to 25.91 GHz, demonstrating its suitability for high-frequency applications.

In conclusion, the proposed VCO design offers a compelling trade-off between phase noise performance and power consumption. While the larger 0.18 µm transistors enhance phase noise characteristics, they also lead to higher power consumption. The findings highlight the importance of selecting appropriate transistor sizes based on specific application requirements, balancing the need for low noise performance with power efficiency. This research contributes valuable insights into VCO design optimization for automotive radar systems, paving the way for further advancements in this critical technology.

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