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Design and simulation of gate and channel engineered dopingless tunnel FET

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ABSTRACT

This work presents an innovative device design of a dopingless tunnel field effect transistor (DL-TFET). The device presented in this work is a double gate that uses dual oxide, a dual gate material, and a silicon germanium (SiGe) channel to boost the performance of the proposed device. As such, the device is named a gate and channel engineered dopingless tunnel field effect transistor (GCE-DL-TFET). The use of a high-k material and a suitable work function at the gate and the SiGe channel has considerably enhanced the performance of the GCE-DL-TFET. A fair investigation of the GCE-DL-TFET device with the DL-TFET device reveals significant improvements in ON-current (I_{ON}), I_{ON}/I_{OFF} ratio, subthreshold slope (SS), and cut-off frequency (f_T). The proposed device shows the following increases: ~200 times in I_{ON}, 2.5 times in I_{ON}/I_{OFF}, and 20 times in f_T, as well as 70% improvement in SS. The transient analysis indicates the following decreases: 84% in transient-ON delay and 62% in transient-OFF delay in the GCE-DL-TFET-constructed inverting amplifier in contrast to the DL-TFET-based inverting amplifier.

Keywords: *Virtual doping, Gate and channel engineering, Tunneling, Dopingless, TFET, Subthreshold swing, Switching performance, MOSFET, SiGe.*

1. INTRODUCTION

A tunnel field effect transistor (TFET) is the most promising contender for the possible substitution of Complementary metal–oxide–semiconductor (CMOS) in an ultra-low-voltage application due to its steep subthreshold swing (SS) [1–4]. An MOS-based device and circuits have arrived at their cut-off points, and it is difficult to work with circuits beneath the 22/14-nm node. The primary issues that block scaling in CMOS-based devices and circuits below the 22-nm technology node are short-channel effects, OFF-state leakage (I_{OFF}), channel transport impediments, doping-related issues, and so on [5–6]. In addition, scaling of the MOS dimension requires a decrease in the biasing voltage (V_{DD}) to keep the electric field of the metal–oxide–semiconductor field-effect transistor (MOSFET) under control. The decrease in V_{DD} must be trailed by a reduction in the threshold voltage to have a high overdrive factor for improved execution of the MOS-based devices and circuits. However, a decrease in the threshold voltage intensifies the I_{OFF} and consequently the static power dissipation [7–10]. Reducing the SS of the MOSFET is one approach to decreasing the static power dissipation, but the SS of the MOSFET is not scalable [11–14]. Therefore, devices with a sharp SS can possibly scale the MOSFET further without any performance loss.

Various methods have been employed to reduce the supply voltage without performance degradation. However, the use of various steep SS devices has been mostly favored. These include TFET [15–26], impact ionization MOS (IMOS) [15], and negative-capacitance FET (NC-FET) [16]. Among them, TFET has the potential to replace the conventional bulk MOSFET. TFETs have a steep threshold slope, which results in very low I_{OFF} and better ON current (I_{ON})/I_{OFF} ratio. The other steep SS device structures have voltage scaling problems and reliability issues and need a stringent precise environment for robust operation. However, TFETs face a significant challenge due to their poor ON-state performance. The major performance issues associated with TFETs are larger tunneling width, insignificant tunneling variation, drop in the tunneling region [25], ambipolarity [27], statistical doping variations [25–27], and so on. It is quite reasonable for the I_{OFF} and thus the I_{ON}/I_{OFF} ratio in a TFET to worsen due to random dopant fluctuation (RDF) [28–30]. Furthermore, the crucial prerequisite of steep doping profiles for the tunnel mechanism in TFETs cannot be realized easily due to the fabrication complexity. The high temperature fabrication process and the dissemination of dopant atoms from source/drain (S/D) regions to channels can be among the gigantic obstructions [31].

In a recent work [26], a gate-engineered charge plasma-based TFET demonstrated substantial potential for reducing power consumption while maintaining high switching speeds. The study focused on gate architecture and material modifications, resulting in improved SS, increased ON-current, and reduced leakage current. These enhancements make the proposed structure more suitable for ultra-low-power applications.

2. Theoretical Background

In this study, we attempt to address the above-mentioned difficulties by presenting a novel device architecture with a sharp SS and a small I_{OFF} and is free from doping-related concerns. This innovative device is called a gate and channel engineered dopingless tunnel field effect transistor (GCE-DL-TFET). In the GCE-DL-TFET, the S/D regions are virtually doped by using the idea of the "charge plasma" [31–38]. It employs metals of altered workfunctions to induce a source (p+ doping), a drain (n+ doping), and a pocket of n+ type at the interface of source to channel in an undoped material. In the GCE-DL-TFET, the top and the bottom gates consist of a dual metal, so two gates appear: the upper, as well as the bottom, tunneling gate (TG) and main gates. Moreover, this dual oxide is used at the top and the bottom, and the channel consists of a silicon germanium (SiGe) material. Because of the use of these two dissimilar metals (the dual oxide and the SiGe channel), the device is referred to as a gate and channel engineered dopingless TFET. The TGs (in this case, TG1 and TG2) act as performance promoters for the GCE-DL-TFET.

The TGs act as virtually doped n+ type pockets, and the use of SiGe in the channel reduces the band gap; the two work together to increase the tunneling probability and thus improve the performance of the device by thinning the tunneling area. The improvement in the performance-measuring parameters of the GCE-DL-TFET device has been compared with the double-gate MOSFET (DG-MOSFET) and a dopingless TFET (DL-TFET) [31]. Noteworthy enhancements in the I_{ON} (more than 100 times), I_{ON}/I_{OFF} ratio (~3 times), and point SS (~55%) have been accomplished in the GCE-DL-TFET in comparison to the DL-TFET device. The cut-off frequency (f_T) of the GCE-DL-TFET (155 GHz) has also increased by ~20 times in comparison to that of the DL-TFET (~7.77 GHz). Moreover, the circuit feature of the Atlas device simulator has shown substantial progress in the switching behavior of the GCE-DL-TFET. Compared to an inverting circuit based on DL-TFET devices, the GCE-DL-TFET-based inverter circuit has achieved 84% and 62% development in switching-ON and switching-OFF delays, respectively.

The remainder of this paper is organized as follows: Section 3 describes our methodology, data collection, and analysis in depth. Section 4 discusses and analyzes the findings. Section 5 presents the paper's conclusions.

3. Methodology, Data Collection, and Analysis

The structures of the double-gate DL-TFET [31] and the recommended GCE-DL-TFET are presented in Figure 1. Intended for a rigorous comparative examination of the results, the same device considerations have been applied in the GCE-DL-TFET as those in the D-TFET [39] and the DL-TFET [31].

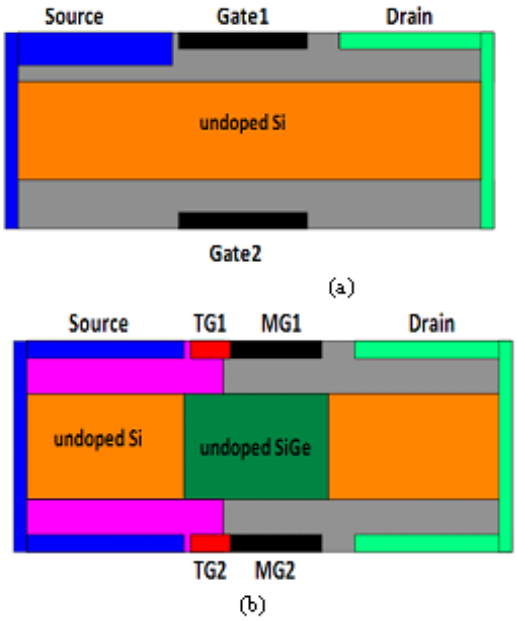


Figure 1. Device representations of (a) DL-TFET [31] and (b) the proposed GCE-DL-TFET

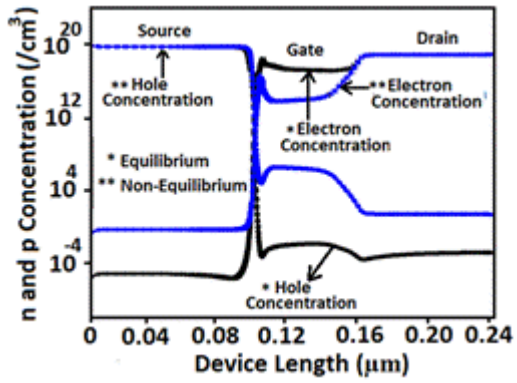
Table 1 provides the necessary information about the different structural parameters and dimensions of the devices under consideration.

Table 1. Structural parameters

Parameters	GCE-DL-TFET	DL-TFET	MOSFET
TSi (silicon)	10 nm	10 nm	10 nm
TOx (gate oxide)	2 nm	2 nm	2 nm
TOx1 (source oxide)	2 nm	0.5 nm	
MG1 workfunction	4.5 eV	4.5 eV	
MG2 workfunction	4.5 eV	4.5 eV	
TG1 workfunction	3.9 eV		
TG2 workfunction	3.9 eV		
Gate length	50 nm	50 nm	50 nm
Source workfunction	5.9 eV	5.9 eV	
Drain workfunction	3.9 eV	3.9 eV	
Dielectric	SiO2 + HfO2	SiO2	SiO2

4. Results and Discussion

The Atlas Silvaco device simulator has been used to study the behavior of the two devices presented in this work [40]. Several models, including drift diffusion, Shockley–Read–Hall (SRH), Fermi–Dirac, BBT.NONLOCAL, constant voltage and temperature (CVT), and so on, have been used in the simulations to capture the actual behavior of the device. The Lombardi CVT model captures the temperature-dependent, doping, and transverse field behavior of mobility. The SRH recombination model captures the recombination effects.



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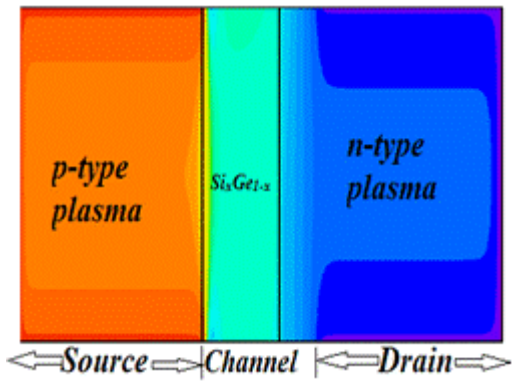
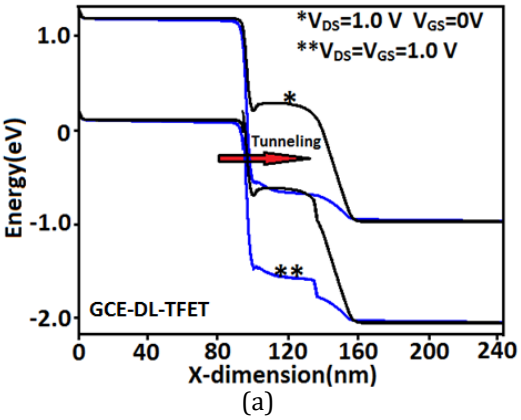


(b)

Figure 2. GCE-DL-TFE (a) Carrier concentration (VGS = VDS = 0V) and (VGS = VDS = 1V). (b) Proposed device profile under thermal equilibrium

The band-to-band tunneling (BTBT) model was invoked to observe the tunneling at the source channel junction by using the BBT.NONLOCAL model. We calibrated our model parameters with the experimental data, as stated in earlier and related works [26, 31, 39]. In model calibration, the device and its parameters were kept the same as those used in previous research [34, 39] to produce simulation results. The best possible settlement among the replicated results and the practical data was perceived [26]. Figure 2 shows the induced carrier concentration in the GCE-DL-TFET created by the virtual doping mechanism under different biasing conditions and the device profile under equilibrium conditions.

The performance improvement in the GCE-DL-TFET can be observed from the energy band plots of the devices under different biasing situations. Figure 3 shows the energy band plots of the GCE-DL-TFET and the conventional DL-TFET in the ON (V_{DS} = V_{GS} = 1V) and OFF (V_{DS} = 1V and V_{GS} = 0V) states. The band structure provides an insight into the thinning of the tunneling width in the GCE-DL-TFET in contrast to the DL-TFET, making the GCE-DL-TFET outperform the state of the tunneling devices. This enhancement can be credited to the high electron concentration due to the use of the TGs and the SiGe channel. Furthermore, using the low material workfunction and the high-k dielectric generates a high electric field, which accounts for the thinning of the tunneling width at the source–channel interface. The condensed tunneling width results in a noteworthy rise in the I_{ON} and the I_{ON}/I_{OFF} ratio of the proposed GCE-DL-TFET.



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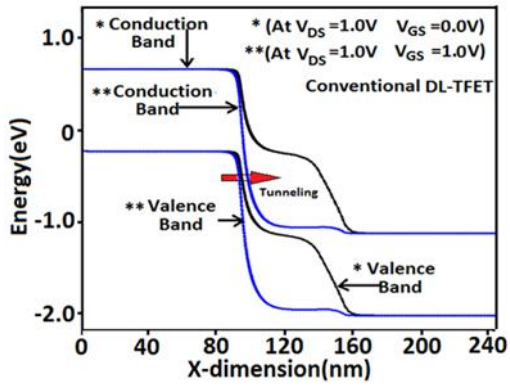


(b)

Figure 3. Energy band diagrams of (a) GCE-DL-TFET and (b) DL-TFET in the OFF state and in the ON state.

The ID VGS response of the DG-MOSFET with the matching threshold voltage (Vth) and the double-gate TFET devices are presented in Figure 4. The I_{OFF}, considered for V_{GS} = 0V and V_{DS} = 1.0V, is of the order of ~ 1 × 10^{-16} A/μm in the GCE-DL-TFET. The I_{ON}, considered for V_{GS} = 1V and V_{DS} = 1.0V, is of the order of ~ 1.5 × 10^{-4} A/μm in the GCE-DL-TFET. The I_{ON} and the I_{ON}/I_{OFF} ratio in the proposed GCE-DL-TFET have improved by ~200 times and ~2.5 times, respectively, compared with those in the conventional device (I_{ON} = 8 × 10^{-7} A/μm, I_{OFF} = 1×10^{-17} A/μm).

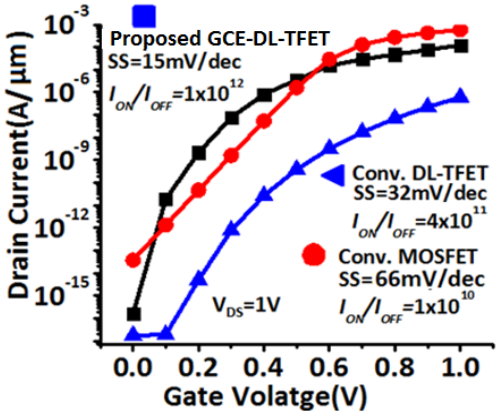


Figure 4. Transfer characteristics of MOSFET, DL-TFET, and GCE-DL-TFET

The GCE-DL-TFET device evidently has greater potential than those of the other devices, with a noteworthy enhancement in SS, ON current, and switching. As illustrated in Figure 4, the supply voltage (V_{DD}) of the GCE-DL-TFET can be reduced without deteriorating its performance compared with that of the device presented in a previous study [31] and that of the conventional DG-MOSFET. The scaling of V_{DD} is possible due to the steep SS of 15 mV/dec in the GCE-DL-TFET in comparison to those of the conventional TFET and MOSFET, with 32 mV/dec and 66 mV/dec, respectively. It is obvious from Figure 4 that the GCE-DL-TFET shows noteworthy enhancements in SS and leakage current in contrast to that of the DG-MOSFET although the latter possesses a larger driving capability than those of the DL-TFET and the GCE-DL-TFET device. To improve I_{ON} in the TFET-based devices, various techniques have been employed [25, 27, 41]; one is the use of the SiGe [9, 42] material to boost the performance of the said devices. The SiGe has been used in the channel of the proposed GEC-DL-TFET device to enhance the latter's performance. As presented in Figure 5, an increase in the germanium content of the SiGe has a huge influence on the performance of the GCE-DL-TFET.

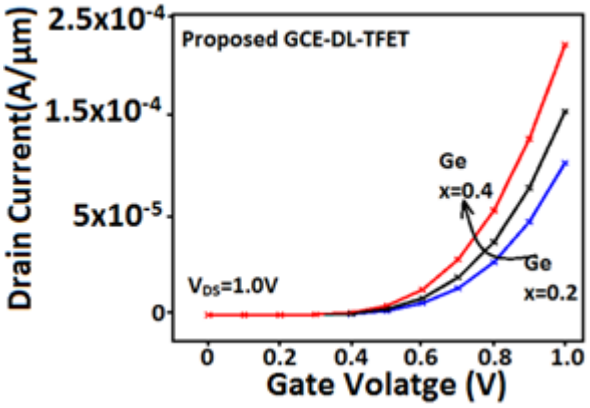
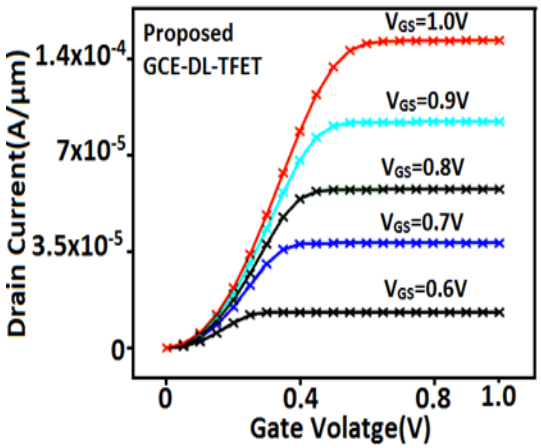


Figure 5. Effect of germanium content on the performance of the proposed GCE-DL-TFET device

This improvement can be attributed to the reduction of the band gap of the channel, which enhances the tunneling and thus improves the performance of the GCE-DL-TFET. Figure 6 shows the output characteristics of the proposed GCE-DL-TFET and the conventional DG-MOSFET device.



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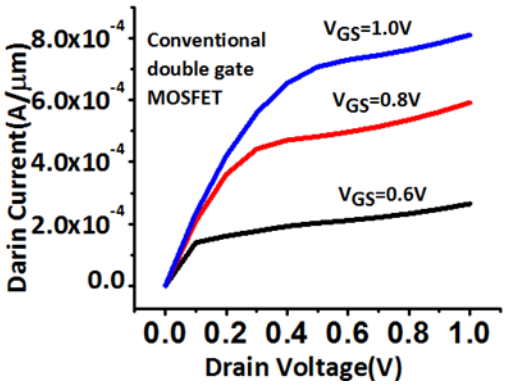


(b)

Figure 6. Output characteristics of (a) the proposed GCE-DL-TFET and (b) the conventional double-gate MOSFET

In the saturation mode, the I_{DS} is almost independent of the V_{DS} in the GCE-DL-TFET in comparison to the conventional DG-MOSFET, due to the smaller amount dependency of the tunneling width on the V_{DS}, at a higher V_{DS}. However, in the case of the DG-MOSFET, the saturation region shows the dependence on V_{DS}, which results in its lower output resistance than that of the TFET-based device.

The plot of transconductance (g_m) as a function of V_{GS} is shown in Figure 7. It is obvious that a considerable enhancement in the g_m is obtained in the GCE-DL-TFET. The higher g_m is accredited to the efficient modulation by the tunneling gates (TGs) and the SiGe channel that results in the thin tunneling width and the reduced band gap of the channel. Figure 8 displays the plot of transconductance-to-drive current ratio (g_m/I_{DS}) of the proposed device and of the conventional MOSFET.

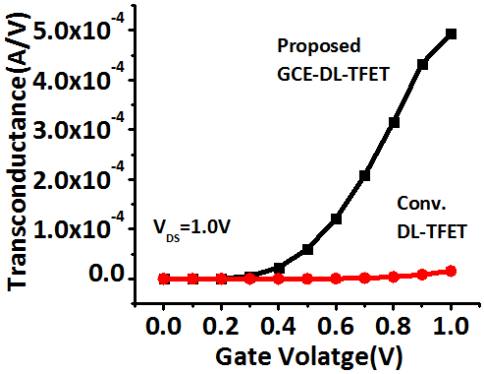


Figure 7. Transconductance assessment of the GCE-DL-TFET and DL-TFET

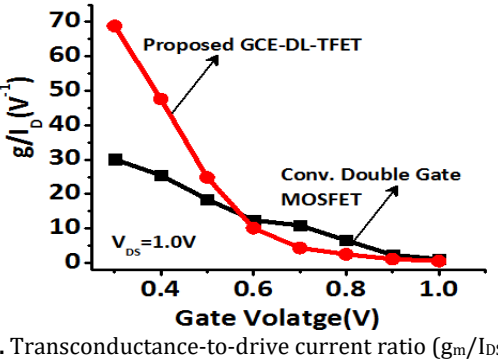


Figure 8. Transconductance-to-drive current ratio (g_m/I_{DS}) of (a) the proposed GCE-DL-TFET and (b) the conventional double-gate MOSFET

It is clear from the plot that the proposed device has a large g_m/I_{DS} ratio in contrast to that of the DL-TFET for all values of the gate voltage. This can be credited to the high drive in the case of the GCE-DL-TFET.

The noteworthy rise in the g_m has led to a substantial intensification in the cutoff frequency of the GCE-DL-TFET. It can be well understood from Figure 9 that the cutoff frequency of the GCE-DL-TFET (~155G Hz) is 20 times higher than that of the conventional device (~7 GHz). The cutoff frequency has been calculated by using Equation 1.

$$f_T = \frac{g_m}{2 * \pi (c_{gd} + c_{gs})} \quad \ldots\ldots\ldots\ldots\ldots\ldots 1$$

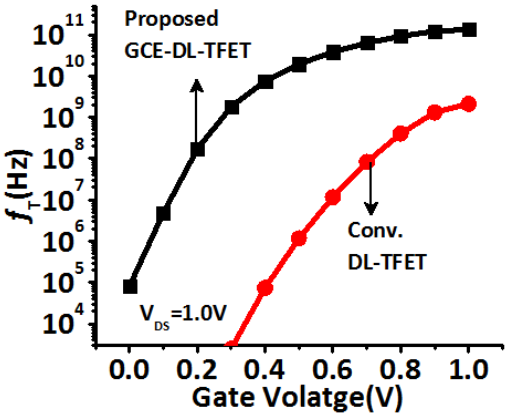


Figure 9. Cutoff frequency (f_T) evaluation of the GCE-DL-TFET and DL-TFET

The lower static power observed in the GCE-DL-TFET at all gate lengths in comparison to that of the conventional MOSFET (Figure 10) can be due to the lower off-current in the GCE-DL-TFET.

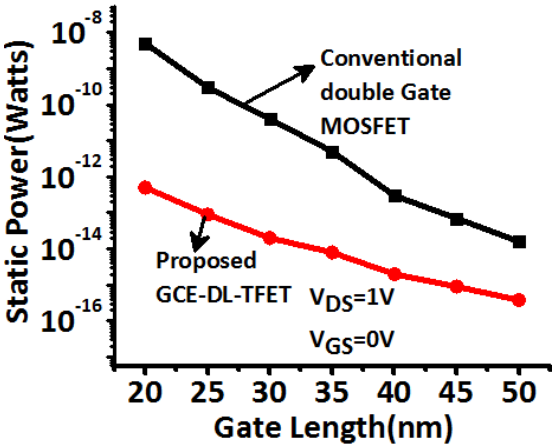
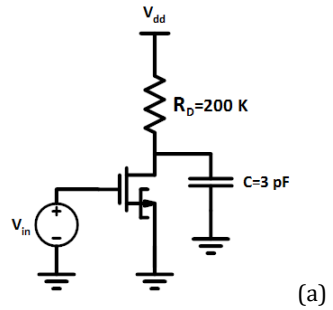


Figure 10. Variation of static power dissipation at various gate lengths

By designing the inverter, the devices were examined at the circuit level. Figure 11 shows the transient response of the resistive inverter based on the DL-TFET and the GCE-DL-TFET circuit. The inverter circuit based on the GCE-DL-TFET has lower OFF and ON delays than those of the one designed using DL-TFET. With the GCE-DL-TFET- based inverter, the computed percentage change in the ON latency is 84%, as compared to DL-TFET based inverter. In a similar vein, the inverter's OFF delay is observed to have a 62% decrease based on the GCE-DL-TFET inverter. By lowering the circuit's average delay, this reduction in both ON and OFF delays speeds up the design of the GCE-DL-TFET circuit.



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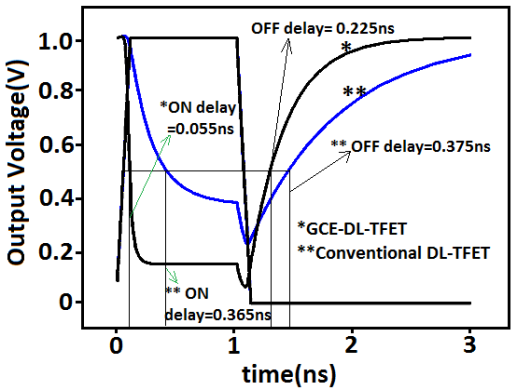

(b)

Figure 11. (a) TFET inverter circuit and (b) transient study of GCE-DL-TFET and DL-TFET

5. Conclusion

The design and replication of a novel dopingless TFET have been undertaken in this work. The GCE-DL-TFET is a double-gate device that uses virtual doping to realize different regions. Both gates consist of a dual metal; as such, two gates (the TG and the main gate) appear at the top and at the bottom of the GCE-DL-TFET. Furthermore, a high-k material has been used under the TG and the channel consisting of the SiGe material. Due to the use of two dissimilar metals (dual oxide and the SiGe channel material), the device has been named a gate and channel engineered dopingless tunnel field effect transistor (GCE-DL-TFET. A comparative investigation of the GCE-DL-TFET and the DL-TFET [31] has shown a noteworthy enhancement in I_{ON}, I_{ON}/I_{OFF} ratio, SS, and circuit switching performance. A steep SS is accomplished in the GCE-DL-TFET, with the result that the device can be scaled along with V_{DD} without performance deprivation. The GCE-DL-TFET is also virtually doped; therefore, high-temperature fabrication procedures are not required. Besides, RDF is not present in the GCE-DL-TFET as it is a dopingless FET.

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