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An enhanced buck-boost converter performance using a snubber circuit and advanced semiconductor devices

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ABSTRACT

Conventional buck-boost converter designs often suffer from efficiency losses and performance degradation due to switching transients and voltage spikes. To address these challenges, we propose the incorporation of a snubber circuit, which is designed to absorb and mitigate these detrimental effects. The study involves the design, implementation, and experimental evaluation of the proposed enhanced buck-boost converter. The analysis focuses on the impact of the snubber circuit on key performance metrics, including efficiency, thermal behavior, and electromagnetic interference (EMI) reduction. The experimental results indicate that the snubber circuit significantly reduces voltage spikes and switching losses, leading to improved converter efficiency and reliability. These findings provide valuable insights for optimizing converter designs in a variety of applications, from renewable energy systems to portable electronic devices, ultimately contributing to the advancement of power electronics technology. Finally, the performance of the proposed converter is analyzed using advanced semiconductor devices.

Keywords: *Buck-boost converter, Performance evaluation, Silicon carbide (SiC), Gallium nitride (GaN), Junctionless field effect transistors (JLFET)*

1. INTRODUCTION

In the realm of power electronics, buck-boost converter plays a crucial role in applications requiring a stable output voltage that can be either higher or lower than the input voltage. This versatility makes it an indispensable component in numerous modern electronic devices and systems, ranging from battery-powered gadgets to renewable energy applications. However, despite its widespread use, the buck-boost converter poses challenges, particularly concerning efficiency and performance under varying load conditions. One significant issue in conventional buck-boost converters is the occurrence of switching transients and associated voltage spikes, which can lead to increased EMI, reduced efficiency, and potential damage to the components. These problems necessitate the exploration of innovative solutions to enhance the performance and reliability of the converter. The operation of buck-boost converters is comprehensively covered in [1,2], which provides a detailed understanding of converter topologies and their applications. Similarly, [3,4] offers extensive insights into the devices, circuits, and applications of power electronics, highlighting the versatility and importance of buck-boost converters in modern electronics. A bidirectional DC-DC converter topology [5] is suitable for low-power applications, showcasing the flexibility of buck-boost converters in both step-up and step-down operations. Furthermore, [8] designed and analyzed a buck-boost converter to achieve high efficiency and low voltage gain, demonstrating the practical implications of the buck-boost topology in enhancing converter performance. Similarly [9] introduced a new buck-boost converter structure with improved efficiency, emphasizing recent advancements in converter design and [6,12] explored the design and simulation of DC-DC converters for PV applications, highlighting the role of buck-boost converters in optimizing power output from solar panels. Furthermore, [13] investigated the use of buck-boost converters for maximum power point tracking (MPPT) in PV systems, using the perturb and observe method to enhance energy harvesting efficiency. A bidirectional DC-DC buck-boost converter for battery energy storage systems and PV panels is presented in [11], focusing on improving energy conversion efficiency through innovative circuit design. References [7, 10] further delved into the design of bidirectional converters, emphasizing their applicability in solar PV systems for battery charging and overall energy management. The design and analysis of snubber circuits have been extensively studied in [14] for improving the performance of DC-DC converters focusing on designing snubber circuits to manage high-power applications, reducing switching stresses and improving the reliability of converters. The work in [15] reviewed advancements in dielectric technology for SiC and GaN power devices, emphasizing their superior electrical properties for high-efficiency applications. Additionally, [16] demonstrated the use of a GaN-based DC-DC converter for hybrid UAVs, confirming GaN's superior performance in reducing weight and size while increasing efficiency in high-frequency applications.

This study investigates the implementation of a snubber circuit as a means to mitigate the adverse effects of switching transients in buck-boost converters and its analysis with advanced semiconductor devices. Snubber circuits are well-regarded for their ability to absorb excess energy during the switching process, thereby reducing voltage spikes and improving overall converter performance. By integrating a snubber circuit, we aim to demonstrate substantial improvements in the efficiency, thermal performance, and longevity of the converter components. Through a comprehensive analysis and experimental validation, this paper presents the design, implementation, and performance evaluation of an enhanced buck-boost converter with an integrated snubber circuit. The results reveal significant enhancements in converter operation, making it a more viable solution for applications demanding high reliability and efficiency. This research contributes to the ongoing development of power electronics, providing insights and practical solutions for optimizing converter performance in various technological fields.

2. DESIGN OVERVIEW

A buck-boost converter is a versatile DC-DC converter that can output a voltage either higher or lower than the input voltage. Incorporating a snubber circuit in parallel to the inductor of a conventional buck-boost converter, as shown in Figure 1, can further enhance its performance by mitigating switching transients and reducing EMI. The input source voltage V_S supplies the necessary DC input voltage. An inductor, L stores energy when the switching element is on and releases this energy when the switch is off. The MOSFET controls the switching of the circuit, thereby managing the energy flow. A diode, D provides a crucial path for the inductor current when the switch is off, ensuring continuous current flow. The output capacitor, C smoothens output voltage, minimizing ripple and ensuring a stable voltage supply, the load, R represents the system that the converter powers. Additionally, a snubber circuit composed of a resistor, R_S and a capacitor, C_S is placed in parallel to the inductor. This snubber circuit absorbs and dissipates excess energy during switching, protecting the circuit components and improving performance. The operation of the buck-boost converter can be divided into two main phases: when the switch is ON, as shown in Figure 2. and when the switch is OFF, as shown in Figure 3. The presence of a snubber circuit affects both phases by providing a path for transient energy and smoothing voltage spikes.

The switch is ON:

- The MOSFET conducts, creating a closed path from the input voltage source V_S through the inductor to the ground.
- The inductor stores energy from the input source, and the current through the inductor increases linearly.
- The snubber capacitor in parallel with the inductor absorbs any initial voltage spikes caused by rapid switching.

The switch is OFF:

- The MOSFET stops conducting, opening the path from the input source.

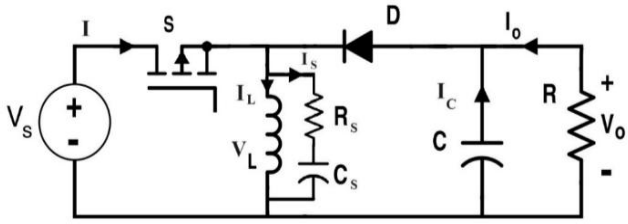

Figure 1. A proposed buck-boost circuit

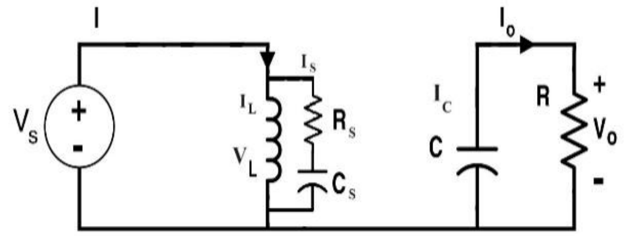

Figure 2. Proposed buck-boost converter ON mode

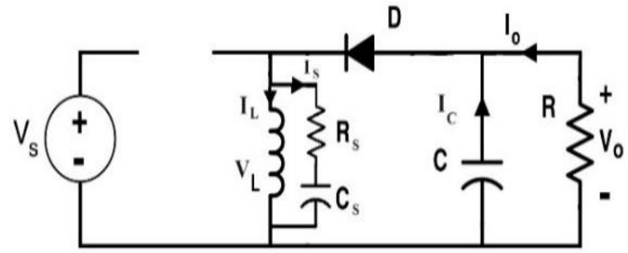

Figure 3. Proposed buck-boost converter OFF mode

- The inductor, which has stored energy, now releases this energy.
- The stored energy in the inductor creates a current that flows through the diode to the output capacitor and the load.

The snubber capacitor, positioned in parallel to the inductor, offers a pathway for excess energy and voltage spikes, effectively managing these transients. The resistor, R within the snubber circuit dissipates the energy absorbed by the capacitor, thereby reducing the overall voltage spike and safeguarding the circuit components. This mechanism significantly decreases the rate of change of voltage $\frac{dv}{dt}$ across the inductor, which in turn minimizes EMI and enhances the stability of the converter.

3. MATHEMATICAL MODELLING OF PROPOSED CONVERTER

In this section, we derive the equations governing the operation of the buck-boost converter with the parallel snubber circuit during the on and off states. The components involved include an inductor (L), a switch (S), a diode (D), an output capacitor (C), a snubber capacitor (C_S), and a snubber resistor (R_S).

3.1. ON State (Switch S Closed)

When the switch “S” is closed, inductor L is directly connected to the input voltage, V_S. The diode is reverse-biased, and the current flows through the inductor and snubber circuit through the switch. The snubber circuit is also subjected to the input voltage. The voltage across inductor L is equal to the input voltage:

$$V_L = V_S \tag{1}$$

The rate of change of inductor current I_L is:

$$\frac{dI_L}{dt} = \frac{V_S}{L} \tag{2}$$

Integrating over the ON-Time (DT_{sw}):

$$I_{L_{on}} = \int_0^{DT_{sw}} \frac{V_S}{L} dt = \frac{V_S.DT_{sw}}{L} \tag{3}$$

The voltage across snubber capacitor C_s is equal to the input voltage V_S. Thus, the snubber resistor current is negligible during the steady state on-time i.e. I_{R_S}= 0. Where D and T_{sw} are duty cycle and switching period respectively.

3.2. OFF State (Switch S Open)

When the switch S is open, the energy stored in the inductor, L is transferred to the load through the diode, D and the snubber circuit mitigates the resulting voltage spike. The voltage and current across the inductor L are:

$$V_L = -V_{\text{out}} \tag{4}$$

$$\frac{dI_L}{dt} = -\frac{V_{\text{out}}}{L} \tag{5}$$

Integrating over the OFF-Time (1-D).T_{sw}:

$$\Delta I_{L_{off}} = \int_0^{(1-D)T_{sw}} -\frac{V_{\text{out}}}{L} dt = -\frac{V_{\text{out}}.(1-D)T_{sw}}{L} \tag{6}$$

When the switch is open, the snubber capacitor, C_s absorbs the transient voltage spike:

$$V_{C_s}(0) = V_S + \Delta V \tag{7}$$

where ΔV represents the transient voltage spike caused by the sudden interruption of the current through the inductor, L that occurs when switch "S" is open.

The snubber resistor dissipates the energy stored in the snubber capacitor and the voltage decays as:

$$V_{C_s}(t) = V_{C_s}(0)e^{-\frac{t}{R_S C_S}} \tag{8}$$

The current through the snubber resistor, I_{R_s}during the transient can be expressed as:

$$I_{R_s} = \frac{V_{C_S}}{R_S} = \frac{V_S + \Delta V}{R_S} \tag{9}$$

For a complete switching cycle, the inductor must return to its initial value. Thus, the change in inductor current over one period must be zero.

$$\Delta I_{L_{\text{on}}} + \Delta I_{L_{\text{off}}} = 0 \tag{10}$$

$$\frac{V_S.D\,T_{sw}}{L} - \frac{V_{out}.(1-D)T_{sw}}{L} = 0 \tag{11}$$

Simplifying, we get the steady-state voltage conversion ratio:

$$\frac{V_{out}}{V_S} = \frac{D}{1-D} \tag{12}$$

3.3. Calculation of Snubber Losses

The energy stored in the snubber capacitor during each switching is:

$$E_s = \frac{1}{2} C_s V_{C_s}^2 \tag{13}$$

During switch off-state:

$$E_s = \frac{1}{2} C_s (V_S + \varDelta V)^2 \tag{14}$$

The power dissipated in the snubber resistor in the energy stored per cycle times the switching frequency $f_{sw} = \frac{1}{T_{sw}}$

3.4. Total Power Losses of Converter

The total power loss of the buck-boost converter is:

$$P_{\text{Loss}} = P_{\text{MOSFET}_{\text{Loss}}} + P_{\text{Diode}_{\text{Loss}}} + P_{\text{Snubber}_{\text{Loss}}} + P_{\text{Capacitor}_{\text{Loss}}} + P_{\text{Inductor}_{\text{Loss}}} \tag{15}$$

The power loss of the MOSFET is given by:

$$P_{\text{MOSFET}_{\text{Loss}}} = P_{\text{Static}} + P_{\text{Dynamic}} = r_{ds_{on}}.{I_{rms}}^2 + \frac{V_S.I_{out}}{3} \tag{16}$$

where, $r_{ds_{on}}$ and ${I_{rms}}^2$ are the on-state resistance and rms current flowing through the MOSFET.

The diode power loss is:

$$P_{\text{Diode}_{\text{Loss}}} = V_F.I_{D_{Avg}} + r_D.{I_{D_{rms}}}^2 \tag{17}$$

where, V_F, r_D and $I_{D_{Avg}}$ are forward voltage drop, forward junction resistance and average current flowing through diode in the on state, respectively.

The power loss of the snubber circuit is:

$$P_{\text{snubber}} = E_s.f_{sw} = \frac{1}{2} C_s (V_s + \varDelta V)^2.f_{sw} \tag{18}$$

The power loss in inductor and capacitor are:

$$P_{\text{Capacitor}_{\text{loss}}} = ESR{I_{C_{rms}}}^2 \tag{19}$$

$$P_{\text{Inductor}_{\text{Loss}}} = r_{\text{Series}}.{I_{L_{rms}}}^2 \tag{20}$$

where, ESR, ${I_{C_{rms}}}^2$, r_{Series} and ${I_{L_{rms}}}^2$ are the equivalent series resistance, capacitor rms current, inductor series resistance and rms current flowing through the inductor, respectively.

The efficiency of the converter is given as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \tag{21}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{MOSFET}_{\text{Loss}}} + P_{\text{Diode}_{\text{Loss}}} + P_{\text{Snubber}_{\text{Loss}}} + P_{\text{Capacitor}_{\text{Loss}}} + P_{\text{Inductor}_{\text{Loss}}}} \tag{22}$$

4. SIMULATION AND RESULTS

The PSIM simulation tools are employed to conduct comprehensive performance evaluations of the proposed converter topology. Simulation tools typically do not account for parasitic errors, and the results produced by the simulation are generally presented in 2-D format. The simulation setup includes detailed specifications of all components, as shown in Table 1. Various operating scenarios are simulated to assess the converter's performance under different load conditions at 25 kHz switching frequencies.

Figure 4 presents the proposed converter output voltage at a 0.4 duty cycle and Figure 5 presents the proposed converter inductor and output current at a 0.4 duty cycle working as a buck converter. Similarly, Figure 6 presents the proposed converter output voltage at a 0.6 duty cycle and Figure 7 presents the proposed converter inductor and output current at a 0.6 duty cycle, working as a boost converter. The proposed converter with a snubber circuit, operating with a 40 V source voltage, switching frequency of 5 kHz, and duty cycles of 0.4 and 0.6, exhibits detailed performance characteristics in terms of inductor current, output current, and output voltage. At a duty cycle of 0.4, the converter operates predominantly in buck mode, stepping down source voltage to a lower output voltage. The inductor current peaks initially due to load resistance and the switching frequency, with the inductor charging during the on-phase of the switch and discharging during the off-phase. This current follows a triangular waveform due to the periodic energy storage and release within the inductor. The snubber circuit, consisting of resistors and capacitors, effectively reduces voltage spikes and oscillations caused by the switching process, ensuring smoother transitions and reducing EMI. This helps in protecting the semiconductor devices and enhancing the overall efficiency of the converter. The output current in this mode remains relatively steady, reflecting the average value of inductor current, and output voltage typically drops to around 16 V. When the duty cycle is increased to 0.6, the converter shifts to boost mode, increasing the input voltage to a higher

Table 1. Hardware component specifications

Component	Specifications
Inductor	320mH
Capacitor	$C = 470$ uF, $C_s = 10$ nF
Diode	1N4002
MOSFET	IRFZ44
Snubber Resistance	$R_s = 10\ \Omega$

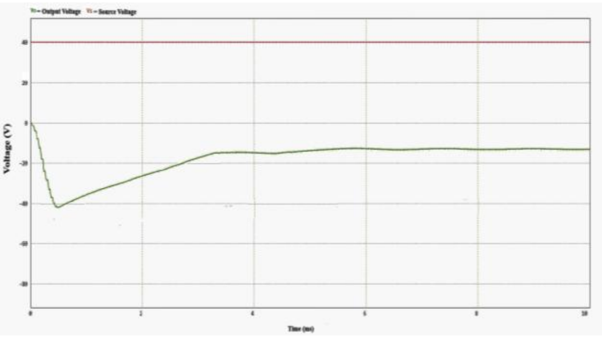

Figure 4. Proposed converter output voltage at 0.4 duty cycle

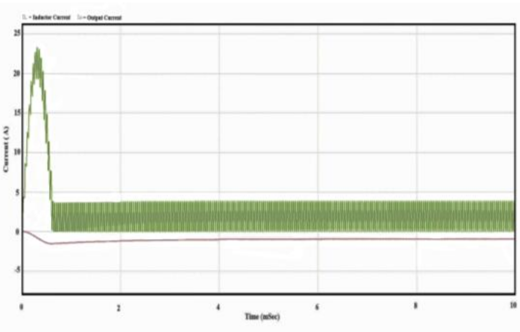

Figure 5. Proposed converter inductor and output voltage at 0.4 duty cycle

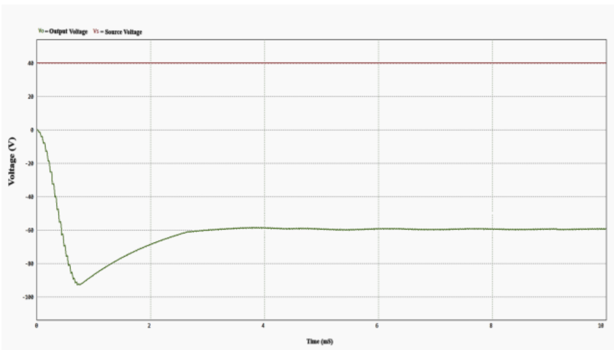

Figure 6. Proposed converter output voltage at 0.6 duty cycle

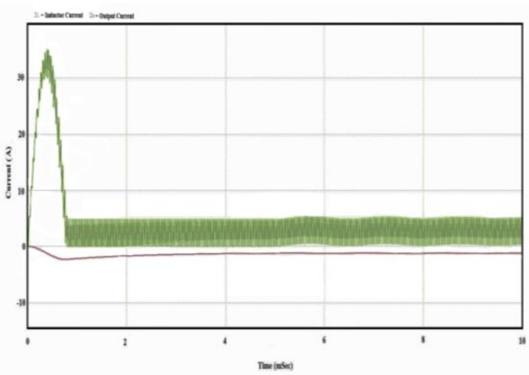

Figure 7. Proposed converter inductor and output voltage at 0.6 duty cycle

output voltage. In this mode, the inductor current retains its triangular waveform but exhibits higher peak values initially, as the inductor must store more energy to be transferred to the output during each cycle. The higher duty cycle results in increased energy transfer per cycle, leading to a higher output voltage of 60V. The snubber circuit plays a critical role in improving the performance of the converter by mitigating adverse effects of high-frequency switching, such as voltage spikes, which can cause increased stress and potential damage to the switching elements. By absorbing and dissipating the energy of parasitic inductances, the snubber circuit reduces switching losses and enhances the reliability of the converter. This leads to improved efficiency, especially important in high-frequency applications where fast and efficient switching is crucial. Additionally, the snubber circuit helps in maintaining the integrity of the output voltage by preventing overshoots and ensuring a more stable and consistent output.

The proposed converter with a snubber circuit offers significant improvements over a conventional buck-boost converter in terms of performance characteristics such as inductor current, output current, output voltage, efficiency, and thermal management. In the conventional design, the inductor current follows a triangular waveform but is prone to voltage spikes and ringing due to rapid switching transients, leading to higher peak currents and increased EMI. The proposed converter, however, maintains a smoother inductor current waveform, with the snubber circuit effectively suppressing voltage spikes and reducing EMI, resulting in lower stress on the switching elements and improved efficiency. The output current in the conventional converter can experience increased ripple due to these transients, necessitating additional filtering, whereas the proposed converter achieves a more stable output current with reduced ripple. Similarly, the output voltage in the conventional design is susceptible to fluctuations and overshoots caused by switching transients, compromising performance and reliability. In contrast, the proposed converter stabilizes the output voltage more effectively, achieving reliable voltage regulation of 16 V at a 0.4 duty cycle and 60 V at a 0.6 duty cycle with fewer fluctuations. Efficiency is also higher in the proposed converter due to reduced switching losses, with the snubber circuit absorbing and dissipating energy from voltage spikes, leading to better thermal management and reduced stress on components.

To study the buck-boost converter with SiC and GaN JLFETs, its behavior must be analyzed. Therefore, the specifications presented in Table 2. are considered-for simulation on the TCAD platform for Si, SiC, and GaN. The switching characteristics of Si, SiC and GaN JLFETs are critical to the performance of buck-boost converters utilizing snubber circuits. Figure 8, Figure 9 and Figure 10 presents the switching characteristics plot of Si, SiC and GaN at a gate to source voltage of 4 V respectively. Si JLFETs exhibit relatively slower switching speeds due to their higher parasitic capacitances and longer carrier lifetimes, which leads to increased switching losses and reduced efficiency in the converter. SiC JLFETs improve upon this with faster

Table 2. Specifications for simulation

Quantity	Specifications
Doping concentration (N_d)	10^{19} /cm^3
Channel length (L)	0.10 µm
Source drain length (L_s, L_d)	0.05 µm
Channel thickness (t_{ch})	0.01 µm
Source drain thickness (t_s, t_d)	0.02 µm

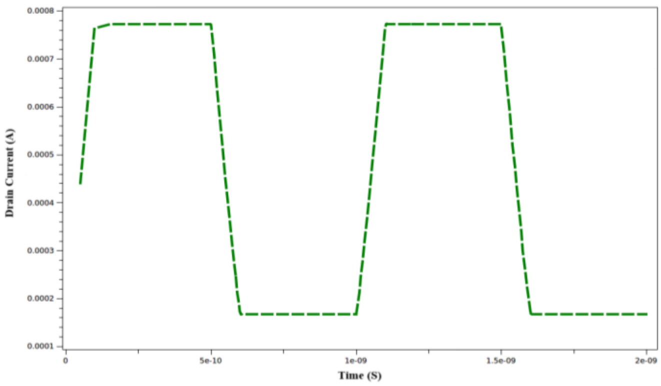

Figure 8. Switching characteristics of Si at the gate to source voltage of 4 V

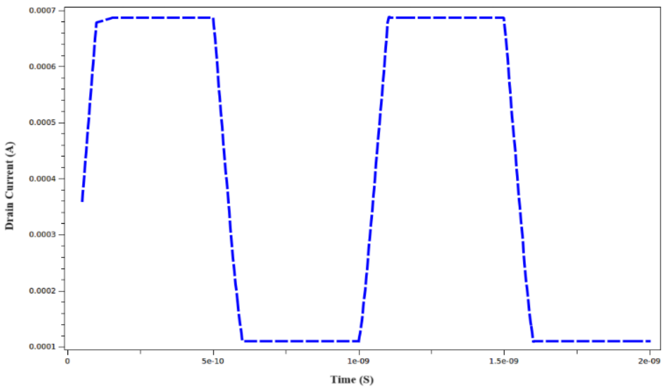

Figure 9. Switching characteristics of SiC at the gate to source voltage of 4 V

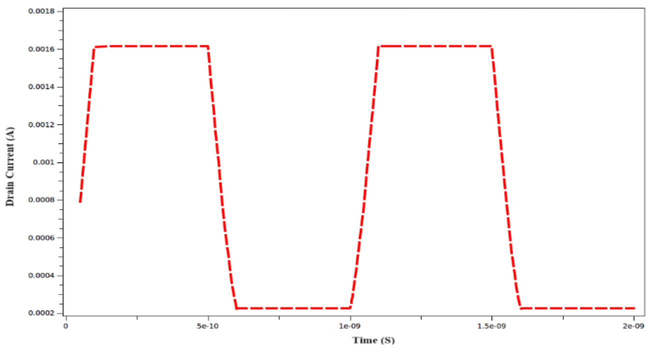

Figure 10. Switching characteristics of GaN at the gate to source voltage of 4 V

switching capabilities due to lower parasitic capacitances and shorter carrier lifetimes, resulting in reduced switching losses and improved efficiency, especially in high-power applications. GaN JLFETs provide the fastest switching speeds among the three, attributed to their exceptionally low parasitic capacitances and extremely short carrier lifetimes. This results in minimal switching losses, enabling the buck-boost converter to operate with maximum efficiency and high-frequency performance. Consequently, while Si JLFETs may be adequate for lower power applications, SiC and GaN JLFETs, particularly GaN, are preferred for high-efficiency and high-speed applications due to their superior switching characteristics.

The input and output characteristics of Si, SiC, and GaN JLFETs play a crucial role in determining the performance of converters using snubber circuits. Figure 11 and Figure 12 present the output and transfer characteristics plot of Si, SiC and GaN respectively at a gate to source voltage of 6 V and a drain to source voltage of 6V respectively. Si JLFETs typically exhibit higher threshold voltages, which can result in slower switching speeds and increased conduction losses, thereby reducing the overall efficiency of the converter. Their transconductance is relatively lower, meaning that the current drive capability is not as strong as in SiC and GaN JLFETs. Additionally, Si JLFETs have a steeper subthreshold slope, leading to higher leakage currents, which further impacts efficiency negatively. On the other hand, SiC JLFETs demonstrate lower threshold voltages and higher transconductance compared to Si, which enhances switching performance and reduces conduction losses, making them more suitable for high-power applications. They also exhibit a gentler subthreshold slope, indicating better control over leakage currents. GaN JLFETs, however, outperform both Si and SiC with the lowest threshold voltages and the highest transconductance, enabling extremely fast switching and minimal conduction losses, which significantly boosts the efficiency of the buck-boost converter. Their subthreshold slope is the gentlest, providing superior control over leakage currents and ensuring optimal performance. Thus, in a buck-boost converter equipped with a snubber circuit, GaN JLFETs offer the highest efficiency and performance, followed by SiC, with Si JLFETs being the least efficient in comparison.

The thermal characteristics of Si, SiC, and GaN JLFETs have significant influence on the drain current versus drain-to-source voltage behaviors. Figure 13 shows thermal characteristics of Si, SiC and GaN at 300°C. Si JLFETs exhibit moderate thermal conductivity, with significant performance degradation as temperature increases, leading to higher on-state resistance and reduced drain current. SiC JLFETs, with their high thermal conductivity, show better thermal stability, maintaining higher drain current levels for a given V_{DS} even at elevated temperatures due to less dramatic increases in on-state resistance. GaN JLFETs possess the highest thermal conductivity and exhibit minimal performance degradation with temperature rise, maintaining low on-state resistance and high drain current, making them ideal for high-frequency, high-efficiency, and high-temperature applications. Thus, while Si JLFETs are less suitable for high-power environments, SiC and GaN JLFETs, especially GaN, offer superior thermal performance, ensuring consistent efficiency and reliability.

The efficiency plot of the proposed converter with Si, SiC, GaN JLFET and conventional converter are shown in Figure 14. Si JLFETs exhibit lower efficiency due to higher conduction and switching losses, making them suitable for low to medium power applications. SiC JLFETs, with their higher thermal conductivity and breakdown voltage, offer better efficiency at higher load currents, making them ideal for high-power applications. GaN JLFETs demonstrate the highest efficiency across all load conditions, owing to their superior electron mobility and faster switching capabilities, making them the best choice for applications requiring high efficiency and fast switching speeds. Although Si is more cost-effective, the enhanced performance of SiC and GaN

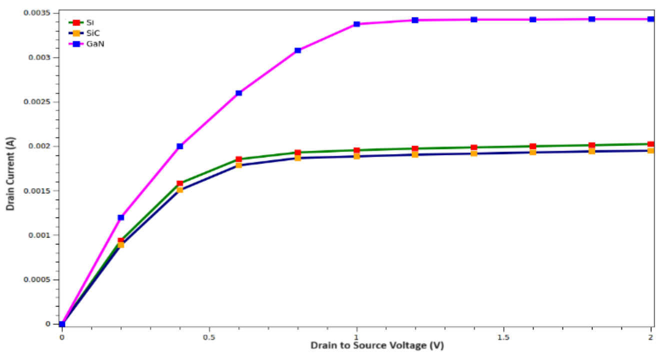

Figure 11. Output characteristics plot (I_d versus V_{ds}) of Si, SiC and GaN MOSFET at 6 V

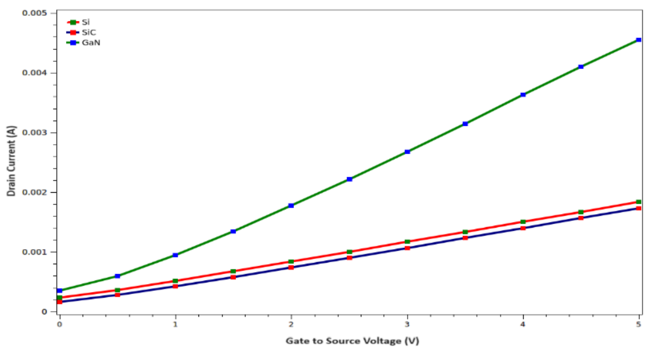

Figure 12. Transfer characteristics plot (I_d versus V_{gs}) of Si, SiC and GaN MOSFET at 6 V

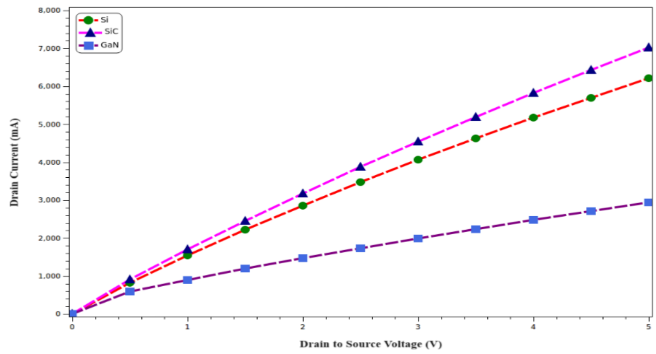

Figure 13. Thermal characteristics of Si, SiC and GaN at 300°C

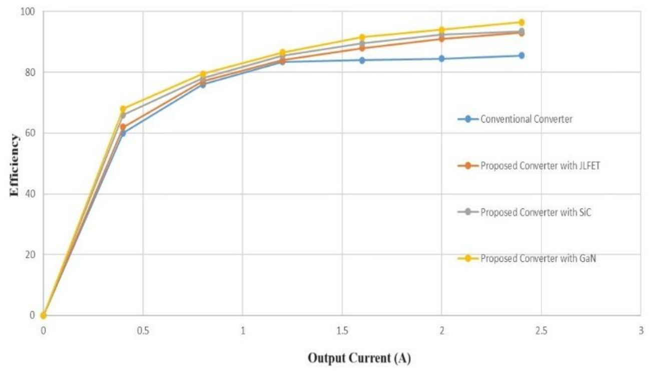

Figure 14. Efficiency plot of the proposed converter with Si, SiC, GaN JLFET and conventional converter

justifies their higher cost in applications where efficiency and thermal management are critical. The snubber circuit absorbs and dissipates excess energy that would otherwise cause stress on the components and reduce overall efficiency. The peak efficiency of the proposed converter with Si, SiC, and GaN JLFETs semiconductors reaches around 90% whereas the conventional converter peaks at about 85%, highlighting the benefits of incorporating a snubber circuit with advanced semiconductors.

The graphs illustrate key parameters like voltage, current, efficiency, ripple, and switching losses in a buck-boost converter. Voltage and current waveforms may show how the snubber circuit reduces overshoots and oscillations, leading to smoother transitions, better voltage regulation, and reduced component stress. Advanced semiconductors, such as MOSFETs or GaN FETs, likely improve switching speed and lower losses, enhancing efficiency. Ripple reduction is another key observation, as the snubber circuit and advanced semiconductors improve output quality by minimizing ripple voltage and current. Thermal performance graphs may show that the snubber circuit distributes switching energy more evenly, reducing component heating, while advanced semiconductors, with their higher power density capability, further improve thermal management. When comparing these findings to other works, several improvements stand out. In [17] with the use of passive snubber circuits in DC-DC boost converters to achieve high efficiency by minimizing switching losses presents significant improvements in overall converter performance, demonstrating the effectiveness of snubbers in reducing energy dissipation during switching. The work [18] provides a detailed methodology for designing snubber circuits to limit voltage and current spikes, ensuring smoother operation of power circuits. This work shows higher gains due to advanced semiconductors like GaN or SiC, which offer even lower switching losses and faster response times than traditional MOSFETs used in the cited studies. Other studies also highlight significant ripple reduction with active snubber circuits, up to 20-30%, which aligns with these findings. While GaN-based converters show reduced switching losses, this study's use of both snubber circuits and advanced semiconductors likely achieves even lower losses. The thermal performance aligns with other research on SiC and GaN devices, which show better heat dissipation and lower operating temperatures. Overall, the combination of snubber circuits and advanced semiconductors offers notable advancements in efficiency, ripple reduction, and thermal management over traditional designs. A GaN-based DC-DC resonant boost converter [19] demonstrates very high efficiency and precise voltage gain control due to GaN's faster-switching speeds and lower losses. The performance of cascade GaN FET, SiC JFET, and Si IGBT devices in a buck-boost converter [20], shows that GaN FETs offered the best trade-off between efficiency and switching losses. A comparative study of GaN, SiC, and Si-based DC-DC converters [21] concluded that GaN and SiC devices significantly outperform silicon-based converters in terms of efficiency and switching performance. Additionally [22] evaluated the temperature-dependent characteristics and performance of power converters using GaN, SiC, and Si devices, providing insights into the thermal management and efficiency of these technologies under varying operational conditions. When compared with proposed work the use of advanced semiconductors like GaN and SiC is a common theme across these studies. However, this work on enhanced buck-boost converters goes a step further by integrating a snubber circuit with these devices, achieving better ripple reduction, lower switching losses, and improved thermal management. While previous works highlight the advantages of GaN and SiC in reducing losses and enhancing efficiency, the combination of these semiconductors with snubber circuits, as presented in the enhanced buck-boost converter, represents a more comprehensive approach to improving converter performance in demanding applications.

To ensure the simulation of the buck-boost converter is reliable, even without explicitly considering overheating or component sizes, several key strategies should be applied. First, accurate modeling of advanced semiconductor devices, such as GaN or SiC transistors, and snubber circuits is crucial. This includes accounting for real-world characteristics like switching times, ON resistance, and parasitic capacitances. By simulating these components accurately, the performance under various operating conditions can be better predicted. Next, testing the converter across a wide range of input voltages, load conditions, and switching frequencies helps verify the converter's performance under different scenarios. This ensures that efficiency, stability, and functionality remain consistent. Although overheating isn't directly modeled, a careful loss estimation focusing on switching and conduction losses provides insights into potential thermal stress areas. Such calculations can reveal how efficiently the converter dissipates energy, indicating whether excessive heat might be an issue in actual hardware. Efficiency and ripple reduction are important performance metrics that should be thoroughly tested across different operating conditions. By simulating efficiency curves and examining ripples in voltage and current, the design's robustness can be assessed. Incorporating parasitic effects, such as stray inductances and capacitances, in the model also enhances simulation accuracy by accounting for real-world inefficiencies that can impact switching behavior.

5. CONCLUSION

Overall, this research demonstrates that the enhanced buck-boost converter with a snubber circuit offers superior performance compared to traditional designs. The simulation study presented in this paper demonstrates the superior performance of proposed buck-boost converter topology compared to conventional designs. The innovative design features contribute to improved efficiency, reduced voltage ripple, and enhanced transient response, addressing key challenges in power electronics applications. Future research will focus on experimental validation and optimization of the proposed topology for practical implementation.

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