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Enhancing circuit development and layout implementation of benchmark circuit in 0.18-µm CMOS technology

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ABSTRACT

Power consumption and delay are the most critical factors in circuit development and layout implementation. It is challenging to optimize all aspects simultaneously. This research addresses this challenge by analysing the power consumption and delay effects in benchmark circuit operation, C6288, using 0.18-µm CMOS technology operating at an optimal voltage of 1.6V. Additionally, this research also contributes to developing the initial layout implementation of a benchmark circuit with a 10% area reduction. By utilizing new layout techniques and simulations, the study has proven a significant decrease in power consumption and enhanced area optimization with a moderate increase in delay at 1.6V, all while maintaining acceptable performance standards. In addition, simulation results indicate less than a 10% deviation between pre- and post-layout designs. Finally, through the properties of layout design and the research conclusions, it has provided valuable insights for the design of energy-efficient digital circuits in CMOS technology.

Keywords: *Layout implementation, Benchmark circuit, Power consumption, Delay effects area optimization, CMOS technology*

1. INTRODUCTION

The CMOS circuit plays a significant role in today's digital and mixed-signal applications, where efficiency and performance are achieved through the design of integrated circuits using Complementary Metal-Oxide-Semiconductor (CMOS) technology. Known for its low power consumption and high noise immunity criteria, CMOS technology will be an ideal option for this research study. However, as device dimensions continue to shrink to meet the demands for faster and more power-efficient systems, managing power consumption and delay which is due to many aspects such as load capacitance, resistance and transistor sizing in CMOS circuits has become increasingly challenging [1-5]. This research seeks to address these challenges by implementing effective techniques in the layout development of the benchmark circuit C6288.

The C6288 circuit as shown in Figure 1 is a prominent benchmark commonly used in IC floor planning research [6-10]. The development of its layout begins with defining the circuit's functionality and creating a schematic design that serves as a blueprint of interconnected CMOS transistors. After simulating the schematic to ensure its logic and performance, the design progresses to the layout stage which is the most crucial part of the overall design process. Layout implementation is where the design of integrated circuits (ICs) transitions from conceptual schematics to detailed physical structures on silicon wafers. The layout process involves precise placement and routing of these transistors, interconnects, and other components within the limited space of the silicon die. Any errors or inefficiencies at this stage can adversely affect the functionality, speed, and power consumption of the final CMOS chip, making it a critical aspect of developing the benchmark circuit.

The core layout of the C6288 as a multiplier involves an arrangement of half adders and full adders configured to manage both power efficiency and processing speed. Given that the benchmark circuit consists of numerous full adders, addressing power consumption and delay early in the circuit development is essential since power reduction is

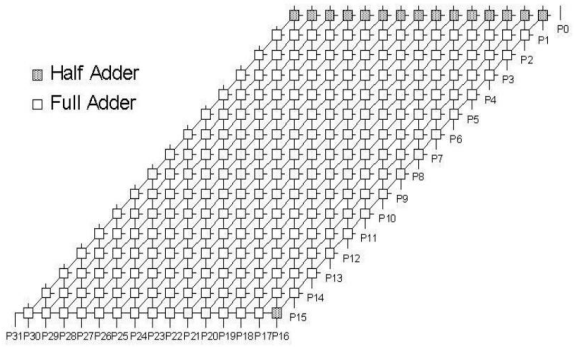

Figure 1. Benchmark circuit of C6288 consisting of Full-adders and Half-adders [4]

crucial to the VLSI circuit design process [11]. To assess how well floor planning algorithms perform, a 256-cell multiplier circuit is utilized, where each cell is a 4x4-bit multiplication unit, resulting in a total 1024-bit output for the entire multiplier circuit. On the other hand, using the device in the subthreshold area will result in significant leakage, which is best described as a parasitic leakage in a situation where there should be no current [12]. These considerations are also crucial for ensuring the circuit's effectiveness and efficiency, particularly in battery-operated devices where power conservation is vital.

A good digital circuit requires a reduction in the power delay product (PDP), which may be obtained by enhancing a few factors like the width-to-length (W/L) ratio. When building VLSI circuits, we are constantly searching for new designs because our primary goal is to minimize size, power consumption, and latency to optimize design performance. Despite that, finding the ideal design to achieve our goals feels like an endless challenge. Our primary objective is to optimize performance while minimizing resource consumption [13]. In terms of layout area optimization, serpentine routing and device stacking offer substantial improvements in power consumption and layout accuracy for CMOS oscillators [14]. Despite increased layout complexity due to its intricate geometric pattern and increased wiring length, designers can achieve more consistent signal propagation and minimal timing discrepancies by routing wires in a serpentine pattern. Besides, this method reduces interconnection and parasitic capacitances through the separation or confinement of high-speed logic to their specific functions, and minimizing the source and drain surface area, respectively [15]. As a result, it enhances noise immunity by reducing crosstalk and noise reception of the circuits [16, 17]. Since this method primarily equalizes the length of parallel signal paths, it is therefore crucial to carefully balance the benefits of reduced delay mismatches and reduced crosstalk against the penalties of increased wiring length [18]. Given the demonstrated effectiveness of these methods in previous works, this project will integrate serpentine routing and stacking techniques to achieve its design objectives.

As for this research, the focus is on developing a benchmark circuit C6288 using 0.18μm process technology in Cadence software. The optimal operational voltage is determined to maximize power consumption without increasing delay. Additionally, the initial layout design must optimize area utilization and be implemented by the recent layout serpentine technique. By carefully optimizing transistor and layout parameters, significant reductions in energy consumption can be achieved while still meeting performance requirements [19]. This is especially important in applications where low power consumption is needed, such as in battery-powered devices or where power consumption significantly impacts operational costs [20].

2. DESIGN METHODOLOGY

This research employs a systematic design stage to achieve the objective of this research. The development begins with adapting the benchmark circuit from its original technology to the Silterra 0.18µm process using several techniques. Following this adaptation, the serpentine layout technique will be implemented which simplifies the routing of metals in the layout design to optimize the area. This approach is aimed at ensuring the circuit meets the required performance and efficiency standards.

2.1. Benchmark Circuit Implementation

The physical design of the circuit is organized into three levels which are standard cells (N-0), full and half adders (N-1), and the completed benchmark circuit (N-2). This hierarchical approach, represented by N-levels, simplifies the design process, allowing for easier error resolution and debugging without compromising the integrity of the higher-level circuits. The development of the benchmark circuit begins with the construction of Full-Adders and Half-Adders, utilizing NAND, XOR, and AND gates. These fundamental components are crucial for executing arithmetic operations in digital circuits.

Full-Adders combine three input bits to produce both a sum and a carry-out, while Half-Adders process two input bits to generate a sum and a carry. The strategic use of NAND, XOR, and AND gates ensures a versatile and efficient implementation of addition logic. Each gate's inputs and outputs are carefully arranged in accordance with the logic diagrams for Full-Adders and Half-Adders. During this process, the parameters of each transistor are adjusted to the optimized design specifications. This is to ensure that all transistors have no difference in variables, making sure that the results obtained are absolute. Figure 2 displays the fully constructed benchmark circuit, showcasing the integration of these gates. Accurate interconnection of these gates is essential for the proper flow of data and carrying bits throughout the circuit. Thorough testing and simulation are employed to validate the correctness and functionality of the base circuit prior to its incorporation into the benchmark circuit, ensuring its reliability and performance in practical applications. The outcomes of these simulations will be highlighted in the results section.

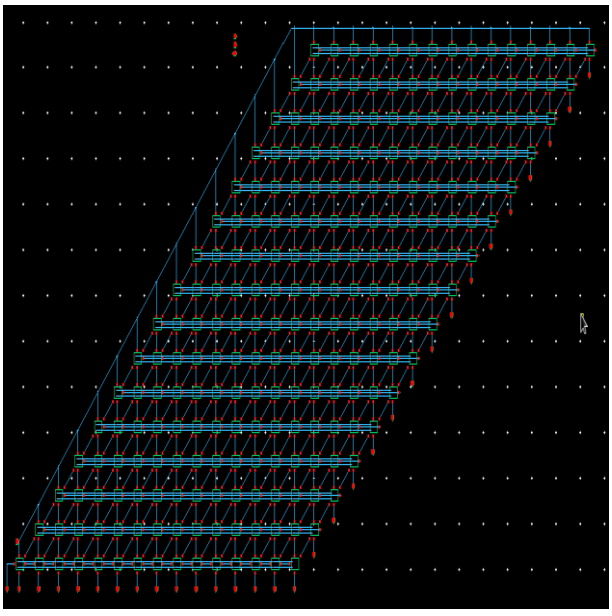

Figure 2. Benchmark circuit of C6288

2.2. Layout Design Implementation

The layout generated from the circuit must be symmetrically arranged to optimize net routing efficiency. Thorough management of the spacing between NMOS and PMOS transistors relative to the boundary is essential. Following the placement of components, routing is performed using metal layers. The routing process involves creating electrical connections between the placed components, ensuring the signal integrity and optimizing the performance. The routing sequence is carefully designed to prioritize critical circuit connections, ensuring that critical networks are routed efficiently while maximizing the use of available routing resources. Metal 5 is used to connect critical signals such as power and ground, where the signal is routed with metal 4 to maximize area usage, as illustrated in Figure 3. Shielding wires are placed parallel to sensitive signal cables to prevent interference, and power or ground nets are strategically routed to provide stability to the circuit.

This detailed routing approach helps optimize the layout, reducing the overall area and enhancing the reliability of the final design. Furthermore, by incorporating metal track patterns, sufficient spacing between metals is maintained, thereby reducing the risk of errors and contributing to the robustness of the circuit. In this study, the width and distance between metals were precisely evaluated for the layout design including the full adder and half adder design as depicted in Figure 4 and Figure 5.

The initial floorplan is designed using the serpentine technique, which arranges the components in a snake-like pattern to maximize the use of available space and minimize interconnect lengths. This technique is chosen for its efficiency in optimizing the layout, ensuring that the critical components are placed strategically to facilitate subsequent processes. As a result, all stages and metal placements are completed effectively as shown in Figure 6. A well-designed floorplan reduces interconnect lengths, minimizes delays, and optimizes space usage, thereby improving overall chip performance and manufacturability.

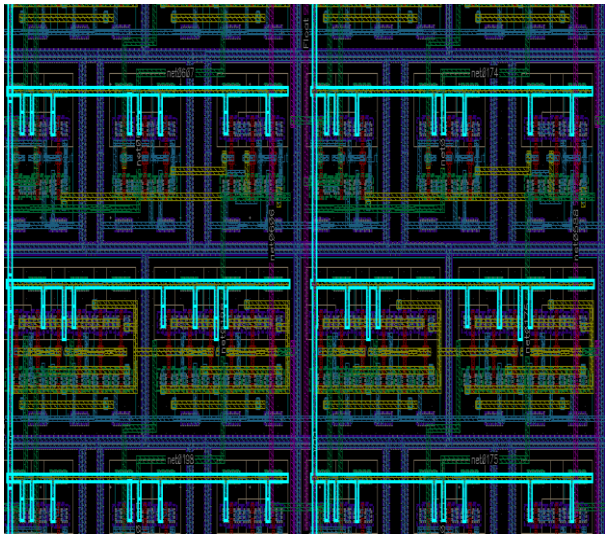

Figure 3. Power rails and metal routing close inspection

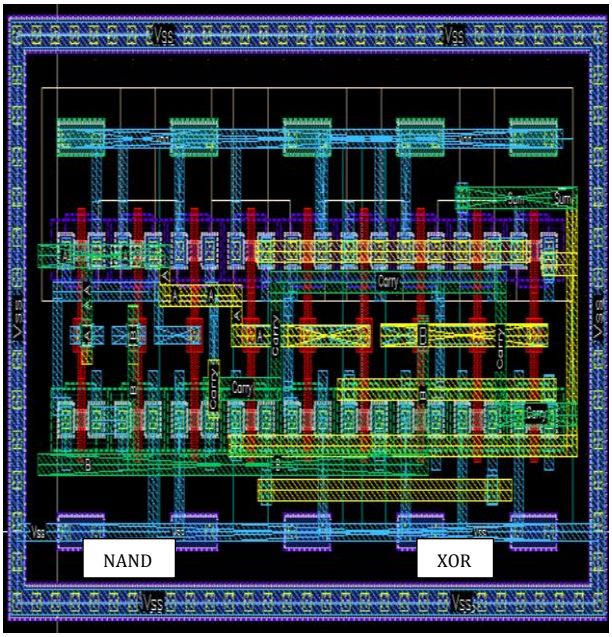

Figure 4. Half-adder layout implementation

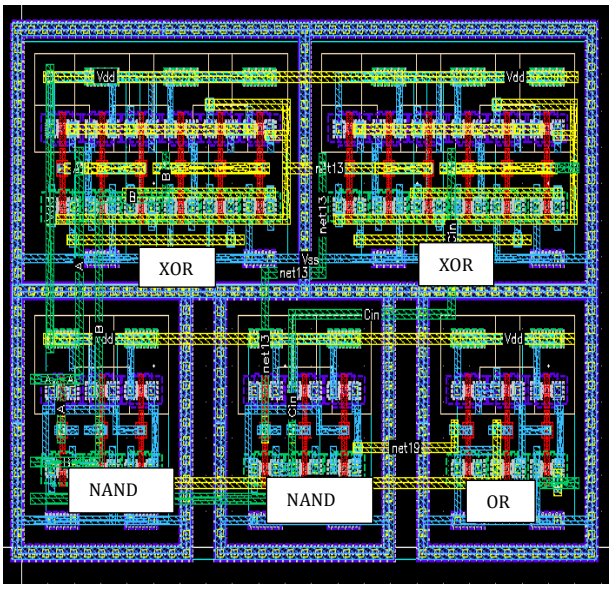

Figure 5. Full-adder layout implementation

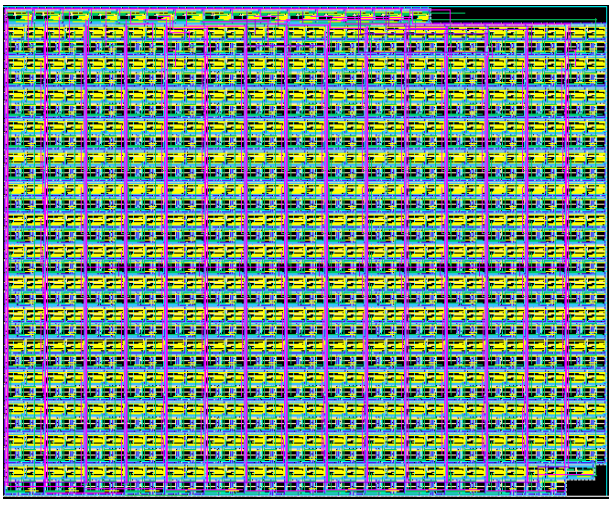

Figure 6. Benchmark circuit layout view

3. RESULTS AND DISCUSSION

3.1. Area Optimization

As mentioned above, the cells are placed according to the schematic arrangement considering the minimum values of the DRC rules as depicted in Figure 7. This is done to maximize the area used while complying with the circuit's expected output and parameters used. The earlier-mentioned serpentine technique is employed to enhance area efficiency and maintain accuracy in post-layout simulation. This method ensures strong power distribution and grounding connections to each device, contributing to effective area reduction. As presented in Table 1, the area of each cell was measured both before and after applying area optimization techniques. Given that no previous layout implementation exists for this circuit, the generated layout serves as a valid benchmark for evaluating these optimization methods. The results indicate that significant area reduction is achieved in lower-level cells, which can be attributed to the greater flexibility in CMOS placement and routing at these levels.

However, as the circuit level increases, the percentage of area reduction diminishes due to the increasing design constraints and limitations. The reduced area percentage at the highest circuit level is further impacted by the presence of guard rings. Theoretically, removing these guard rings could lead to an even greater area reduction. Additionally, the serpentine technique has proven how efficient metal routing can significantly minimize chip area.

3.2. Power and Delay Trade-offs

There is a fundamental trade-off between power consumption and delay in digital circuits. Lowering the operating voltage reduces power consumption but increases the delay. This trade-off is critical in the design of energy-efficient circuits. Achieving the optimal balance involves finding a voltage that minimizes power without causing unacceptable delays. Tables 2 and 3 show the tabulated data from pre-layout and post-layout simulation of the benchmark circuit. The initial values of all the parameters are measured and tabulated to be compared to the post-layout simulation. From the pre-layout simulation, the power consumption is 73.08 µW at an operating voltage

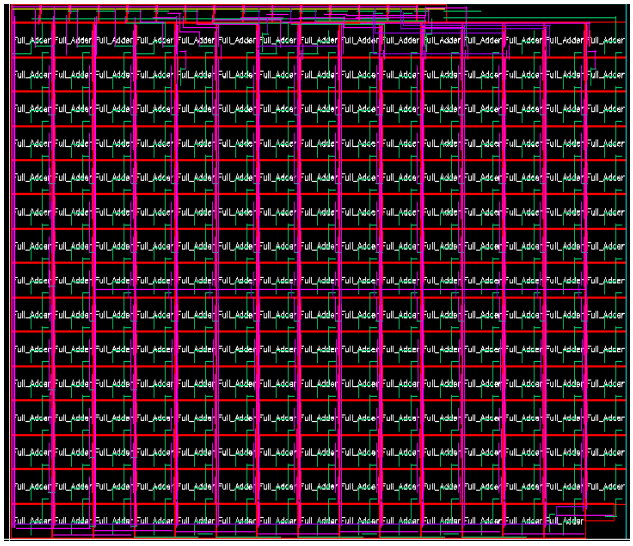

Figure 7. Floor planning device placement after minimum spacing rule

of 1.8 V. Reducing the operating voltage to 1.6 V decreases the power consumption to 50.29 µW, and further lowering it to 1.4V results in a power consumption of 32.17 µW. The delay per gate at 1.8 V is 0.20 ns.

The delay behavior observed in both the 15-gate and 32-gate paths reveals important insights into the impact of voltage scaling on circuit performance. When the voltage is reduced to 1.6 V, the delay increases to 0.224 ns for pre-layout and 0.25 ns for post-layout. At 1.4 V, the delay further rises to 0.3 ns and 0.34 ns for pre-layout and post-layout, respectively. A similar trend is observed in the 15-gate path, where the delay increases from 3.14 ns at 1.8 V to 4.45 ns at 1.4 V. The 32-gate path has the same behavior, with delays increasing as voltage decreases. The 15-gate path represents the longest delay path, hence, a substantial increase in delay is observed as the operating voltage is reduced from 1.8 V to 1.0 V. This is attributed to the slower transistor switching speeds at lower voltages, particularly in more complex gates that require longer to propagate signals. Equally, the 32-gate path, despite having more gates, exhibits a shorter overall delay compared to the 15-gate path across the same voltage range. This is due to the simpler gates and lower parasitic effects in the 32-gate path, which allow for faster switching.

Table 1. Area difference in comparison to source-generated floor planning

Cell Name		Width (µm)	Length (µm)	Area (µm²)	Area reduction percentage (%)
Full layout	Source generated	363.375	246.255	89.48×10^3	18.17%
	Optimized	327.465	223.595	73.22×10^3	
Full Adder	Source generated	27.12	16.47	446.58	25.96%
	Optimized	22.26	14.86	330.67	
XOR cell	Source generated	9.27	12.77	118.38	52.49%
	Optimized	9.58	5.87	56.24	

Table 2. Pre-layout simulation data of power consumption and delay of the circuit. Delay 15 gates refer to the longest delay path whilst delay 32 gates refers to the shortest delay path

Operating Voltage (V)	Current (µA)	Power Consumption (µW)	Delay per gate (ns)	Delay 15 gates (ns)	Delay 32 gates (ns)
1.8	40.6	73.08	0.20	3.14	0.109
1.6	31.4	50.29	0.22	3.64	0.126
1.4	23.0	32.17	0.30	4.45	0.146
1.2	15.5	18.6	0.40	5.91	0.21
1.0	9.27	9.27	0.70	9.01	0.382

Table 3. Post-layout simulation data of power consumption and delay of the circuit. Delay 15 gates refer to the longest delay path whilst delay 32 gates refers to the shortest delay path

Operating Voltage (V)	Current (µA)	Power Consumption (µW)	Delay per gate (ns)	Delay 15 gates (ns)	Delay 32 gates (ns)
1.8	45.4	81.79	0.23	3.52	0.123
1.6	35.2	56.29	0.25	4.07	0.141
1.4	25.7	35.99	0.34	4.97	0.163
1.2	17.3	20.81	0.45	6.61	0.235
1.0	10.4	10.37	0.78	10.08	0.428

The trade-off between lower power consumption and increased delay is evident in both paths and it becomes more pronounced at lower voltages. This shows the importance of balancing power efficiency with performance, particularly in low-power designs where voltage scaling is a key technique. From the tabulated data, it is observed that the optimal operating voltage of 1.6V balances the reduction in power consumption with an acceptable increase in delay. This voltage provides a significant power reduction compared to 1.8 V, while maintaining a delay that is not excessively high, making it suitable for practical applications and an efficient choice for balancing performance and energy efficiency. Additionally, results from pre-layout and post-layout simulations indicate a slight difference, with calculations showing a difference of approximately 11 % for all parameters at all voltages. This discrepancy arises because pre-layout simulations do not account for parasitic elements and other real-world effects inherent in the physical layout, leading to more optimistic estimates of power consumption and delay. In contrast, post-layout simulations incorporate these parasitic, resulting in more accurate and typically higher estimates. For a layout to be considered optimal for tape-out, the stage where the circuit design is finalized and prepared for manufacturing, the difference between pre- and post-layout simulations for digital circuits should ideally be less than 15 %. Hence, the measured simulation gap of 11% is considered acceptable to ensure a reliable and efficient design ready for tape-out. Achieving this threshold indicates that the layout is well-optimized, accurately reflecting the expected performance and minimizing discrepancies between initial predictions and real-world outcomes. An optimal layout ensures that the design will perform as intended once manufactured, reducing the risk of costly post-manufacturing modifications. Therefore, maintaining a difference percentage below 15 % is crucial.

4. CONCLUSION

In conclusion, this research has been conducted successfully by developing, implementing layout and area-optimizing techniques in the design of the benchmark circuits. By utilizing the serpentine technique for the initial floorplan and strategic placement and routing of components, the layout achieved significant space efficiency and minimized interconnect lengths. In addition, through extensive simulations, the power consumption and delay across both circuit design and layout were compared. The simulations allow for a detailed comparative analysis by evaluating the difference percentage between the two approaches and demonstrating how the design of the layout significantly impacts and influences circuit performance. Summarizing the findings from the research, the serpentine layout technique exhibited superior capability in the handling process evidenced by the lowest power consumption and optimal delay times obtained from the simulations. Overall, this research illustrates the importance of proper layout design and voltage management in optimizing circuit performance.

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