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Numerical Simulation on the Impact of Back Gate Voltage in Thin Body and Thin Buried Oxide of Silicon on Insulator (SOI) MOSFETs

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ABSTRACT

Silicon-on-Insulator (SOI) technology provides a solution for controlling Short-Channel Effects (SCEs) and enhancing the performance of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). However, scaling down SOI MOSFETs to a nanometer scale does not necessarily yield further scaling benefits. Introducing multiple gates, such as a double gate configuration, can effectively mitigate SCEs. Nonetheless, fabricating a flawless double gate structure is an exceedingly challenging endeavor that remains unrealized. The adoption of a back gate bias, with an asymmetrical thickness arrangement between the front and back gates, mimicking the behavior of a double gate, offers an alternative approach. This approach has the potential to modify the electrical characteristics of the device, thus potentially leading to improved control over SCEs. In this study, we employed 2D simulations using Atlas to investigate the influence of back gate biases, namely, -2.0 V, 0 V, and 2.0 V on a 10 nm silicon thickness at the top and a 20 nm buried oxide thickness for n-channel MOSFETs. We focused on key parameters, including threshold voltage (V_{Th}), Drain Induced Barrier Lowering (DIBL), and Subthreshold Swing (SS). The results demonstrate that a negative back gate bias is the most favorable configuration, as it yields superior performance. This translates into more effectively controlled SCEs across all the parameters of interest.

Keywords: SOI MOSFETs, Multiple gates MOSFETs, Negative back gate bias MOSFETs

1. INTRODUCTION

The MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) was first invented by Mohamad Atalla and Dawon Kahng at Bell Labs in 1959. Their invention led to revolutionized in the field of electronics and laid the foundation for modern integrated circuit technology. The MOSFET's ability to amplify and switch the electronic signals with high efficiency and low power consumption has made it a fundamental component in a wide range of electronic devices and systems. A typical structure of a MOSFET consists of a source, a drain, a gate and a body. The successful of MOSFET has been driven by the success of scaling the MOSFETs which leads to more functionalities and improved performances. However, aggressive technology scaling instigates the short-channel effects (SCE) and may lead to reliability issues. The SCEs are attributed to the limitation imposed on the electron drift in the channel and the change of threshold voltage of the device due to the shortening of channel length. The SCEs includes drain-induced barrier lowering (DIBL), subthreshold slope (SS), I_{off}, I_{on}, velocity saturation, surface scattering, impact ionization, and hot carrier effect.

One of the proposed structure modifications to minimize the SCEs is SOI MOSFET. It is done by inserting an insulating layer, called buried oxide (BOX) layer right under the transistor's

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channel. The SOI MOSFET can minimize the parasitic capacitance effect so that the device can operated in higher speed, handle high temperature and high voltage. The downsizing of the SOI MOSFET has been an attractive to be explored by researcher with various architectures. Currently, the application of ultra-thin body and buried oxide (UTBB) on SOI MOSFET had been developed and has further improved the SCEs and front-gate-to-channel controllability. Figure 1 shows the evolution of MOSFET from bulk wafer to silicon-on-insulator. In silicon-on-insulator the evolution can be seen from partially-depleted SOI until fully depletion SOI, which can be achieved in SOI technology, shown in Fig. 1 c) and d).

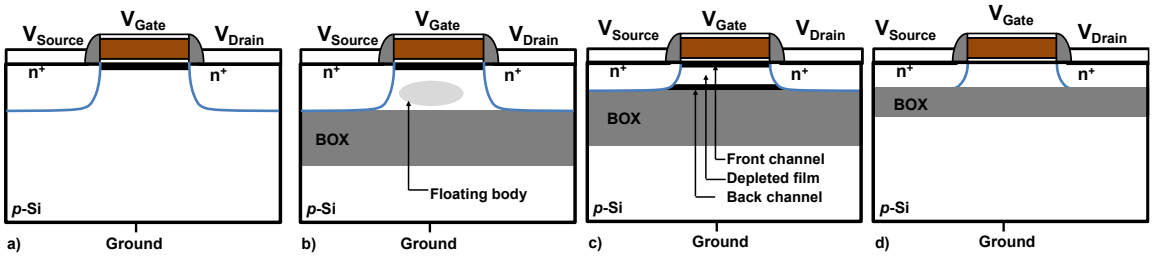


Figure 1. The schematic shows the MOSFET device evolution from a) Bulk silicon wafer, b) Thick buried oxide (BOX) and thick silicon, identified as partially depleted silicon-on-insulator (PD-SOI), c) thick buried oxide and thin silicon and d) thin buried oxide and thin silicon (UTBB).

For small scale transistor, SOI MOSFET has been one of the most popular options that it provides much better performance compared to bulk MOSFET, particularly in thin-body and thin buried oxide architecture (see Fig. 1 d)). Basically, the SOI MOSFET offers lower leakage current and junction capacitance, better subthreshold characteristics, and provides better gate control over the device. However, in thick channel SOI MOSFET as in Fig. 1(b), floating body occurs when large drain voltage is applied, where the SOI device in this case is called PD (Partially-Depleted) SOI device. As large drain voltage is applied, impact ionization may occur and generate electron-hole pair. The electron will swipe to the drain terminal, but the hole will accumulate right above BOX layer. It takes time to be discharged through source due potential barrier at the source-to-channel junction. The floating body will yield parasitic effects such as lowering drain breakdown voltage, abnormal subthreshold characteristics, and current instability during switching operating, kink effect, history effect, and negative conductance. There are two ways to solve floating body effects [1]. One of the methods is to provide body contact. However, this results in area penalization. Another way is by using some engineering techniques at drain or source, such as forming a recombination center at source/drain junction using argon ion implantation, bipolar embedded source structure by using formation of Si^+ implantation, and narrowing the bandgap of source region by using Ge ion implantation [2]. However, using these techniques does not solve the floating body effects in the p-MOSFET effectively, and it may cause the drain breakdown voltage to become even worse. Therefore, reducing the channel depth will help to solve the floating body, and this will shift the PD SOI to FD SOI. The FD SOI MOSFET will be free from the kink effect because the hole carrier can penetrate to the source region much easier than thick channel SOI MOSFET.

In this work, we explore interesting device architecture, which can only be achieved with thin body SOI MOSFETs, to mimicking double gate device architecture, for feasible implementation of double gate architecture.

2. SIMULATED DEVICE

Figure 2 illustrates the two-dimensional cross-section silicon-on-insulator wafer with 10 nm thickness for both silicon body and buried oxide. The designed structure is then simulated using

numerical TCAD software simulation. The models that had been included in these simulations were Auger recombination and Shockley-Read-Hall recombination models. For mobility models we choose parallel electric field dependence, Shirahata and Klaassen surface mobility models. The bandgap narrowing is included for carrier statistics models. In addition, the numerical solution technique such as basic drift diffusion calculations has been used throughout these simulations [3].

In this work, we vary the channel length, and the other parameters are remained the same. The channel length is set at 10 nm, 100 nm and 200 nm. The source and drain are an n-type, doped with 1×10^{20} cm^{-3}, while the channel is undoped (doped at 6.5×10^{-14} cm^{-3}) and the substrate is nearly to the channel, is doped at 1×10^{-15} cm^{-3}. The drain voltage is set at low drain voltage, i.e. 50 mV and 1.0 V at high drain voltage. The gate voltages were swept simultaneously from 0 to 1.5 V with 10 mV steps.

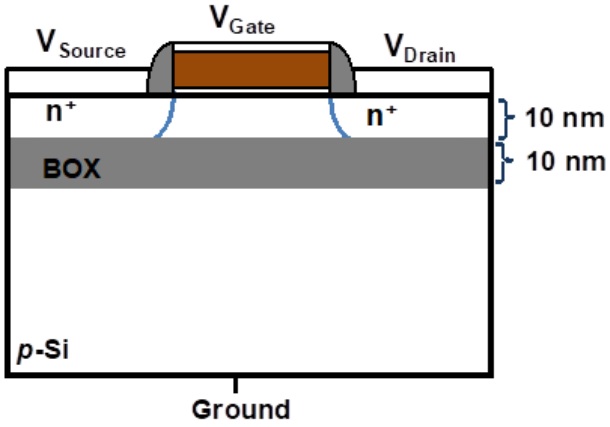


Figure 2. Simulated structure with 10 nm of silicon body and 10 nm thickness of buried oxide.

For the extraction method, the threshold voltage is extracted by using second derivative method [4]. The second-derivate method is determined from the gate voltage at which the rate of transconductance change ($(dg_m/dV_g = d^2I_d/dV_g^2)$ is maximum. The method is considered to be insensitive to doping profiles [5] and relatively insensitive to mobility degradation, series resistance and hot carrier effects [4]. However, the method has limitation for advanced MOSFETs (particularly with thin gate oxide and thin silicon body) device which will be discussed next. Another figure of merit is Drain-Induced Barrier Lowering (DIBL). The DIBL is extracted as the shift of V_g with V_d (DIBL = $\Delta V_g/\Delta V_d$) at constant normalized drain current (i.e. $I_{d\_norm} = I_d/(W/L)$. The method appears the most usually used due to simplicity. Alternatively DIBL can be defined as a V_{Th} shift due to the variation in drain voltage ($\Delta V_{Th}/\Delta V_d$), similarly as shown in Eq. 1 [6].

$$\text{DIBL} = \frac{dV_{Th}}{dV_d} = \frac{V_{Th\ (saturation)} - V_{Th\ (linear)}}{V_{drain\ (saturation)} - V_{drain\ (linear)}}\ mV/V \quad (1)$$

For the third interest of figures-of-merit is subthreshold slope (SS). Basically, for weak inversion, the drain current depends exponentially on gate and drain voltages. By taking the slope of the straight line at this regime based on $dV_g/d\log(I_d)$ (hence the inverse of $d\log(I_d)/dV_g$), the sharpness of the current transition from off-state to on-state can be determined. Lower value of the subthreshold slope implies more efficient and rapid switching of the devices. It is defined as the change in gate voltage required to produce a decade change in drain current and given by Eq. 2.

$$S = \frac{dV_g}{d\log(I_d)} \quad (2)$$

For interface traps and capacitive coupling at the front interface and depletion region, the expression of the subthreshold slope which accounts can be written as in Eq. 3.

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{dep}+C_{it}}{C_{ox}}\right) = n.\frac{kT}{q}\ln(10) \quad (3)$$

where C_{it} is the top interface trap capacitance, C_{dep} is the depletion capacitance, C_{ox} is the oxide capacitance and n is the body factor. The body factor is an image of the coupling efficiency between the front-gate voltage and the channel [7]. The closer n is to unity, the sharper the transition between the off- and on-states of the transistor.

3. RESULTS AND DISCUSSION

Figure 3 depicts the drain current versus gate voltage characteristics for a gate length of 100 nm. The devices were measured at two drain voltages, namely 50 mV and 1.0 V, while the back gate was set at -2.0 V, 0 V, and +2.0 V. As evident from the figure, excellent current-voltage characteristics are observed at V_{bg} = -2.0 V and 0.0 V. However, at a positive voltage of V_{bg} = 2.0 V, the characteristics exhibit a deviation with a significantly high off-drain current. These observations hold true for both low (V_d = 50 mV) and high drain (V_d = 1.0 V) biases. Similar trends are noticed for a gate length of 200 nm, except that in the long-channel devices, the drain current is slightly lower compared to short-channel devices.

Figures 3(b) and 3(c) display the electron concentration distribution in the channel for V_{bg} = -2.0 V and V_{bg} = +2.0 V, respectively. At V_{bg} = -2.0 V, the electron concentration is concentrated near the gate interface, signifying that the gate maintains full control over the channel. Additionally, this also implying that only front channel is formed. In contrast, at V_{bg} = 2.0 V, the electron concentration is spread throughout the channel in a rectangular fashion; with clearly show the formation of front channel and back channel. This indicates that at this V_{bg}, the gate loses control over the channel due to the influence of the back gate voltage. These observations manifest in distinct current-voltage characteristics, where V_{bg} = -2.0 V yields superior characteristics owing to better channel control by the gate itself.

Figure 4 depicts the threshold voltage, extracted by using double derivate method at three different back gate voltages, i.e. V_{bg} = -2.0 V, 0.0 V and + 2.0 V at L_{ch}=100 nm and V_d=50 mV. It shows that the V_{th} for V_{bg}=2 V is the lowest, i.e. 0.3 V, and as the V_{bg} transits from negative bias to positive, the V_{th} increases. The trend shown is in agreement with previously reported [8]. This is because of the positive V_{bg} has better confinement of subthreshold carrier due to coupling effect from the back gate [9]. A back gate channel will be formed right above the BOX / substrate interface in the channel ^{13}, which it is proved from the electron current density extracted as shown in Figure 3 (c), with the exists the back gate channel right above the BOX / substrate interface layer.

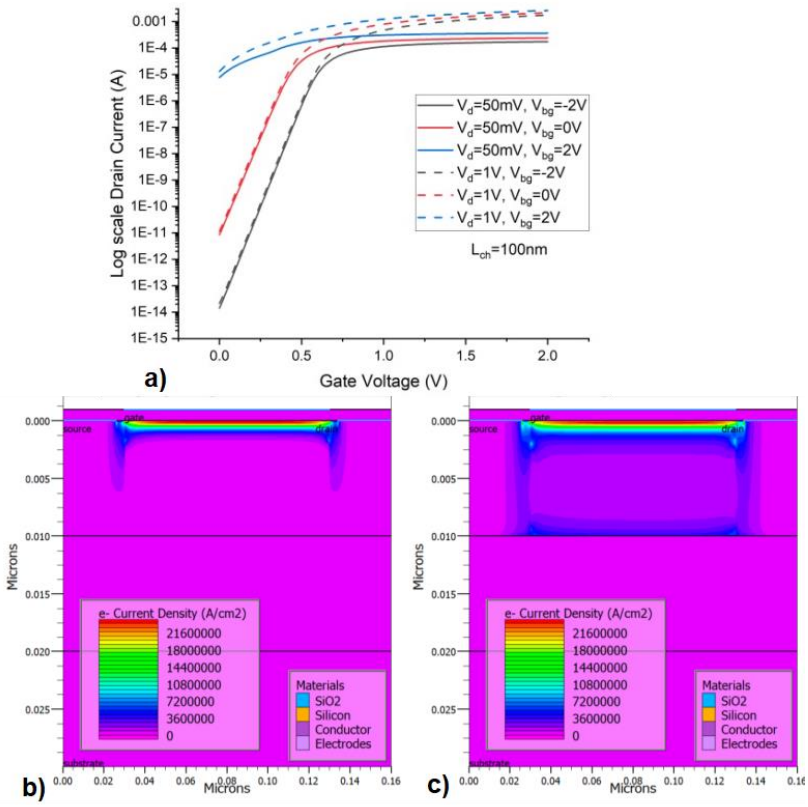


Figure 3. (a) Current – voltage characteristics for V_{bg} at -2.0 V, 0 V and +2.0 V. The drain voltage is biased at V_d = 50 mV and 1.0 V and Lg = 100 nm, electron current density distribution in the channel at (b) V_{bg} = -2.0 V and (c) V_{bg} = +2.0 V.

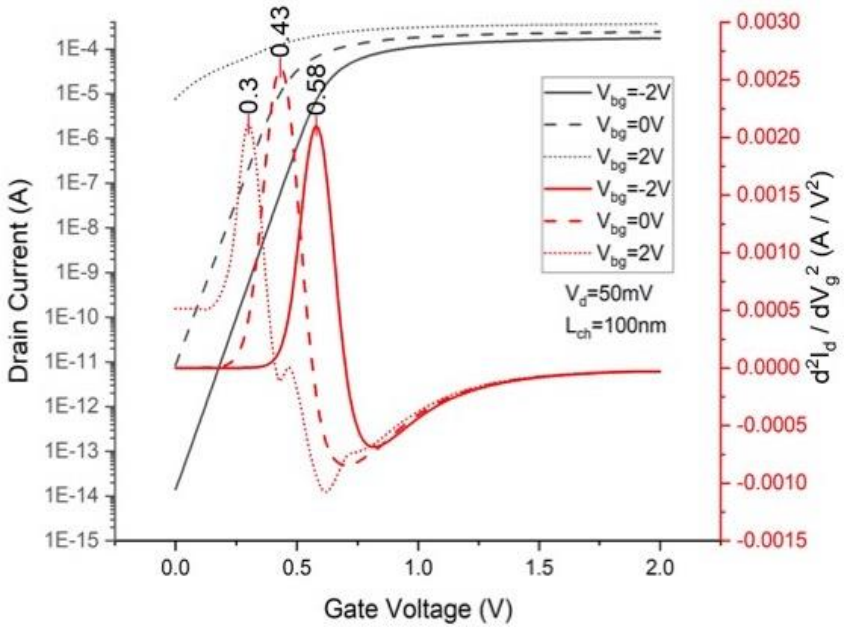
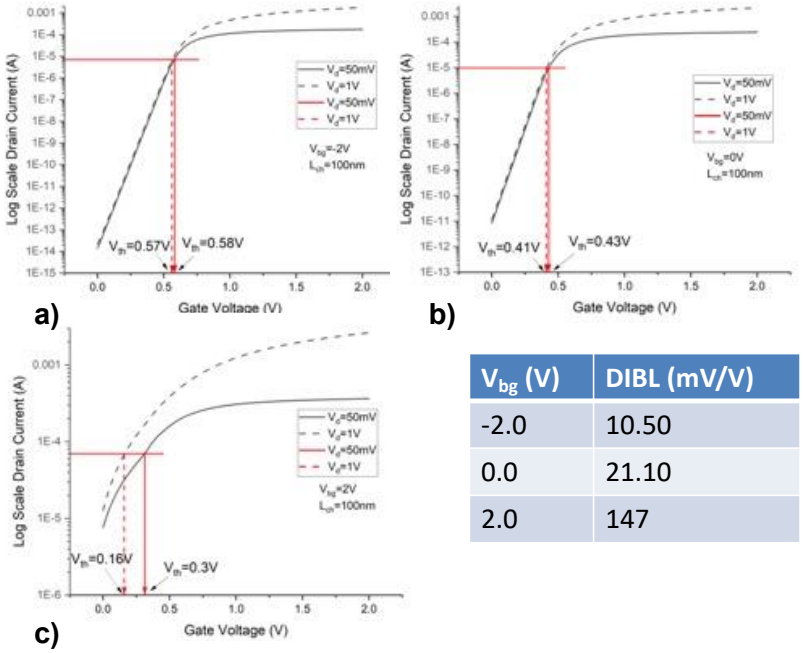


Figure 4. Threshold voltage extracted from double derivatives method for L_{ch}=100 nm at three different back-gate voltages, i.e. V_{bg} = 0 V, V_{bg} = -2 V, and V_{bg}=2 V.

Next, we look in Drain-Induced Barrier Lowering (DIBL). DIBL is extracted at two different drain voltages (V_d = 50 mV and V_d = 1.0 V). With this extraction we can determine the severity of short-channel effect, in relation to effect of threshold voltage of the transistor at low and high drain voltages. Basically, in long channel, the channel formation occurs far enough from drain voltage, thus the channel is independent from drain voltage. In short channel, this is no longer true since the drain is close enough to the gate and channel, thus high drain voltage can give impact to the channel, thus impact the performance. We observed, the impact is more significant in bigger diameter as compared to smaller diameter nanowires. Figure 5 shows that as the V_{bg} transits from negative bias to positive, the DIBL value increases. This can be explained by reducing negative bias of V_{bg} or even increasing positive V_{bg} will pull some carriers away from the top channel which reduce the confinement of the carriers in the channel [10], thus forming the second channel as previously explained in Figure 3 (c). Additionally, we also observed that the potential increases at low V_d and high V_d near the drain at V_{bg} = -2.0 V is less significant as compared at V_{bg} = 2.0 V. Another thing that need to be highlighted, we observed slight DIBL differences between 100 nm and 200 nm, especially at V_{bg} = 0 V. This might be due the channel length different is not significant, which result no significant change of potential at both channel at low and high drain biases.



V_{bg} (V)	DIBL (mV/V)
-2.0	10.50
0.0	21.10
2.0	147

Figure 5. I_d-V_g characteristics for DIBL extraction at low and high drain biases for a) V_{bg} = -2.0 V, b) V_{bg} = 0.0 V and c) V_{bg} = 2.0 V for L_g = 100 nm. The inset table shows the extracted DIBL.

Table 1 shows the trend of SS at different V_{bg} bias, extracted from I_d versus V_g curve at V_d = 50 mV. The SS value increased significantly as V_{bg} moves from negative bias to positive, reflecting that the switching speed at negative V_{bg} is the fastest and vice versa for positive V_{bg}. As previously explained, at positive V_{bg} more carriers will be push to the the BOX / substrate interface, which forming another channel at this area, thus increase of channel potential changes capacitance between of channel-to-source and channel-to-drain junction. In term of channel length, we do observe that generally the performance of SS at shorter L_{ch} is worse than longer L_{ch} for every V_{bg}, with similar reason, capacitance increase with shorter channel length due to increase of depletion region.

Table 1. Extraction of SS at different V_{bg} for Lg = 100 nm and V_d = 50 mV

V_{bg}	SS
-2.0 V	65.00
0.0 V	68.30
2.0 V	320.00

4. CONCLUSION

The simulation was conducted using 2D Device Simulation software, with a focus on the performance of Vth, DIBL, and SS under different V_{bg} conditions: -2.0 V, 0.0 V, and 2.0 V. Optimal performance is attained under negative V_{bg} bias, where the channel forms exclusively at the front channel region. Conversely, under positive V_{bg} bias, electron carriers are drawn towards the back gate, giving rise to a conductive back channel and leading to an additional channel formation near the BOX/substrate interface. This phenomenon contributes to the deterioration of DIBL and SS under this bias condition. Another intriguing aspect of back-gate biasing voltage is its capacity to enable the adjustment of the threshold voltage based on specific applications.

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