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Taguchi Method Statistical Analysis on Characterization and Optimization of 18-nm Double Gate MOSFETs

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ABSTRACT

A bi-layer graphene with a multigate structure was intensified and analysed on an 18-nm Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) device to obtain an optimal performance parameter. The device has a gate structure made of Titanium Dioxide (TiO_2) that serves as a high-k material and a metal gate made of Tungsten Silicide (WSi_x). The Silvaco TCAD Software which are ATHENA and ATLAS modules were used to enhance the fabrication process of virtual devices and to verify the electrical properties of a specific device. According to the International Technology Roadmap Semiconductor (ITRS) specifications of 0.179 V ± 12.7% for threshold voltage (V_{TH}) and 20 nA/m for leakage current (I_{LEAK}), the Taguchi L9 orthogonal array strategy was used to improve the device process parameters for optimum V_{TH} and I_{LEAK}. For the NMOS device, the process parameter of V_{TH} Adjust Implant Dose was used as the dominant factor while Source/Drain (S/D) Implant Energy was used as the adjustment factor whereby for PMOS device, S/D Implant Energy was the dominant factor while S/D Implant Tilt was the adjustment factor in order to achieve a robust design through the Taguchi method implementation. The percentage affecting the process parameter is then applied to the results of the signal to noise ratio (SNR) of Nominal-the-best (NTB) for V_{TH} and Smaller-the-better (STB) for I_{LEAK}.

Keywords: *Bilayer Graphene, Double gate-MOSFET, High-K/Metal gate, TCAD*

1. INTRODUCTION

In this paper, an introduction on the bi-layer graphene metal-oxide-semiconductor field-effect transistor (MOSFET) device with double gate along with the previous transistor invention is discussed. Initially, the traditional transistor using Silicon Dioxide (SiO_2) and downsizing the transistors' dimension needs the reduction in the dielectric thickness [1]. Using SiO_2 to fabricate the nanoscale device makes it impossible as high current leakage occurs. Followed by the high-k/polysilicon transistor which enhanced the device through the increase of gate field effect, and allowed the usage of a thicker dielectric layer in order to reduce gate leakage but eventually when the device is shrunk, poly depletion occurred [2]. Thus, graphene with high-k metal gate transistor was preferred as it has a low resistance loss and heat dissipation, while the significant performance of the device increased with a source-drain and gate oxide leakage reduction [3]. Hence, a smaller gate length such as 18 nm could be produced.

The MOSFET is designed to regulate voltage and current flow from the source to the drain. It almost functions like a switch. Furthermore, MOS capacitor determines the functionality of the MOSFET. The most important section of the MOSFET is the MOS capacitor. It is the surface of the semiconductor among the source and the drain terminal on the lower oxide layer, where the current flow is controlled. Besides, it can be inverted from p-type to n-type by using whether a positive gate voltage or a negative gate voltage.

The drain and source regions are highly doped n+, while the substrate is p-type. The flow of current through the negative electron MOSFET is referred to as the n-channel MOSFET. The p-type device body and the terminal source are both connected to the same ground. A positive polarity voltage is delivered to the terminal gate, resulting a capacitor effect. The minority carriers, which are free electrons, are then drawn and move toward terminal gate in the p substrate. As a result, a layer of uncovered ions forms beneath the dielectric layer, in which the combinations of holes and electrons occur. As the applied positive voltage rises and crosses the minimum threshold, electrons, as minority carriers, can eliminate recombination with holes and form a channel between two p-type materials [4].

A p-channel MOSFET is formed when one delicately doped n-type substrate is joined to two heavily doped p-type materials. Whenever a negative (-) voltage is supplied to the MOSFET's gate terminal, charge carriers such as electrons that are accessible below the oxide layer are pressured downward into the substrate. As a result, the depletion region occupied by the holes is linked to the

donor atoms. As a result, the negative (-) gate voltage will attract holes from the drain and p+ source regions into the channel region [5].

The hot-electron effect has a greatly limited MOSFET innovation progress, especially complementary metal-oxide semiconductor (CMOS). To create smaller devices and to enlarge the integration of the chip level, from a very beginning, advanced lithographic and process techniques have been utilized. In 1963, the CMOS system was declared to guarantee irrelevant dissipation of power. As a result, when the concept of MOSFET scaling was introduced, the potential outcome of minimal power dissipation of MOSFET circuits that are both easy to make and scalable appeared very viable [6].

In the history of transistor innovation, SiO_2 has been used for a decade as the effective dielectric gate material. Various high-k dielectric material has established recently to replace a thinner SiO_2 dielectric layer in order to solve leakage current issue. TiO_2, HfO_2, ZrO_2, and Al_2O_3 are examples of high-k that are being studied [5]. Most researchers used TiO_2 as a dielectric gate for upcoming applications of CMOS. On other hand, a high-k dielectric permittivity has excellent electrical characteristics and thermal stability such as the material based on Hafnium. It will be very helpful in finding the low current leakage. To be more specific, that is the main reason why TiO_2 has been determined and recognized as the best candidate stated in [7]. To eradicate the depletion of Poly-Si, the high-k dielectric is coupled with the metal gate. Furthermore, identifying a metal gate substance for the counterpart work purpose and process integration in conjunction with a high-k dielectric material is vital for better productivity [8].

Statistical variations in fabrication process parameters have historically influenced semiconductor technology scaling and will continue to do so in the future. Notable process variations, such as those associated with implants, anneals, pocket implants, and tiling angles, significantly impact future technology scaling [9]. The Taguchi method is employed to optimize multiple process parameters efficiently, using fewer experiments. This method utilizes orthogonal arrays to study process parameter variability with a reduced experimental workload. By incorporating noise factors known as the signal-to-noise ratio (SNR), the Taguchi method enhances the reliability of process parameter variability studies. Additionally, analysis of variance (ANOVA) is performed to determine the most significant process parameters. The combination of SNR and ANOVA analyses allows for excellent prediction of the optimal process parameters for PMOS devices [10].

Currently, the threshold voltage (V_{TH}) is widely recognized as a crucial parameter affecting device power consumption. This parameter is known to vary due to semiconductor process variability, significantly impacting device performance [11].

Accurately estimating variability in the process parameters of scaled devices is essential for designing optimal nanoscale transistors with minimal leakage current (I_{LEAK}). Various leakage mechanisms contribute to the total leakage current in a device, depending on factors such as gate length (Lg), oxide thickness (Tox) and doping profile [12].

2. PROCESS AND DEVICE STRUCTURE

2.1. Fabrication Process

ATHENA was utilized to virtually fabricate an 18-nm bilayer graphene device with a high-k/metal gate as well as multigate NMOS and PMOS devices, while ATLAS was used to measure electrical properties. The fabrication leads to a series of the same regular top-down transistor well-matched procedure as before, with the exception of a few process parameters in doping density and annealing temperature, to achieve the standard by International Technology Roadmap for Semiconductors (ITRS) expectations outcome.

In addition, the process and device simulations of multigate MOSFET used ATHENA and ATLAS modules of the SILVACO TCAD tool respectively. The substrate is prepared similarly in this procedure. The multigate MOSFET device process simulation requires a sequence of processing steps known as a process flow. Table 1 and Table 2 show the main process step and their parameters in order to design the NMOS and PMOS, respectively.

Table 1. Fabrication steps of NMOS

Process Step	Parameters
p-type Silicon	<100> orientation, Boron
Threshold Voltage Implantation	7.08 x 10^{13} atom/cm^2
Bilayer Graphene deposition	Thickness = 0.001 µm
High-k deposition	Thickness = 0.003 µm of TiO_2
Metal Gate Deposition	18nm length, 0.15 µm thickness
S/D implantation	1.27x10^{18} atoms/cm^2 Arsenic
Aluminium Depostition	Thickness = 0.01 µm

Table 2. Fabrication steps of PMOS

Process Step	Parameters
n-type Silicon	<100> orientation, Arsenic
Threshold Voltage Implantation	0.99 x 10^{11} atom/cm^2
Bilayer Graphene deposition	Thickness = 0.001 µm
High-k deposition	Thickness = 0.003 µm of TiO_2
Metal Gate Deposition	18nm length, 0.15 µm
S/D implantation	4.97 x 10^{18} atoms/cm^2 Boron
Aluminium Depostition	Thickness = 0.001 µm

The fabrication results for MOSFET transistor in Silvaco ATHENA are shown in Figure 1.

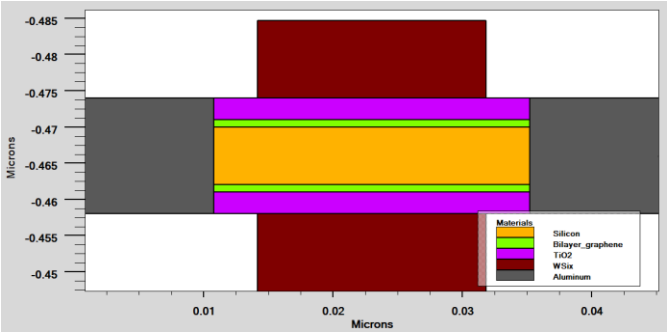

Figure 1. The complete MOSFET virtual transistor

2.2. Taguchi L9 Orthogonal Array Method

After the designed MOSFET was successfully fabricated and simulated, Taguchi method was used to optimize process parameters using an experimental layout of L9 Orthogonal Array [13]. In this study, four control factors and two noise factors were selected on the basis of previous papers. The factor for V_{TH} and I_{LEAK} has been quenched as the most convincing parameters. Table 3 displays the values of the varying levels of process parameters for NMOS. Followed by, two noise factors were examined, as indicated. Table 4 displays the values of the varying levels of process parameters for PMOS along with two noise factors that were examined, as indicated.

Table 3. Process parameter and noise factor for NMOS

Factor	Process Parameter	Unit	Level 1	Level 2	Level 3
A	V_{TH} Adjust Implant Dose ($\times 10^{13}$)	Atom/cm^3	7.08	7.13	7.18
B	S/D Implant Dose ($\times 10^{18}$)	Atom/cm^3	1.17	1.22	1.27
C	S/D Implant Energy	keV	1	3	5
D	S/D Implant Tilt	degree	68	70	72
	Noise Factor	**Unit**	**Level 1**	**Level 2**	
X	V_{TH} Adjust Implant Energy	keV	20	22	
Y	V_{TH} Adjust Implant Tilt	degree	10	12	

Table 4. Process parameters and noise factor for PMOS

Factor	Process Parameter	Unit	Level 1	Level 2	Level 3
A	V_{TH} Adjust Implant Dose ($\times 10^{11}$)	Atom/cm^3	0.94	0.99	1.04
B	S/D Implant Dose ($\times 10^{14}$)	Atom/cm^3	4.97	5.02	5.07
C	S/D Implant Energy	keV	4	6	8
D	S/D Implant Tilt	degree	23	25	27
	Noise Factor	**Unit**	**Level 1**	**Level 2**	
X	V_{TH} Adjust Implant Energy	keV	35	37	
Y	V_{TH} Adjust Implant Tilt	degree	9	11	

3. RESULTS AND DISCUSSION

3.1. Simulation of Electrical Characteristics

Figure 2 portrays the designed NMOS device's I_{DS}-V_{DS} characteristics while Figure 3 portrays the NMOS devices I_{DS}-V_{GS} characteristics. If the voltage of the gate (V_{GS}) is lesser than the V_{TH}, the drain leakage current (I_{LEAK}) occurs. Comparably, when the transistor, V_{GS} = 0V and V_{DS} = V_{DD} (voltage supply) is turned off, there will be no current in the channel (I_{LEAK}). Figure 4 portrays the designed PMOS device's I_{DS}-V_{DS} characteristics while Figure 5 portrays the PMOS devices I_{DS}-V_{GS} characteristics.

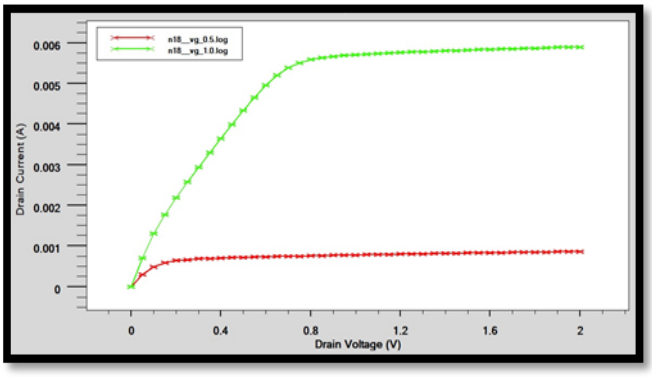

Figure 2. I_{DS} – V_{DS} characteristics of the NMOS device

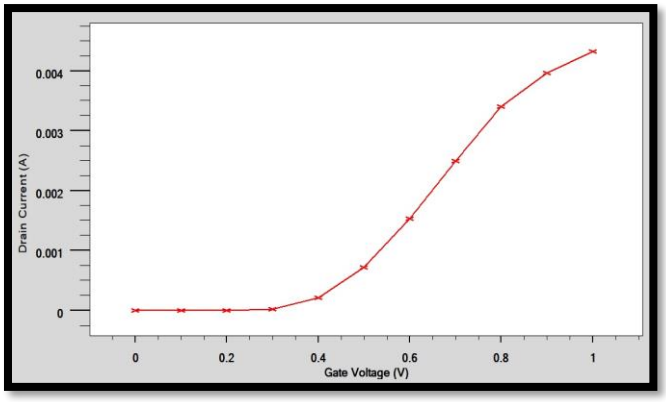

Figure 3. I_{DS} – V_{GS} characteristics of the NMOS device.

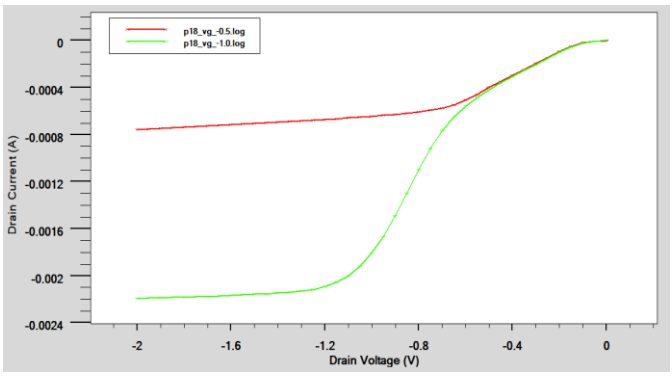

Figure 4. I_{DS} – V_{DS} characteristics of the PMOS device.

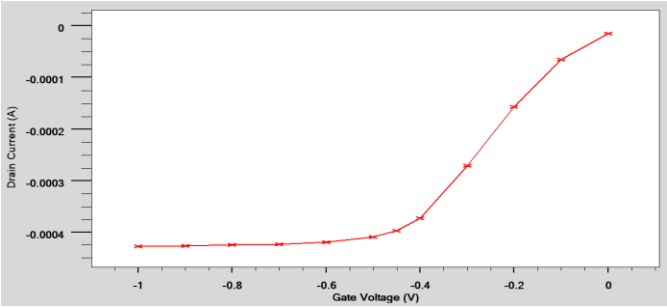

Figure 5. I_{DS} – V_{GS} characteristics of the PMOS device.

The linear increase in I_{DS} with V_{DS} is due to the field-effect within the channel. As V_{DS} increases, the electric field along the channel increases, leading to more carriers being swept towards the drain, thus increasing I_{DS} linearly. In saturation, the channel is pinched off near the drain end, creating a constant current path from drain to source. V_{DS} does not significantly affect I_{DS} because the channel is fully conductive regardless of the drain-source voltage. At lower V_{GS}, the channel is only partially inverted, leading to a smaller number of carriers contributing to current flow. Hence, I_{DS} increases exponentially as more carriers are induced by increasing V_{GS}. As V_{GS} increases beyond V_{TH}, the channel becomes fully inverted, and additional carriers do not contribute significantly to I_{DS}. Therefore, I_{DS} saturates and remains relatively constant. For PMOS, at higher V_{GS}, the channel is only partially inverted, leading to a smaller number of carriers contributing to current flow. Hence, I_{DS} decreases exponentially as fewer carriers are available for conduction.

3.2. Optimization Using Taguchi L9

For the L9 Taguchi orthogonal array analysis, 36 simulations were constructed with four parameters and two noise factors at various levels. The process parameters used as the control factors are V_{TH} adjust implant dose (Factor A), source/drain (S/D) implant dose (Factor B), S/D implantation energy (Factor C) and S/D implant tilt (Factor D). Followed by V_{TH} adjust implant energy (Factor X) and V_{TH} adjust implant tilt (Factor Y) as the noise factors. The process parameters were simulated according to the L9 Orthogonal Array specification using X1, X2, Y1 and Y2 indicated as noise factors respectively. The simulation outputs for V_{TH} and I_{LEAK} are shown in Table 5 and Table 6 for NMOS while Table 7 and 8 for PMOS respectively.

Table 5. Result of V_{TH} (V) for NMOS

Exp. no.	Threshold Voltage (V_{TH})			
	X1Y1	X1Y2	X2Y1	X2Y2
1	-0.537531	-0.545982	-0.472421	-0.479669
2	0.176056	0.177614	0.174974	0.175099
3	-0.153194	-0.153079	-0.154091	-0.153988
4	0.180204	0.180334	0.179168	0.176599
5	-0.124495	-0.12438	-0.125379	-0.125276
6	-0.607044	-0.615604	-0.551454	-0.548507
7	-0.115836	-0.031521	-0.116734	-0.11663
8	-0.644586	-0.303685	-0.588583	-0.595986
9	0.164321	0.176075	0.174824	0.174952

Table 6. Result of I_{LEAK} (nA/μm) for NMOS

Exp. no.	Leakage Current (I_{LEAK})			
	X1Y1	X1Y2	X2Y1	X2Y2
1	30.0058	29.977	30.2457	30.2172
2	796.565	306.272	924.924	909.225
3	0.007490	0.007488	0.007513	0.007511
4	57.8522	57.0378e	64.8964	331.985
5	0.00668	0.006677	0.006702	0.0067
6	29.8334	29.8073	30.0222	30.0235
7	0.006442	0.004197	0.006465	0.006463
8	29.748	29.7011	29.9287	29.905
9	11915	924.879	1095.39	1076.74

Table 7. Result of V_{TH} (V) for PMOS

Exp. no.	Threshold Voltage (V_{TH})			
	X1Y1	X1Y2	X2Y1	X2Y2
1	-0.096106	-0.094792	-0.104943	-0.103248
2	0.157261	0.157259	0.157269	0.157268
3	0.080370	0.080032	0.080035	0.080372
4	0.167354	0.167355	0.16735	0.167351
5	-8.666667	-8.24773	-8.24851	-8.2484
6	-0.092925	-0.0917232	-0.100977	-0.099437
7	0.071069	0.071068	0.071077	0.071075
8	-0.090152	-0.089046	-0.097540	-0.096131
9	0.142726	0.140238	0.142738	0.142736

Table 8. Result of I_{LEAK} (nA/μm) for PMOS

Exp. no.	Leakage Current (I_{LEAK})			
	X1Y1	X1Y2	X2Y1	X2Y2
1	36.61	36.5984	36.679	36.6669
2	20.4543	20.4544	20.454	20.4541
3	24.3607	24.3958	24.3955	24.3605
4	19.9837	19.9838	19.9835	19.9835
5	23.4808	23.4808	23.4806	23.4806
6	36.5812	36.5697	36.6498	36.6378
7	24.9143	24.9144	24.914	24.914
8	36.554	36.5425	36.6222	36.6102
9	20.8959	20.9715	20.8955	20.8956

The 36 analyses are used to identify the dominant factor and adjustment factor. The dominant factor and adjustment factor are two attributes that ought to be studied for the SNR of NTB analysis. The factor with the highest percentage of SNR of NTB is claimed to be the dominant factor, which contributes significantly to the yield reaction.

The other factor to be assessed is the adjustment factor with the lowest percentage of factor effect on SNR of NTB but the highest percentage of factor effect SNR (Mean). In a nutshell, the factor which can be balanced until the yield reaches to the nearest targeted value. The NTB characteristic determines the optimum V_{TH} analysis, while the STB characteristic determines minimum I_{LEAK} analysis [14]. Table 9 and Table 10 represent the SNR response for V_{TH} and I_{LEAK} for NMOS device while both Table 11 and 12 are for PMOS device.

Table 9. SNR Response for V_{TH} in NMOS

Factor	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N
		Level 1	Level 2	Level 3	
A	V_{TH} Adjust Implant Dose	38.33	37.40	15.89	**43.83**
B	S/D Implant Dose	23.26	33.86	34.49	
C	S/D Implant Energy	19.16	37.80	34.66	
D	S/D Implant Tilt	33.35	24.82	33.45	

Table 10. SNR Response for I_{LEAK} in NMOS

Factor	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N
		Level 1	Level 2	Level 3	
A	V_{TH} Adjust Implant Dose	105.04	109.72	99.80	**150.47**
B	S/D Implant Dose	110.03	105.40	99.13	
C	S/D Implant Energy	150.47	120.60	43.49	
D	S/D Implant Tilt	99.44	105.72	109.40	

Table 11. SNR Response for V_{TH} in PMOS

Factor	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N
		Level 1	Level 2	Level 3	
A	V_{TH} Adjust Implant Dose	56.05	69.94	50.81	**62.13**
B	S/D Implant Dose	69.10	67.77	39.93	
C	S/D Implant Energy	26.37	76.01	74.42	
D	S/D Implant Tilt	51.18	66.94	58.69	

Table 12. SNR Response for I_{LEAK} in PMOS

Factor	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N
		Level 1	Level 2	Level 3	
A	V_{TH} Adjust Implant Dose	151.59	151.77	151.47	**148.73**
B	S/D Implant Dose	151.59	151.70	151.53	
C	S/D Implant Energy	148.73	153.79	152.31	
D	S/D Implant Tilt	151.63	151.53	151.66	

3.3. Analysis of Variance (ANOVA)

ANOVA is a familiar factual evaluation that is illustrated to acknowledge the contribution rate with each factor. In relation to the table, the dominant factor and adjustment factor can be defined to select the most efficient combination of process parameters. According to the observation in NMOS device, A1 which represents Level 1 value of Factor A the V_{TH} Adjust Implant Dose process parameter, B3 which represents Level 3 value of Factor B the S/D Implant Dose process parameter, C_{sweep} which represents the adjustment factor of Factor C the S/D Implant Energy process parameter and D3 which represents Level 3 value of Factor D the S/D Implant Tilt process parameter are considered the best combination of process parameters while for PMOS device, A2 which represents Level 2 value of Factor A the V_{TH} Adjust Implant Dose process parameter, B1 which represents Level 1 value of Factor B the S/D Implant Dose process parameter, C2 which represents Level 2 value of Factor C the S/D Implant Energy and D_{sweep} which represents the adjustment factor of Factor D the S/D Implant Tilt process parameter are the best process parameter combinations. However, it is essential to attain another analysis to finalize the combination of process parameters in order to evaluate the most effective process of parameter in ANOVA. The percentage of the SNR effect factor reflects the process parameter's tendency to minimize fluctuation [15]. Table 13 and 14 depict the ANOVA results for V_{TH} and I_{LEAK}, respectively for NMOS device whereby Table 15 and Table 16 are the ANOVA results for V_{TH} and I_{LEAK}, respectively for PMOS devices.

Table 13. ANOVA Results for V_{TH} in NMOS

Factor	Process Parameter	Factor Effect	
		NTB (%)	Mean (%)
A	V_{TH} Adjust Implant Dose	50	1
B	S/D Implant Dose	12	1
C	S/D Implant Energy	31	97
D	S/D Implant Tilt	8	1

Table 14. ANOVA Results for I_{LEAK} in NMOS

Factor	Process Parameter	Factor Effect
		STB
A	V_{TH} Adjust Implant Dose	1
B	S/D Implant Dose	1
C	S/D Implant Energy	97
D	S/D Implant Tilt	1

Table 15. ANOVA Results for V_{TH} in PMOS

Factor	Process Parameter	Factor Effect	
		NTB (%)	Mean (%)
A	V_{TH} Adjust Implant Dose	8	30
B	S/D Implant Dose	22	28
C	S/D Implant Energy	65	15
D	S/D Implant Tilt	5	27

Table 16. ANOVA Results for I_{LEAK} in PMOS

Factor	Process Parameter	Factor Effect
		STB
A	V_{TH} Adjust Implant Dose	0
B	S/D Implant Dose	0
C	S/D Implant Energy	99
D	S/D Implant Tilt	0

The factor effect on SNR of NTB results highlights that Factor A is unquestionably the most dominant factor in the V_{TH} as an outcome of the NMOS device, with a highest proportion of 50%, and Factor C is the most dominant factor in the V_{TH} as an outcome of the PMOS device, with the highest proportion of 65%. The adjustment factor for NMOS device is considered as Factor C with the percentage of 31% for NTB and 97% for mean. Meanwhile in PMOS device, the adjustment factor is Factor D with a percentage of 5% for NTB and 27% for mean. The factor with the high percentage value on average and the lowest percentage on the NTB can be recognised. As the adjustment factor for NMOS is the Factor C and for PMOS is the Factor D, the range was diversified until the obtained V_{TH} was closer to the nominal. For NMOS, an optimal value of Factor C by sweeping the value was obtained as 2 keV. While for PMOS, an optimal value of Factor D angle by sweeping the value was obtained as 27°.

For NMOS devices, V_{TH} Adjust Implant Dose directly affects the threshold voltage. This parameter controls the dopant concentration in the channel region, influencing the V_{TH} by shifting the energy barrier at the junction. Higher implant doses increase dopant concentration, reducing the threshold voltage. Lower doses result in higher V_{TH} values. The S/D Implant Energy fine-tunes the characteristics of NMOS devices, including performance metrics like current drive and leakage current. Adjusting implant energy affects the depth and distribution of dopants in the source and drain regions. Higher energy implants can increase dopant diffusion depth, affecting channel conductivity and leakage characteristics.

For PMOS devices, S/D Implant Energy is identified as the dominant factor. This parameter primarily influences characteristics such as V_{TH}, I_{LEAK}, and speed. Higher implant energies can alter the doping profile near the S/D regions, affecting junction characteristics and thus the overall device performance. S/D Implant Tilt is an adjustment factor critical for fine-tuning PMOS device characteristics. Implant tilt angle influences the lateral distribution of dopants under the gate, affecting channel length modulation, V_{TH} roll-off, and overall device performance. Optimizing this parameter ensures consistent and predictable device behavior across manufacturing variations.

3.4. Optimum Combination Factor

The finalized parameter combined effect for obtaining an enhanced V_{TH} value for NMOS devices are A1, B3, C_{sweep}, D3 and for PMOS devices are A2, B1, C2, D_{sweep} according to the combination and analysis. Whereby the combination of parameters for I_{LEAK} of the NMOS device are A2, B1, C1, D3 and of the PMOS device are A2, B3, C1, D1.

Simulation with the noise factor was carried out using the final parameters in order to obtain the optimum result for V_{TH} and I_{LEAK} as shown in Table 17 and Table 18 for NMOS and Table 19 and Table 20 for PMOS.

Followed by the final improvement through the noise factor parameter process.

Table 17. Final NMOS results with added noise of V_{TH} (V)

$V_{TH}1$ (X1, Y1)	$V_{TH}2$ (X1, Y2)	$V_{TH}3$ (X2, Y1)	$V_{TH}4$ (X2, Y2)
0.190402	0.190588	**0.188939**	0.189107

Table 18. Final NMOS results with added noise of I_{LEAK} (nA/μm)

$I_{LEAK}1$ (X1, Y1)	$I_{LEAK}2$ (X1, Y2)	$I_{LEAK}3$(X2, Y1)	$I_{LEAK}4$(X2, Y2)
28.0579	28.0389	**28.2279**	28.2064

Table 19. Final PMOS results with added noise of V_{TH} (V)

$V_{TH}1$ (X1, Y1)	$V_{TH}2$ (X1, Y2)	$V_{TH}3$ (X2, Y1)	$V_{TH}4$ (X2, Y2)
0.167355	**0.167356**	0.167351	0.167352

Table 20. Final PMOS results with added noise of I_{LEAK} (nA/μm)

$I_{LEAK}1$ (X1, Y1)	$I_{LEAK}2$ (X1, Y2)	$I_{LEAK}3$(X2, Y1)	$I_{LEAK}4$(X2, Y2)
19.9838	**19.9838**	19.9835	19.9836

The results achieved for the V_{TH} value are within the ITRS expectation range of 0.179 V ±12.7%. Using the NMOS process combination of A1, B3, C_{sweep}, D3 with X2 and Y1, the value of 0.177553 V which is closer 8.08% to the nominal value was gained. For the PMOS process combination of A2, B1, C2, D_{sweep} with X1 and Y2, the value of 0.167356 V which is 6.51% closer to the nominal was obtained. After final optimization, the lowest I_{LEAK} at noise X2 and Y1 for NMOS is 28.2279 nA/μm and lowest I_{LEAK} at noise X1 and Y2 for PMOS is 20.3736 nA/μm. Table 21 and Table 22 show the comparison values between the non-optimized and optimized value gained for NMOS and PMOS, respectively.

Table 21. NMOS simulation result vs. ITRS prediction

Performance Parameter	ITRS Predictions	Non-Optimized Result	Optimized Result
V_{TH} (V)	0.179 ± 12.7	0.188939	0.177553
I_{LEAK}(A/μm)	20×10^{-12}	29.7298×10^{-9}	28.2279×10^{-9}

Table 22. PMOS simulation result vs. ITRS prediction

Performance Parameter	ITRS Predictions	Non-Optimized Result	Optimized Result
V_{TH} (V)	0.179 ± 12.7	0.159673	0.167356
I_{LEAK}(A/μm)	20×10^{-12}	19.9838×10^{-9}	20.3736×10^{-9}

4. CONCLUSION

In a nutshell, it could be concluded that the V_{TH} and I_{LEAK} value for both the NMOS and PMOS devices has been successfully optimized through the Taguchi method. The four control factors for the L9 Taguchi orthogonal approach are V_{TH} Adjust Implant Dose, S/D Implant Dose, S/D Implant Energy and S/D Implant Tilt. The Taguchi orthogonal method is used because its application strengthens research analysis on the parameter with the greatest impact on device performance and facilitates in the refinement of design reliability. In this study, S/D Implant Energy and S/D Implant Tilt are the dominant and adjustment factors for PMOS, respectively, while V_{TH} Adjust Implant Dose and S/D Implant Energy are the dominant and adjustment factors for NMOS. Last but not least, the V_{TH} and I_{LEAK} outcomes are consistent with the ITRS requirement for high-performance devices.

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