International Journal of Nanoelectronics and Materials
Volume 16 January 2023 [187-194]

Performance Analysis of JL-FinFET with Varied Non-Uniform Doping Concentrations, Fin Height and Fin Width using Device Simulator

M. Hazeem Hariff[1], Noraini Othman[1,2,*], S. N. Sabki[1,2], and Alhan Farhanah Abd Rahim[3]

[1]Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis, Arau, 02600, Perlis, Malaysia
[2]Centre of Excellence for Micro System Technology (MiCTEC), Universiti Malaysia Perlis, Arau, 02600, Perlis, Malaysia
[3]Faculty of Electrical Engineering, Universiti Teknologi MARA, Pulau Pinang Campus

Received 4 Oct 2022, Revised 9 Mar 2023, Accepted 23 March 2023

ABSTRACT

With the growth of the MOSFET technology, the size of the transistor becomes smaller which can lead to Short-Channel Effects (SCEs). In order to address the SCEs, multi-gate transistor such as Fin Field-Effect Transistor (FinFET)has been invented. Meanwhile, it is found that the conventional transistor with junctions also has its drawbacks and limitations due to the decrease in the gate length. The SCEs can occur and affect the overall performance of the device with lower switching times and lower current density. In order to address these limitations, new structure of transistor without junction known as a junctionless (JL) transistor has been proposed. In this work, the impact of uniform versus non-uniform doping concentrations, fin height (H_{fin}) and fin width (W_{fin}) in JL-FinFET were investigated by using Technology Computer Aided Design (TCAD) Tools. It was found that non-uniform doping concentration of 4 $x10^{18}$ cm^{-3} for the source/drain and of 4 $x10^{17}$ cm^{-3} for the channel, together with H_{fin} of 20 nm andW_{fin} of 4 nm provide the best electrical performance of I_{off} = 6.45 $x10^{-17}$ A, I_{on} = 6.14 $x10^{-6}$ A, I_{on}/I_{off} = 9.52 $x10^{10}$ and DIBL = 11 mV/V. The outcome of this research work can be used as a basis to understand JL-FinFET biosensors for medical applications and more complex JL structures.

Keywords: Junctionless Fin Field-Effect Transistor (JL-FinFET), Non-Uniform Doping, Short-Channel Effects

1. INTRODUCTION

According to Moore's Law, the number of transistors will double in every 18 to 24 months. With the growth of the MOSFET technology, the size of the transistor will become smaller (downscaling), which can lead to Short-Channel Effects (SCEs). SCEs arise when the close proximity between the source and the drain causes the gate to lose control of the potential distribution and the flow of current in the channel region. With shorter gate length L_g, the depletion regions of high electric fields associated with the source and drain regions started to interact with each other, causing direct carrier transport between the source and drain. This reduces control of the gate over the channel and in turn, give rise to off-state current (I_{off}), lower threshold voltage (V_{th}) and degradation in the Subthreshold Slope (*SS*) and Drain-Induced Barrier Lowering (*DIBL*).

In order to address the SCEs, multi-gate transistor such as Fin-Field Effect Transistor (FinFET) serves as one of the alternatives. Figure 1a shows an example of a MOSFET, where the current conduction between the source and drain is controlled by a voltage applied to the gate (V_G) terminal. *When a voltage is applied across a MOS structure, it modifies the distribution of charges*

* noraini_othman@unimap.edu.my

(either holes or electrons) *in the semiconductor*. Meanwhile, Figure 1b shows an example of a FinFET structure. In FinFET, the channel is surrounded on three sides by the gate, which allows for greater electrostatic control. The FinFET devices have significantly faster switching times and higher current density than planar CMOS technology. The working principle of a FinFET is similar to that of a conventional MOSFET. Various studies on the impact of FinFET parameters have been carried out. In [1], it was found that *DIBL* reduces with the reduction in fin width whereas in [2], it was found that low leakage current and high I_{on}/I_{off} ratio can be obtained with small W_{fin} and H_{fin}.

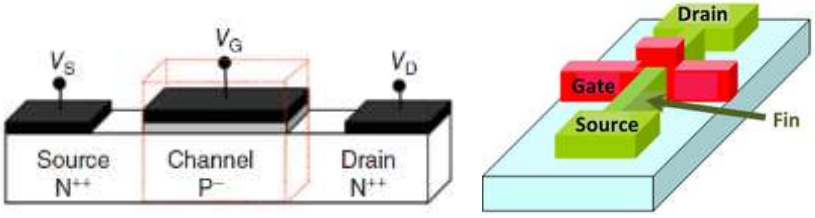

Figure 1. (a) Three-dimensional view of an MOSFET (b) FinFET device

Meanwhile, it is also found that the conventional transistor with junctions also has its drawbacks and limitations due to the decrease in the length of the gate. In order to address these limitations, new structure of transistor which is known as a junctionless FET (JL-FET) has been proposed, where it has a much simpler manufacturing procedures since there are no requirement for doping concentration gradient between the channel and the source/drain region. JL-FET exhibits a near-ideal sub threshold slope, exceptionally low leakage currents, and reducedmobility deterioration with gate voltage and temperature [3][4]. It facilitates the production of transistors smaller than 10 nm. There are two fundamentalprerequisites for making JLTs: the transistor channel must be considerably doped to begin with,and the channel thickness must be in nanoscale. As there are many factors that affect the performance of a JL-FET, this work embarks on studying the impact of various parameters such as the doping concentrations, fin height, H_{fin} and fin width, W_{fin} on the performance of a JL-FinFET.

2. METHODS

In this work, ATLAS 3D was being used to simulate the semiconductor device structure. In order to validate the simulations being carried out in this work, an initial simulation was first performed by referring to [5]. Some of the physical models being used include the Band Gap Narrowing (bgn) model, the Shockley-Read-Hall recombination model (srh) using fixed lifetimes and Auger recombination model (auger) for carrier concentration dependent. The Lombardi (cvt) model for the inversion layer and the ballistic mobility model for a physical gate length smaller than 10 nm were also employed in this simulation. The result of the validation can be seen in Figure 2 where the results of the off-state current, I_{off} and the on-state current, I_{on} obtained were found to be comparable with the results obtained in [5].

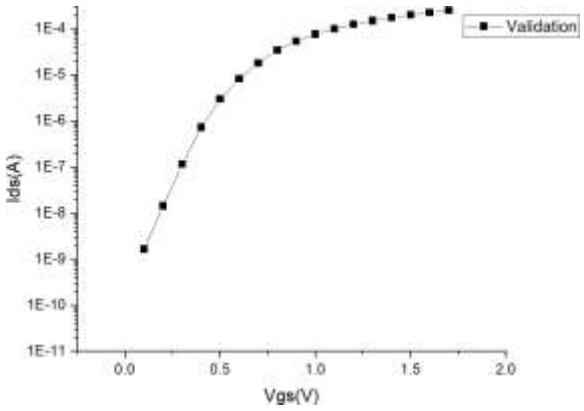

Figure 2. Plot of log I_d-V_g obtained from the initial validation simulations.

Upon successful completion of the validation simulations, the work proceeded to study the impact of doping concentrations, fin height (H_{fin}) and fin width (W_{fin}) on the JL-FET. Parameters used in the simulations are shown in Table 1. For the doping simulations, firstly the uniform vs non-uniform doping was studied. For uniform doping, the source, drain and channel have identical doping concentrations of 4 x10^{18} cm^{-3}, whereas for non-uniform doping simulations, the channel concentration is set to 4 x10^{17} cm^{-3}. Meanwhile, the variations in H_{fin} are of 20 nm, 30 nm and 40 nm whereas the variations in W_{fin} are of 4 nm, 8 nm and 12 nm respectively. Figure 3 shows the simulated structure used in the simulations with the corresponding H_{fin} and W_{fin}. The basis of choosing the device physical parameters in this work are based on parameters adopted in other research work [6][7].

Table 1 Parameters used in the simulations

Parameters	Values
Gate length, L_g	10 nm
Gate oxide thickness, T_{ox}	0.6 nm
Source/drain doping, $N_{S/D}$	4 x 10^{18} cm^{-3}
Fin height, H_{fin}	20 nm (initial), 30 nm, 40 nm
Fin width, W_{fin}	4 nm (initial), 8 nm, 12 nm

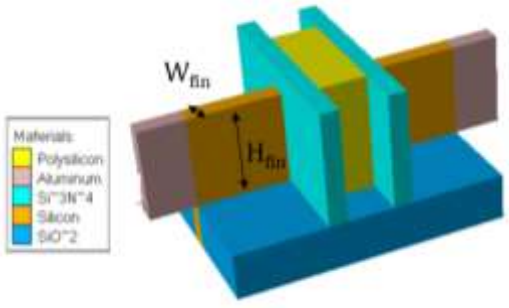

Figure 3. Simulated JL-FinFET structure.

3. RESULTS AND DISCUSSION

3.1 Results for Uniform vs Non-uniform Doping

Figure 4 shows the results of I_d-V_g for uniform vs non-uniform doping concentrations. It can be seen that the non-uniform doping concentration shows a slightly lower off-state leakage current, I_{off} of of 6.45×10^{-17} A as compared to uniform doping concentration of 1.2×10^{-16} A. This is in agreement with [8] where it was found that non-uniform doping JL-FinFET has better control on the SCEs as compared to uniform doping JL-FinFET. This is because, as the doping concentration in the channel in non-uniform doping is low, the depletion of electrons in the fin during the OFF state is greater than in any other doping configurations. From the results obtained, further simulations which focus on the impact of different configurations of non-uniform doping concentrations only were continued.

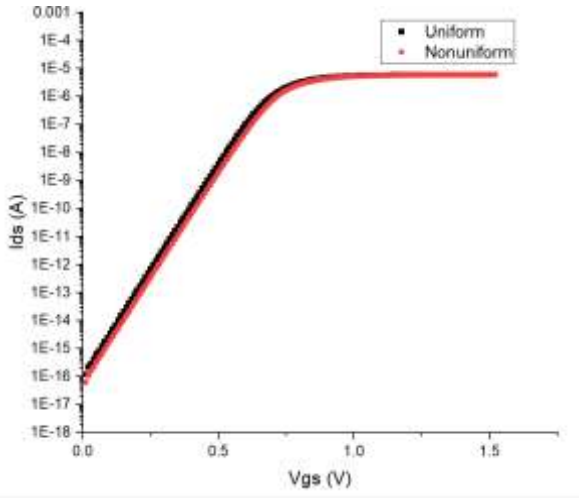

Figure 4. Plot of log I_d-V_g for transistors with uniform vs non-uniform doping concentrations.

3.2 Results for Various Configurations of Non-uniform Doping Concentrations

Various configurations of non-uniform doping concentrations as shown in Table 2 were simulated, where the source and drain concentrations were set to be identical while the channel doping concentration was varied. Results obtained were tabulated in Table 3 while the corresponding plot of log I_d-V_g obtained were shown in Figure 5.

Table 2 Different configurations used in the simulations of non-uniform doping concentrations

Structure	Source	Drain	Channel
A	4×10^{19} cm^{-3}	4×10^{19} cm^{-3}	4×10^{17} cm^{-3}
B	4×10^{18} cm^{-3}	4×10^{18} cm^{-3}	4×10^{17} cm^{-3}
C	4×10^{19} cm^{-3}	4×10^{19} cm^{-3}	4×10^{18} cm^{-3}
D	4×10^{19} cm^{-3}	4×10^{19} cm^{-3}	4×10^{19} cm^{-3}

Table 3 Results obtained for different configurations of non-uniform doping concentrations of JL-FinFET

Parameters	Structure A	Structure B	Structure C	Structure D
I_{on} (A)	3.92 x 10^{-5} A	6.14 x 10^{-6} A	5.11 x 10^{-5} A	6.16 x 10^{-6} A
I_{off} (A)	3.36 x 10^{-14} A	6.45 x 10-^{17} A	5.05 x 10^{-14} A	6.52 x 10^{-14} A
I_{on}/I_{off}	1.17 x 10^{9}	9.52 x 10^{10}	1.01 x 10^{9}	9.45 x 10^{7}
DIBL (mV/V)	63	11	53	21

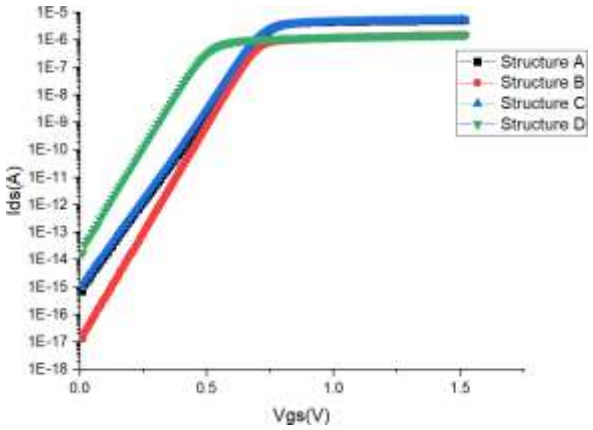

Figure 5. Plot of log I_d-V_g for different configurations of non-uniform doping in saturation mode at V_d=1 V.

From Table 3, it can be seen that Structure B clearly outperforms the others, with thelowest leakage current, I_{off} = 6.45 x10^{-17}A, the highest I_{on}/I_{off} ratio= 9.52 x10^{10}, and *DIBL* of 11 mV/V. The I_{on}/I_{off} values are observed to be lower for low doping concentrations in the channel of JL-FinFETs due to electron crowding is comparatively low, reducing impurity scattering produced by Random Dopant Fluctuation (RDF) which is in agreement with [8]. From the results obtained, Structure B was chosen to further see the impact of various H_{fin} and W_{fin} on the performance of the JL-FET.

3.3 Results for Variations of Fin Height, H_{fin} (Structure B)

The simulations then proceed to see the impact of variations of H_{fin} on Structure B. Figure 6 and Table 4 show the results of various H_{fin} on a non-uniformly doped JL-FinFET at L_g =10 nm, W_{fin} =4 nm, and V_d = 1V. From the results shown in Table 4, it can be seen that the impact of variations in H_{fin} were quite negligible towards I_{off} and I_{on}. However, the variations in H_{fin} give a big impact towards the results of the *DIBL* with H_{fin} of 20nm shows the best results in terms of the lowest *DIBL*.

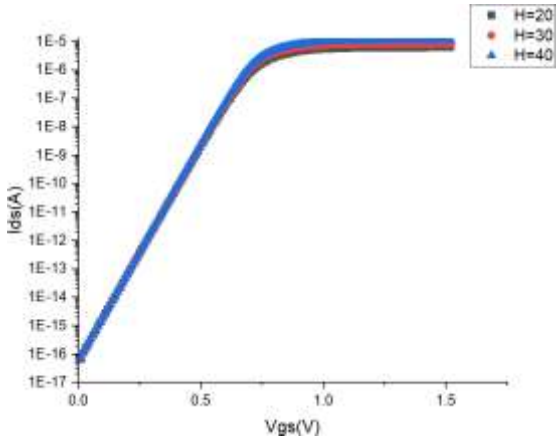

Figure 6. Plot of log I_d-V_g for various fin height, H_{fin} in saturation mode at V_d=1 V for Structure B JL-FinFET.

Table 4 Results obtained for various fin height, H_{fin} for Structure B JL-FinFET

Parameters	H_{fin} = 20 nm	H_{fin} = 30 nm	H_{fin} = 40 nm
I_{on} (A)	6.14 x 10^{-6} A	8.74 x 10^{-6} A	1.13 x 10^{-5} A
I_{off} (A)	6.45 x 10^{-17} A	6.67 x 10^{-17} A	8.70 x 10^{-17} A
I_{on}/I_{off}	9.52 x 10^{10}	1.31 x 10^{11}	1.30 x 10^{11}
DIBL (mV/V)	11	15	21

3.4 Results for Variations of Fin Width, W_{fin} (Structure B)

Lastly, the impact of fin width, W_{fin} variations towards the device performance of structure B at fixed H_{fin} of 20 nm were studied. Figure 7 shows the impact of variations of W_{fin} of 4, 8, and 12 nm respectively at L_g=10 nm in terms of plot of log I_d-V_g. It can be seen from Table 5, that I_{on} and I_{off} are very sensitive to the variations of fin width, W_{fin}. The I_{on}/I_{off} ratio reduces with the increase in W_{fin}. In terms of *DIBL*, W_{fin}=4 nm shows the best *DIBL*, followed by W_{fin}=8 and 12 nm respectively. It could be seen that decreasing the W_{fin} provides lower I_{off} and superior electrostatic performance of *DIBL* which is in agreement with [9].

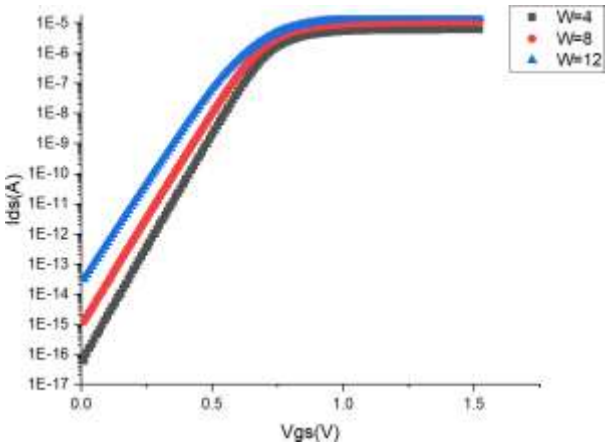

Figure 7. Plot of log I_d-V_g for various fin width, W_{fin} in saturation mode at V_d=1 V for Structure B JL-FinFET.

Table 5 Results obtained for various fin width, W_{fin} for Structure B JL-FinFET

Parameters	W_{fin} **= 4 nm**	W_{fin} **= 8 nm**	W_{fin} **= 12 nm**
I_{on} (A)	6.14 x 10^{-6} A	1.13 x 10^{-5} A	1.64 x 10^{-5} A
I_{off} (A)	6.45 x 10^{-17} A	1.28 x 10^{-15} A	3.36 x 10^{-14} A
I_{on}/I_{off}	9.52 x 10^{10}	8.83 x 10^{9}	4.88 x 10^{18}
DIBL (mV/V)	11	32	63

4. CONCLUSION

In this work, implications of various doping concentrations, fin height (H_{fin}) and fin width (W_{fin}) on the electrostatic performance of a JL-FinFET were investigated. It was found that a non-uniform doping concentration has better control on the results of I_{off} and *DIBL* as compared to uniform doping concentration. Later, it can be further seen that the variations of different configurations of non-doping concentrations also affect the device performance, where among the 4 structures simulated (Structure A, B, C and D), structure B which has a non-uniform doping concentrations of 4 x10^{18} cm^{-3} for source and drain and 4 x10^{17} cm^{-3} for the channel shows the best results. In terms of variations of H_{fin} and W_{fin}, it was found that H_{fin} of 20 nm and W_{fin} of 4 nm give the best results of I_{off} = 6.45 x10^{-17} A, I_{on} = 6.14 x10^{-6} A, I_{on}/I_{off} = 9.52 x10^{10} and *DIBL* = 11 mV/V.

ACKNOWLEDGEMENTS

The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of FRGS/1/2020/STG07/UNIMAP/02/7 from the Ministry of Higher Education Malaysia.

REFERENCES

[1] S. K. Dargar and V. M. Srivastava, "Performance Analysis of 10 nm FinFET with Scaled Fin-Dimension and Oxide Thickness," *2019 Int. Conf. Autom. Comput. Technol. Manag. ICACTM 2019*, pp. 1–5, 2019.

[2] N. E. I. Boukortt, T. R. Lenka, S. Patanè, and G. Crupi, "Effects of varying the fin width, fin height, gate dielectric material, and gate length on the dc and rf performance of a 14-nm soi finfet structure," *Electron.*, vol. 11, no. 1, 2022.

[3] J. P. Colinge *et al.*, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid. State. Electron.*, vol. 65–66, pp. 33–37, Nov. 2011.

[4] C.-W. Lee *et al.*, "Performance estimation of junctionless multigate transistors," *Solid. State. Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[5] J. H. Choi *et al.*, "Origin of device performance enhancement of junctionless accumulation-mode (JAM) bulk FinFETs with high-κ gate spacers," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1182–1184, 2014.

[6] M. Kumar, K. Aditya, and A. Dixit, "A Junctionless Accumulation Mode NC-FinFET Gate Underlap Design for Improved Stability and Self-Heating Reduction," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3424–3430, 2020.

[7] J. Kim, J. W. Han, and M. Meyyappan, "Reduction of Variability in Junctionless and Inversion-Mode FinFETs by Stringer Gate Structure," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 470–475, 2018.

[8] S. Manikandan, N. B. Balamurugan, and T. S. Arun Samuel, "Impact of uniform and non-uniform doping variations for ultrathin body junctionless FinFETs," *Mater. Sci. Semicond. Process.*, vol. 104, no. March, p. 104653, 2019.

[9] A. Paul *et al.*, "Fin width scaling for improved short channel control and performance in aggressively scaled channel length SOI finFETs," *2013 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. S3S 2013*, vol. 54, pp. 3–4, 2013.