

International Journal of Nanoelectronics and Materials

IJNeaM

ISSN 1985-5761 | E-ISSN 2232-1535



A review: Fluorine implantation in poly-Si gate, P+/N-junction, and Ti-Salicide on silicon nanoelectronics device

Lee Sai Link a,b, Tan Chan Lik b, and Mohamed Fauzi Packeer Mohamed a *

- ^aSchool of Electrical and Electronic Engineering, Engineering Campus, Universiti Sains Malaysia, 14300 Nibong Tebal, Pulau Pinang, Malaysia
- ^bInfineon Technologies (Kulim) Sdn Bhd, Kulim Hi-Tech Park, 09000 Kulim, Kedah, Malaysia
- *Corresponding author. Tel.: +604-5996097; fax: +604-5946909; e-mail: fauzi.packeer@usm.my

Received 17 September 2024, Revised 6 January 2025, Accepted 16 January 2025

ABSTRACT

This paper reviews the behavior of Fluorine implantation on nanoelectronics devices, focusing on three device areas: Poly-Si gate, P+/N-junction, and Ti-Salicide. The study reveals that the mechanism of Fluorine in bond strain relaxation at the SiO_2 -Si interface, reduces transient enhanced diffusion of Boron in P+/N-junction, and promotes the formation of C-54 phase Titanium Silicides. The paper summarizes the potential of Fluorine implantation to enhance electrical characteristics and reliability stress in poly-Si gate and P+/N-junction. It provides insights into optimizing Fluorine implantation processes to balance its positive and negative effects on nanoelectronics device fabrication, suggesting an optimum range of Fluorine concentration to achieve the best performance. Ultimately, this paper emphasizes the critical role of Fluorine implantation in advancing the efficiency and performance of nanoelectronics devices.

Keywords: Nanoelectronics device, Fluorine implantation, Poly-Si gate, P+/N-junction, Ti-Salicide

1. INTRODUCTION

Ion implantation is a critical process in nanoelectronics technology, used extensively in the fabrication of semiconductor devices. It involves bombarding a semiconductor substrate, with high-energy ions to modify its electrical properties [1]. This process allows precise control over doping concentration and depth, which is essential for creating various components such as diodes, and transistors. However, creating Ultra Shallow Junctions (USJs) presents specific challenges, particularly in achieving the desired junction depth and sharp doping profiles while minimizing damage to the substrate [2, 3]. Low-energy ion implantation is utilized to control the penetration depth precisely, but this approach necessitates advanced annealing techniques to activate the dopants without causing excessive diffusion. Additionally, minimizing leakage currents, which can result from interface traps and defects introduced during implantation, remains a critical concern.

Therefore, Fluorine implantation which is used as codopant prior to boron can suppress Boron Transient Enhanced Diffusion (TED) [2–5] and enhance Boron activation [3, 4]. Furthermore, it also reduces the interface trap density [5, 6] and reduces leakage current [7] at P+/N junctions, thereby enhancing the electrical characteristics and reliability of the nanoelectronics devices [7–12]. To effectively utilize these benefits, a fundamental understanding of Fluorine behavior is essential. Through

this review, the potential benefits and practical applications of Fluorine implantation in enhancing the performance and reliability of semiconductor devices are explored.

Fluorine ions are introduced during the implantation process and subsequently impact the characteristics of several device areas: (1) Poly-Si gate, (2) P+/N- junction and (3) Ti-Salicide (TiSi₂), while Lightly Doped Drain (LDD) is simultaneously formed, as illustrated in Figure 1. Accordingly, this paper is divided into five main sections, whereby Section 2 describes the methodology of Fluorine implantation. Section 3 explores the characteristics of Fluorine implantation at the interface of Poly/SiO₂ and Si-SiO₂. Section 4 investigates the characterization of Fluorine implant in P+/N-Junction. Section 5 examines the effect of Fluorine implantation on Ti-Salicide. Finally, Section 6 concludes with an overall impact of Fluorine implantation on P-type Metal-Oxide-Semiconductors (PMOS) devices.

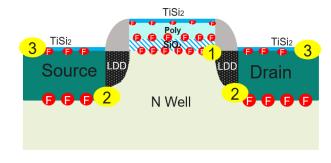


Figure 1. Physical structure of PMOS transistors

2. METHODOLOGY OF FLUORINE IMPLANTATION

PMOS process flow is introduced in Figure 2 as a general background for the Fluorine-related process [13]. Several combinations of Fluorine implantation with Boron are presented in Table 1. The most used methods for introducing Fluorine ions include BF₂+ ion implantation and a separate Boron implantation followed by Fluorine implantation. In the fabrication process, the existence of Fluorine significantly impacts three process blocks, which are (1) gate oxide and poly deposition, (2) source/drain formation, and (3) Ti-salicidation, as illustrated in Figure 2.

3. CHARACTERISTICS OF FLUORINE IMPLANTATION AT THE INTERFACE OF POLY/SI & SI-SIO $_{\rm 2}$

The mechanism of Fluorine in polysilicon (poly-Si) layers and at the Si/SiO_2 interface has been extensively studied [13]. From various Secondary Ion Mass Spectrometry (SIMS) profiles [10, 24], Fluorine peak is at the middle of SiO_2 , interface, as shown in Figure 3.

Initially, the Fluorine ions are implanted on the polycrystalline silicon, as the annealing temperature increases, Fluorine atoms are anomalously diffused. A localized accumulation of Fluorine was noticed near the peak point of the Fluorine distribution [31]. The redistribution of Fluorine at silicon is observed and influenced by the magnitude and distribution of persistent damages from post-annealing [32]. The Fluorine diffusion is enhanced in the presence of grain boundaries, and Fluorine atoms may be trapped at the grain boundaries. Then, incorporating grain boundaries in the Poly-Si can improve the electrical properties of thin film transistors or solar cells [31]. Therefore, optimum Fluorine passivation of grain boundaries can mitigate the damages caused by previous high-dose implantation at Si–SiO₂ interface [14, 24, 31].

Furthermore, the optimum amounts of Fluorine in the oxide at the Si/SiO₂ interface can improve the oxide breakdown voltage, lower leakage current [11], and interface hardness against hot electrons [12] and radiation damage of MOS devices [33]. The improvement of reliability is due to the reduction of local strain relaxation [13, 34, 35] and interface states [10, 23, 35] due to Fluorine implantation. This process breaks strained Si-O-Si bonds near the SiO₂/Si interface and forms the Si-F bonds and non-bridging Si-O bonds. The Fluorine in thermal SiO₂ tends to form Si-F bonds rather than O-F bond or Si-OF bond [34, 36], which leads to the relaxation of the interfacial strain, consistent to the observed Fluorine-induced oxide stress relaxation [37]. Based on the bond strain gradient model, Si-F bond can suppress the migration of non-bridging oxygen defects towards the Si-SiO₂ interface, thus reducing interface traps [11, 38]. Therefore, the strain distribution near the interface can improve the radiation or hot-carrier hardness of the gate oxide by relaxing the oxide stress near the interface [11].

However, Nishioka et al. [12] found that when an excessive amount of Fluorine is introduced, a high density of

nonbridging oxygen bonds is created. Although there is local strain relaxation to inhibit defect migration at the same time, it will lead to performance degradation due to the O shift of F from strained Si–O–Si bonds [33], this model is also supported by Kouvatsos $et\ al.$ and Mitani $et\ al.$ [23]. Thus, the charge-to-breakdown (Qbd) improvement and oxide thickness increase due to the strain release and the recombination of the local SiO₂ structure by doping Fluorine [8, 23]. It concludes that the optimum Fluorine concentration is achieved when the advantages of strain relaxation far exceed the adverse effect of the non-bridging oxygen bonds [13].

Table 1. Fluorine implantation methodology

Type of dopants	References
B + F	[2, 4, 7–9, 14, 17]
F + B	[3, 18-21]
BF ₂	[3, 16, 18, 21–28]
BF ₂ + B	[18]
BF ₂ + F	[29, 30]
$F + BF_2$	[29, 30]

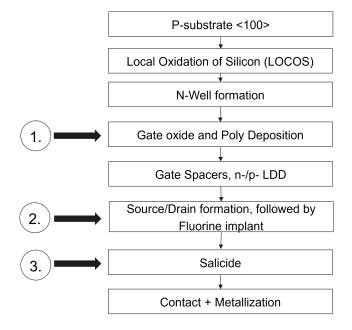


Figure 2. Process flow of PMOS

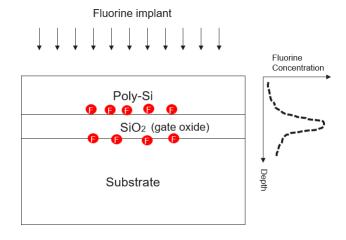


Figure 3. Fluorine distribution in gate oxide

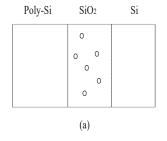
3.1. Si-F Bonds Properties

A Fluorine-enriched region in SiO₂ is created when Fluorine implantation into the top layer of the poly-Si gate electrode at low energies, followed by high-temperature annealing processing that drives Fluorine into the SiO₂ [8]. Stronger interfacial Si-F bonds are more resistant to breakage under high-temperature electrical stress than Si-H bonds. With more incredible bonding energy (5.73 keV) for Si-F bonds than Si-H bonds (3.18 keV) as depicted in Figure 4, the electrical and thermal stress of Si-F bonds is superior, contributing to enhanced oxide reliability [39] and resistance to radiation or hot-carrier damage [10, 11]. Furthermore, the increased bond strength and chemical stability make Si-F bonds less reactive and more resistant to thermal decomposition, which can improve the dielectric quality of the gate oxide layer by reducing trap states. Si dangling bonds and Si-O bonds are replaced by the Fluorine atoms in the gate oxide to form Si-F bonds. In short, Si-F bonds help to suppress the generation of interface traps at the Si/SiO₂ interface due to higher binding energy [12, 36, 39].

3.2. Physical and Electrical Characteristics of Fluorineimplanted PMOS Devices

The incorporation of Fluorine at the interface of poly-Si and $Si-SiO_2$ can enhance both physical and electrical characteristics, as summarized in Table 2. These improvements include a shift in the flat band voltage to positive [8, 9], increase gate oxide thickness [40], decrease dielectric constant [41], decrease in gate leakage current [42], and reduction in interface trap density [37, 42]. It is concluded that there is a trade-off between the amount of Fluorine incorporation, determining the thickness and reliability of the gate oxide.

Fluorine implantation [24, 40] showed that the gate oxide (SiO₂) thickness is increased, and oxide quality is improved due to the reduction in interface state density after the annealing process [40]. Wright *et al.* [8] proposed a two-step model to explain the diffusion behavior of Fluorine in poly-Si/SiO₂ and SiO₂/Si interface, as depicted in Figure 5. First, during the annealing post-fluorine implantation, the Fluorine ion diffuses and bonds to the dangling bonds, weakening bonds at the poly-Si/SiO₂ and SiO₂/Si interface. Thus, Fluorine distribution is established with the peaks near the Si/SiO₂ and poly-Si/SiO₂ interfaces [23]. The Fluorine molecules disrupt Si–O bonds and displaces



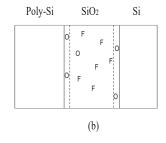


Figure 5. Fluorine distribution (a) without fluorine implant and (b) with fluorine implant after annealing

oxygen at the SiO_2/Si and poly- Si/SiO_2 interfaces, and the dangling bonds on a silicon atom act as a hole trap, as shown in Figure 6(b). Fluorine enhances oxygen diffusion in gate oxide bulk after the annealing process. The free oxygen diffuses towards the interface to oxidize the additional silicon, showing that additional oxide is being generated. This can be explained by the fact that Fluorine contributes to oxide growth as it reacts at the interface between the Si/SiO_2 , therefore increasing the gate oxide (SiO_2) thickness [8, 40].

Table 2. Summary of physical/electrical characteristics impacts by fluorine implantation

Physical / Electrical	Results	References
Characteristics		
Gate thickness oxide	Increase	[8, 22, 23, 29, 43,
	16.75%	44, 46]
Average Roughness (Ra)	Reduce by	[10]
	44.8%	
Flat band voltage	Shift	[8, 9, 14, 24, 40,
	~-40 mV	45]
Refractive index	Decrease	[41]
Gate leakage current	Decrease	[7, 10]
Breakdown electric field	Increase	[8, 10, 66]
Interface trap density	Decrease by	[11–14, 23, 33,
	27%	42-45]
Transconductance	Improve	[33, 45, 46]
DIBL	Shift	[9]
	~24 mV	

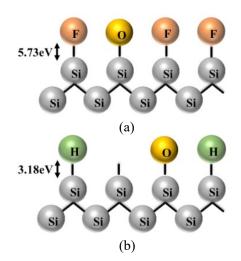


Figure 4. Si/SiO₂ interface bonding structure: (a) passivated interface with fluorine atoms; (b) passivated interface with hydrogen atoms [39]

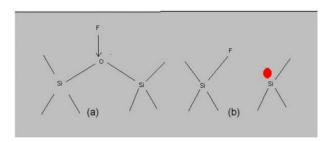


Figure 6. (a) Fluorine displaces oxygen in the Si-O-Si bond. (b) The dangling bond on the silicon atom acts as a trap [40]

Furthermore, Fluorine-implanted devices have more smooth surfaces by 44.8 % than non-implanted devices [10] due to the incorporated Fluorine breaking the strain bonds, lead to the formation of strong Si–F bonds in the interface, thereby smoother the surface morphology. In electrical characteristics, the flat band voltage (V_{FB}) shifted to positive in the Fluorine implant device, indicates that the Fluorine implant can generate a negative fixed charge at the interface of Si/SiO₂ [8, 9]. When the Fluorine atoms are incorporated, Si–F bonds are formed to remove the weak interactions and weak bonds such as Si–Si or Si–O. Thus, the corresponding energy state is moved out of the energy bandgap, reducing the interface state density [37].

Additionally, the incorporation of Fluorine atoms into SiO_2 films can reduce dielectric constant and refractive index [38, 41]. Therefore, the structural alteration of gate-oxide films is a result of the reaction between Fluorine atoms and Si–O bonds [23]. Due to high cumulative dose or etching effect in the process, the Fluorine concentration in the silicon dioxide film is high, which leads to the decrease of dielectric constant with implantation time [47]. As a result, the Fluorine implantation enhances the stability of the SiO_2 film.

Besides that, the Fluorine-implanted poly-gate also lower leakage current [10] and higher breakdown electric field [10] due to the decrease of gate oxide defects [42]. The interface trap density in samples implanted with Fluorine ions is reduced [11] compared to un-implanted oxide samples as Si–F bonds have a smaller bond length and lower polarizability compared to Si–OH bonds, which can reduce the likelihood of defects and traps. Moreover, drain-induced barrier lowering (DIBL) is a short-channel effect in MOSFETs occurring when the voltage at the drain terminal of the transistor causes a reduction in the potential barrier

at the source-drain junction, resulting in a lowering of the threshold voltage. Fluorine-implant also improve the DIBL by \sim 24mV [6, 9], indicating the improvement of the short channel margin. It is believed that the incorporation of Fluorine will increase the barrier.

In short, the observed improvements in electrical characteristics evidence the effectiveness of Fluorine ions in improving gate oxide quality [68]. However, excessive amount of Fluorine dose seems to result in performance degradation due to the generation of non-bridging oxygen centers. Thus, the optimum Fluorine-implanted dose is suggested in the range of 5×10^{14} to 2×10^{15} cm⁻².

3.3. Reliability Improvement by Fluorine Implantation

Fluorine implantation in Poly-Silicon gates enhances device reliability performance in negative-bias temperature instability (NBTI) [9, 22, 29, 39, 67] as shown in Figure 7(a). Siti Zubaidah *et al.* have demonstrated that Fluorine implantation at the channel region effectively mitigates the NBTI at the SiO₂ interface [22]. Moreover, as shown in Figure 7(b), the Fluorine-implanted devices display a longer Time Dependent Dielectric Breakdown (TDDB) lifetime compared to the base device [9], as well as hot carrier injection (HCI) [22].

The reliability enhancement of nanoelectronics devices through Fluorine implantation is summarized in Table 3. By optimizing implantation parameters such as energy and dose, it is possible to achieve these benefits while minimizing potential damage to the gate oxide. Improvements in interfacial stability [10] are attributed to the relaxation of strain at the interface or the replacement of Si–H bonds with stronger Si–F bonds.

Reliability test	Results	References
Negative Bias Temperature Instability (NBTI)	Lifetime improves 0.6x times	[6, 9, 29, 39, 67]
Hot carrier injection (HCI)	Lower shifts of the transconductance and threshold voltage	[12, 22, 46]
Time dependent dielectric breakdown (TDDB)	Lifetime improves	[9, 46]

Table 3. Summary of stress reliability characteristics impacts by fluorine implantation

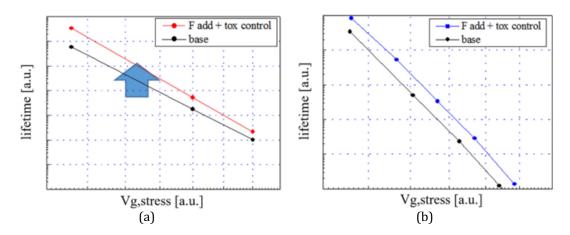


Figure 7. (a) NBTI lifetime vs Vg, stress and (b) TDDB vs Vg, stress for the base device and the F add + tox controlled, respectively [9]

4. CHARACTERIZATION OF FLUORINE IMPLANT ON P+/N-JUNCTION

As semiconductor devices continue to shrink, there is an increasing demand for shallow P+/N-junctions with low sheet resistance. However, achieving these shallow junctions through B+ implantation can be challenging due to the rapid boron diffusion in the Si substrate and ion channeling effect [33]. Ion implantation inherently induces damage to the silicon lattice, resulting in the substantial supersaturation of silicon self-interstitial (I's) during postimplantation annealing. During the initial annealing stages, the self-interstitial supersaturation can enhance the diffusivity of dopants, such as Boron (B), Phosphorus (P), and Arsenic (As). However, the formation of end-of-range (EOR) defects, which are interstitial-type dislocation loops, leads to transient enhanced diffusion (TED) [14-17, 20, 21, 48, 49]. Therefore, Fluorine implantation has been employed in P+/N interface as shown in Figure 8 to improve short-channel effects by diminishing Boron diffusion in Silicon.

One of the techniques that has been utilized to form shallow P+/N-junctions is through BF₂+ ion implantation [18, 19, 25, 26]. Fluorine implantation has been demonstrated to reduce TED of Boron [2, 3, 7, 15, 17, 19, 20, 49, 52], resulting in a steeper annealed Boron profile. This reduction in Boron TED, as observed through various secondary ion mass spectrometry (SIMS) measurements [3, 16, 19, 50] leads to a decrease in junction depth with a pronounced energy dependence [19, 51].

Furthermore, Fluorine significantly impacts diffusivity and reactivation of Boron through the formation of Fluorine-Vacancy (FV) clusters. The effect of Fluorine on point defects has been studied through direct observation of Si self-diffusion [17], which is occurring through the interstitial (I) and vacancy (V) mechanisms. In the presence of Fluorine, the enhanced self-diffusion of Si is due to an increase of vacancies (V) concentration emitted when FV clusters dissolve. Additionally, the diffusion of boron is reduced because I (Interstitial) undersaturation, resulting in an increase in V concentration owing to FV clusters [4, 5, 49, 54, 59]. Thus, the enhancement of Si self-diffusion is explained by the increase of V concentration, while the diffusion of boron is reduced by diminishing the I concentration.

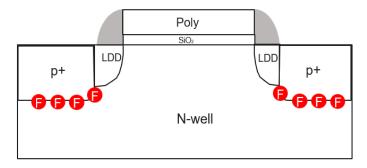


Figure 8. Fluorine ions exist in P+/N-well interfaces

Besides that, the presence of Boron atoms also suppresses the dissolution of FV clusters, and it is observed that the FV clusters are nearly immobile around the Boron peak when Fluorine is implanted with Boron, which is an area that aligns with the peak of Fluorine [20]. The V emission from FV clusters cannot account for the characteristic pinning of the Boron diffusion. These findings suggest there is a direct interaction between Fluorine and Boron, especially when both Fluorine and Boron atoms coexist at the high concentrations [21]. Consequently, this trapping reduces the boron diffusion due to the Fluorine-Boron interaction.

In summary, the overall picture of the boron effect in TED suppression by Fluorine incorporation is attributed to I undersaturation caused by FV clusters in low Fluorine concentration and the direct Fluorine-boron interaction in high Fluorine concentration. The current work demonstrates that the effects of FV clusters and F–B interaction are coexisted to explain the mechanism of boron TED suppression.

4.1. Physical and Electrical Characteristics at P+/N-Junction in PMOS Devices

Table 4 summarizes the effects of Fluorine implantation on the physical and electrical properties. Fluorine has been shown to retard the diffusion of boron, leading to shallower junctions in P+/N-junctions and reduced sheet resistance. According to Huang *et al.* [3], Fluorine pre-amorphization can effectively suppress Boron TED in regions with low Boron concentration. This leads to a steep dopant profile that facilitates the formation of shallow junctions. The interaction of Fluorine with defects in the low boron concentration region is thought to impede boron diffusion, thereby controlling the dopant distribution. As a result, the process of implanting low-energy Boron into Fluorine preamorphized Silicon, followed by rapid thermal annealing to achieve shallow junction formation, is enabled.

Furthermore, the degradation of leakage current in P+/N-junction can be improved by Fluorine implantation [30, 57]. Experiment results [57] demonstrate that the implantation of BF $_2$ followed by Fluorine improves the leakage current in the P+/N-junction by one decade. In a PN-junction, the minority carriers can cross through the depletion region. However, there are generations and recombination occurring at trapping centers. Therefore, when the Fluorine

Table 4. Summary of physical and electrical characteristics impacts by fluorine implantation

Physical / Electrical Characteristics	Results	References
Junction depth	Shallower	[4, 15, 44, 45, 51]
Sheet resistance	Reduce by 44%	[2, 16, 39, 45, 47, 51, 55, 59, 68]
Leakage current	Decrease	[3, 43, 52, 54, 60]
Breakdown voltage	Increase	[52]
Transconductance	Increase	[16]

level is low, fewer traps are generated at the depletion region, thereby resulting in reduced generation-recombination current, which contributes to a decrease in leakage current in pn-junction. As a result, Fluorine can deepen the EOR location [70], which is supported by Haizhou Yin *et al.* [58], thus improving the electrical characteristics of P+/N-junction.

Additionally, the reduced Boron concentration observed in the SIMS profile contributes to an improved breakdown voltage. This is achieved by creating a wider depletion region in the P-N junction [57]. When the Fluorine dose or energy increases, more Si–F bonding is formed and minimizes the V_T shift during NBTI stress. This leads to a deeper F projected range (Rp), as more Fluorine atoms being incorporated into the SiO₂ interface. This interaction reduces capacitance and increases oxide thickness, which is discussed in Section 3. Besides, the effectiveness of lateral redistribution suppression of Boron evidences the improvement of the short-channel effect, which indicates an improvement in the transconductance [18].

In summary, Fluorine implantation has been studied for its beneficial effects on dopant activation and junction performance in P+/N junction. Co-implantation of Fluorine has been proved to reduce the Boron TED and achieve a shallow junction with low sheet resistance. Implantation of Fluorine can alter the doping profile and carrier concentration. By controlling the Fluorine dose and energy during BF_2 implantation, it is possible to optimize the device's electrical performance, particularly those relying on PN junction diodes.

5. CHARACTERISTICS OF TI-SALICIDE POST FLUORINE IMPLANTATION

Fluorine plays a significant role in Salicide processes as shown in Figure 9. Metals like Titanium, Tungsten, Nickel, and Cobalt, are alloyed with the top Poly-Silicon layers to create a metal Silicide layer that exhibit improved electrical properties for interfacing with Aluminum [60, 61].

Titanium Silicide ($TiSi_2$) has been widely used in semiconductor devices due to its low resistivity and good compatibility with Silicon [55, 65]. During the salicidation process, where Titanium reacts with Silicon to form low-resistance contacts, Fluorine is introduced to improve the quality of the silicide. However, a high Fluorine

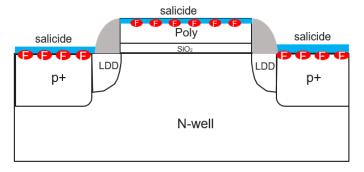


Figure 9. Fluorine ions are present on the silicide metal layer

concentration can diffuse into the TiSi₂ layer and even beyond it during high-temperature annealing. While Fluorine can enhance silicide's smoothness and interface quality, it may also cause Fluorine penetration into nearby regions can lead to detrimental effects. For instance, it may cause void formation [28], ultimately compromising the integrity of the material. Thus, this paper offers a comprehensive overview based on current research, shedding light on both the positive and negative impacts of Fluorine implantation on Ti-Salicide.

5.1. Beneficial Impacts of Fluorine Implant

The sheet resistance of $TiSi_2$ on Si is reduced by enhancing the formation of C-54 nucleation sites [63]. Since the Fluorine is implanted into silicon through BF_2 or Fluorine ion, a cap oxide layer is deposited over the silicon surface [63] after Fluorine implantation. This layer protects the Silicon and controls the diffusion of Fluorine within the Silicon lattice. During the annealing process, Fluorine outgassing produces bubbles in silicon. When the covering oxide is removed, the gas is released, and the surface of the silicon becomes pitted and uneven. This surface topography enhances the subsequent formation of C-54 nucleation sites, leading to improved silicide properties.

The reduced sheet resistance of Titanium Silicide on Silicon can be attributed to the physical principles underlying preamorphization techniques utilizing high-dose Fluorine implants. According to Chenl *et al.* [62], the conversion rate of C-49 to C-54 do not increase by pre-amorphization. However, the pre-amorphization enhance the reaction rate between Titanium (Ti) and weakly bonded amorphous silicon. It leads to the formation of C-54 phases with a larger grains and lower resistivity. Xiao *et al.* [64] also propose that pre-amorphization makes use of the latent energy existing in amorphous silicon, thereby expedite the kinetics of the C-54 phase transformation reaction. Consequently, Fluorine implant causes pre-amorphization and decrease the sheet resistance on silicided surfaces to promote the formation of C-54 phase Titanium Silicides.

5.2. Negative Effects of Fluorine Implant

It has been observed that using BF_2^+ for p+ source/drain implant results in void formation within $TiSi_2$ film on P+ Polycrystalline Silicon (Poly) and diffusion regions [28] and Fluorine atoms are responsible for the void formation [56]. As voids are only observed at post-silicidation, therefore it is suggested that the void formation in Silicide films is a consequence of the interaction between Fluorine outgassing and Titanium silicidation [28, 70].

Majority of the voids exist at the interface between the grain boundary of the Polycrystalline $TiSi_2$ and the P+ Silicon substrate, which often accompanied by an extended defect that penetrates into the P+ Silicon substrate. TEM profiles suggest that the formation of void is particularly susceptible to the BF_2^+ implantation and annealing temperature for the P+ junction. These voids are attributed to Fluorine-related precipitates, which are derived from the BF_2^+ ion

implantation. However, the impact of the Fluorine at the junction leakage and sheet resistance can be substantially minimized by incorporating an additional thermal annealing step between the P+ junction activation anneals, and the Ti-Salicide module. This approach does not compromise the performance of the pMOSFET devices. Therefore, it is concluded that the influence of Fluorine on the TiSi₂ salicide process can lead to void formation. The presence of these voids can significantly reduce the device's electrical characteristics, particularly in terms of leakage current and sheet resistance [28, 70].

6. CONCLUSION AND OUTLOOKS

In conclusion, this review paper provides a comprehensive understanding of the impact of Fluorine implantation on three components of device areas: Poly-Si/SiO2 interface, P+/N-junction, and Ti-salicide formation. At the Poly-gate, it effectively facilitates bond strain relaxation at the SiO₂-Si interface, fostering the development of stronger and more stable Si-F bonds while simultaneously suppressing the formation of interface traps. At the P+/N-junction, the presence of Fluorine contributes to a reduction in the TED of Boron, thereby enabling the creation of shallow junctions with low sheet resistance. The implantation of Fluorine can lead to a steeper doping profile and carrier concentration, thereby significantly improving the device's electrical characteristics and stress reliability. Lastly, at the Ti-Salicide, the pre-amorphization of Fluorine implants leads to decreased sheet resistance on silicided surfaces and promotes the formation of the C-54 phase Titanium silicides.

Overall, these aforementioned advantages emphatically highlight the potential of Fluorine implantation as an effective technique for enhancing the performance and reliability of advanced semiconductor devices. However, it also demonstrated that the use of low doses of Fluorine atoms in the implantation process can result in a reduction of the interface trap density, while higher doses of Fluorine atoms have the opposite effect. Therefore, it is crucial to control the Fluorination process in order to strike an optimal balance between the positive and negative effects.

ACKNOWLEDGMENTS

This research was funded by Infineon Technologies (Kulim) Sdn. Bhd., and the APC was funded by UNIVERSITI SAINS MALAYSIA (USM).

REFERENCES

- [1] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Wiley, 2006. doi: 10.1002/0470068329.
- [2] H. Graoui and M. A. Foad, "A comparative study on ultra-shallow junction formation using co-implantation with fluorine or carbon in preamorphized silicon," *Materials Science and Engineering: B*, vol. 124–125, pp. 188–191, Dec. 2005, doi: 10.1016/j.mseb.2005.08.040.
- [3] T. H. Huang, H. Kinoshita, and D. L. Kwong, "Influence

- of fluorine preamorphization on the diffusion and activation of low-energy implanted boron during rapid thermal annealing," *Applied Physics Letters*, vol. 65, no. 14, pp. 1829–1831, Oct. 1994, doi: 10.1063/1.112857.
- [4] M. Diebel, S. Chakravarthi, S. T. Dunham, C. F. Machala, S. Ekbote, and A. Jain, "Investigation and Modeling of Fluorine Co-Implantation Effects on Dopant Redistribution," *MRS Proceedings*, vol. 765, p. D6.15, Feb. 2003, doi: 10.1557/PROC-765-D6.15.
- [5] H. A. W. el Mubarek *et al.*, "Effect of fluorine implantation dose on boron thermal diffusion in silicon," *Journal of Applied Physics*, vol. 96, no. 8, pp. 4114–4121, Oct. 2004, doi: 10.1063/1.1790063.
- [6] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Dual role of fluorine at the Si-SiO2 interface," *Applied Physics Letters*, vol. 85, no. 21, pp. 4950–4952, Nov. 2004, doi: 10.1063/1.1825621.
- [7] K. Ohyu, T. Itoga, and N. Natsuaki, "Advantages of Fluorine Introduction in Boron Implanted Shallow p+/n-Junction Formation," *Japanese Journal of Applied Physics*, vol. 29, no. 3R, p. 457, Mar. 1990, doi: 10.1143/JJAP.29.457.
- [8] P. J. Wright and K. C. Saraswat, "The effect of fluorine in silicon dioxide gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 36, no. 5, pp. 879–889, May 1989, doi: 10.1109/16.299669.
- [9] S. Lee *et al.*, "Improved electrical characteristics and reliability of p-MOSFET with fluorine implant," *Solid-State Electronics*, vol. 167, p. 107783, May 2020, doi: 10.1016/j.sse.2020.107783.
- [10] C. H. Kao, C. S. Lai, and C. L. Lee, "Electrical and Reliability Improvement in Polyoxide by Fluorine Implantation," *Journal of The Electrochemical Society*, vol. 154, no. 4, p. H259, 2007, doi: 10.1149/1.2433471.
- [11] K. Ohyu, T. Itoga, Y. Nishioka, and N. Natsuaki, "Improvement of SiO₂/Si Interface Properties Utilising Fluorine Ion Implantation and Drive-in Diffusion," *Japanese Journal of Applied Physics*, vol. 28, no. 6R, p. 1041, Jun. 1989, doi: 10.1143/JJAP.28.1041.
- [12] Y. Nishioka, K. Ohyu, Y. Ohji, N. Natuaki, K. Mukai, and T.-P. Ma, "Hot-electron hardened Si-gate MOSFET utilizing Fimplantation," *IEEE Electron Device Letters*, vol. 10, no. 4, pp. 141–143, Apr. 1989, doi: 10.1109/55.31697.
- [13] T. P. Ma, "Effects of Fluorine on MOS Properties," *MRS Proceedings*, vol. 262, p. 741, Sep. 1992, doi: 10.1557/PROC-262-741.
- [14] H.-H. Tseng, P. J. Tobin, F. K. Baker, J. R. Pfiester, K. Evans, and P. L. Fejes, "The effect of silicon gate microstructure and gate oxide process on threshold voltage instabilities in p*-gate p-channel MOSFETs with fluorine incorporation," *IEEE Transactions on Electron Devices*, vol. 39, no. 7, pp. 1687–1693, Jul. 1992, doi: 10.1109/16.141235.
- [15] L. S. Robertson *et al.*, "Junction Depth Reduction of ion Implanted Boron in Silicon Through Fluorine ion Implantation," *MRS Proceedings*, vol. 610, p. B4.2, Mar. 2000, doi: 10.1557/PROC-610-B4.2.
- [16] E. Ishida, D. F. Downey, K. S. Jones, and J. Liu, "The

- chemical effect of fluorine on boron transient enhanced diffusion," in 1998 International Conference on Ion Implantation Technology. Proceedings (Cat. No.98EX144), IEEE, pp. 909–912. doi: 10.1109/IIT.1998.813816.
- [17] M. N. Kham, H. A. W. el Mubarek, J. M. Bonar, and P. Ashburn, "Effect of fluorine on boron thermal diffusion in the presence of point defects," *Materials Science and Engineering: B*, vol. 124–125, pp. 192–195, Dec. 2005, doi: 10.1016/j.mseb.2005.08.101.
- [18] J.-H. Lee, J.-Y. Lee, I. S. Yeo, and S.-K. Lee, "Lower sheet/contact resistance in shallower junction obtained by F+B mixed implant," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 20, no. 1, pp. 396–399, Jan. 2002, doi: 10.1116/1.1447247.
- [19] D. Girginoudi and C. Tsiarapas, "Impact of fluorine coimplantation on B deactivation and leakage currents in low and high energy Ge preamorphised p+n shallow junctions," *Materials Science and Engineering: B*, vol. 154–155, pp. 268–274, Dec. 2008, doi: 10.1016/j.mseb.2008.09.040.
- [20] R. Kiga, M. Uematsu, and K. M. Itoh, "Effect of fluorine on the suppression of boron diffusion in preamorphized silicon," *Journal of Applied Physics*, vol. 128, no. 10, Sep. 2020, doi: 10.1063/5.0015405.
- [21] A. Mokhberi, R. Kasnavi, P. B. Griffin, and J. D. Plummer, "Fluorine interaction with point defects, boron, and arsenic in ion-implanted Si," *Applied Physics Letters*, vol. 80, no. 19, pp. 3530–3532, May 2002, doi: 10.1063/1.1479458.
- [22] T. B. Hook, E. Adler, F. Guarin, J. Lukaitis, N. Rovedo, and K. Schruefer, "The effects of fluorine on parametrics and reliability in a 0.18-μm 3.5/6.8 nm dual gate oxide CMOS technology," *IEEE Transactions on Electron Devices*, vol. 48, no. 7, pp. 1346–1353, Jul. 2001, doi: 10.1109/16.930650.
- [23] Y. Mitani, H. Satake, Y. Nakasaki, and A. Toriumi, "Improvement of charge-to-breakdown distribution by fluorine incorporation into thin gate oxides," *IEEE Transactions on Electron Devices*, vol. 50, no. 11, pp. 2221–2226, Nov. 2003, doi: 10.1109/TED.2003. 818152.
- [24] Hsing-Huang Tseng, M. Orlowski, P. J. Tobin, and R. L. Hance, "Fluorine diffusion on a polysilicon grain boundary network in relation to boron penetration from P+ gates," *IEEE Electron Device Letters*, vol. 13, no. 1, pp. 14–16, Jan. 1992, doi: 10.1109/55. 144936.
- [25] K. K. Bourdelle, H.-J. L. Gossmann, S. Chaudhry, and A. Agarwal, "Comparison of B and BF₂ source/drain extension implants for PMOS transistors with thin gate oxides," in 2000 International Conference on Ion Implantation Technology Proceedings. Ion Implantation Technology 2000 (Cat. No.00EX432), IEEE, pp. 25–27. doi: 10.1109/IIT.2000.924081.
- [26] T.-Q. Zhang, J.-L. Liu, And X.-Y. Yang, "Migration of fluorine atoms and influence on shallow P+ N junction in B+2 implanted silicon under RTA," *Le Journal de Physique Colloques*, vol. 49, no. C4, pp. C4-

- 519-C4-522, Sep. 1988, doi: 10.1051/jphyscol: 19884108.
- [27] T. Noda *et al.*, "Impact of Fluorine co-implant on Boron Diffusion during Non-melt Laser Annealing," in *AIP Conference Proceedings*, AIP, 2006, pp. 21–24. doi: 10.1063/1.2401452.
- [28] K. L. Pey, R. Sundaresan, H. Wong, S. Y. Siah, and C. H. Tung, "Void formation in titanium desilicide/p⁺ silicon interface: impact on junction leakage and silicide sheet resistance," *Materials Science and Engineering: B*, vol. 74, no. 1–3, pp. 289–295, May 2000, doi: 10.1016/S0921-5107(99)00578-4.
- [29] S. Z. M. Saad, T. C. Lik, and S. H. Herman, "A study of fluorine dose and implant energy to the NBTI upon p⁺ implant sequence," in *2013 IEEE International Conference of Electron Devices and Solid-state Circuits*, IEEE, Jun. 2013, pp. 1–2. doi: 10.1109/EDSSC.2013. 6628076.
- [30] S. Z. M. Saad, T. C. Lik, M. A. Othman, P. Holger, and S. H. Herman, "A study of fluorine implant in the formation of low leakage P*/N junction in BiCMOS technologies," in 2012 International Conference on Enabling Science and Nanotechnology, IEEE, Jan. 2012, pp. 1–2. doi: 10.1109/ESciNano.2012. 6149654.
- [31] A. Yoshida *et al.*, "Hydrogen, fluorine ion implantation effects on polycrystalline silicon grain boundaries," *Solar Energy Materials and Solar Cells*, vol. 34, no. 1–4, pp. 211–217, Sep. 1994, doi: 10.1016/0927-0248(94)90042-6.
- [32] S.-P. Jeng, T.-P. Ma, R. Canteri, M. Anderle, and G. W. Rubloff, "Anomalous diffusion of fluorine in silicon," *Applied Physics Letters*, vol. 61, no. 11, pp. 1310–1312, Sep. 1992, doi: 10.1063/1.107575.
- [33] Y. Nishioka, K. Ohyu, Y. Ohji, N. Natsuaki, K. Mukai, and T. P. Ma, "The effect of fluorine implantation on the interface radiation hardness of Si-gate metaloxide-semiconductor transistors," *Journal of Applied Physics*, vol. 66, no. 8, pp. 3909–3912, Oct. 1989, doi: 10.1063/1.344012.
- [34] D. Kouvatsos, F. P. McCluskey, R. J. Jaccodine, and F. A. Stevie, "Silicon-fluorine bonding and fluorine profiling in SiO₂ films grown by NF3-enhanced oxidation," *Applied Physics Letters*, vol. 61, no. 7, pp. 780–782, Aug. 1992, doi: 10.1063/1.107796.
- [35] D. Kouvatsos, J. G. Huang, and R. J. Jaccodine, "Fluorine-Enhanced Oxidation of Silicon: Effects of Fluorine on Oxide Stress and Growth Kinetics," *Journal of The Electrochemical Society*, vol. 138, no. 6, pp. 1752–1755, Jun. 1991, doi: 10.1149/1.2085867.
- [36] M. Morita, T. Kubo, T. Ishihara, and M. Hirose, "Fluorine-enhanced thermal oxidation of silicon in the presence of NF₃," *Applied Physics Letters*, vol. 45, no. 12, pp. 1312–1314, Dec. 1984, doi: 10.1063/1.95131.
- [37] D. N. Kouvatsos, F. A. Stevie, and R. J. Jaccodine, "Interface State Density Reduction and Effect of Oxidation Temperature on Fluorine Incorporation and Profiling for Fluorinated Metal Oxide Semiconductor Capacitors," *Journal of The Electrochemical Society*, vol. 140, no. 4, pp. 1160–

- 1164, Apr. 1993, doi: 10.1149/1.2056216.
- [38] F. J. Grunthaner, P. J. Grunthaner, and J. Maserjian, "Radiation-Induced Defects in SiO₂ as Determined with XPS," *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 1462–1466, Dec. 1982, doi: 10.1109/TNS.1982.4336387.
- [39] S.-K. Kwon *et al.*, "Effects of Fluorine on the NBTI Reliability and Low-Frequency Noise Characteristics of p-MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 808–814, 2018, doi: 10.1109/JEDS.2018.2855432.
- [40] S. K. Sharma, B. Prasad, D. Kumar, and Raj kumar, "Alteration of gate oxides thickness for SOC level integration," *Materials Science in Semiconductor Processing*, vol. 12, no. 3, pp. 99–105, Jun. 2009, doi: 10.1016/j.mssp.2009.08.003.
- [41] J. W. Swart, J. A. Diniz, I. Doi, and M. A. B. de Moraes, "Modification of the refractive index and the dielectric constant of silicon dioxide by means of ion implantation," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 166–167, pp. 171–176, May 2000, doi: 10.1016/S0168-583X(99)00650-3.
- [42] S. K. Sharma, B. Prasad, D. Kumar, and R. Kumar, "Multiple thickness gate oxides with fluorine implantation for system on chip applications," *Vacuum*, vol. 83, no. 11, pp. 1359–1363, Jul. 2009, doi: 10.1016/j.vacuum.2009.04.045.
- [43] G. S. Virdi, C. M. S. Rauthan, B. C. Pathak, and W. S. Khokle, "Properties of the fluorine-implanted Si-SiO₂ system," *Solid-State Electronics*, vol. 34, no. 8, pp. 889–892, Aug. 1991, doi: 10.1016/0038-1101(91)90236-R.
- [44] J. H. Kim *et al.*, "Fluorine improvement of MOSFET interface as revealed by RTS measurements and HRTEM," in *2013 IEEE Radio and Wireless Symposium*, IEEE, Jan. 2013, pp. 97–99. doi: 10.1109/RWS.2013.6486653.
- [45] F. K. Baker *et al.*, "The influence of fluorine on threshold voltage instabilities in p⁺ polysilicon gated p-channel MOSFETs," in *International Technical Digest on Electron Devices Meeting*, IEEE, pp. 443–446. doi: 10.1109/IEDM.1989.74317.
- [46] S. Fujii *et al.*, "Impacts of Depth and Lateral Profiles of Fluorine Atoms in Gate Oxide Films on Reliability," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.2021.9405217.
- [47] T. Sakurai and T. Sugano, "Theory of continuously distributed trap states at Si-SiO₂ interfaces," *Journal of Applied Physics*, vol. 52, no. 4, pp. 2889–2896, Apr. 1981, doi: 10.1063/1.329023.
- [48] G. Impellizzeri, J. H. R. dos Santos, S. Mirabella, F. Priolo, E. Napolitani, and A. Carnera, "Suppression of Boron Diffusion by Fluorine Implantation in Preamorphized Silicon," *MRS Proceedings*, vol. 810, p. C5.9, Mar. 2004, doi: 10.1557/PROC-810-C5.9.
- [49] T. Shano *et al.*, "Realization of ultra-shallow junction: suppressed boron diffusion and activation by optimized fluorine co-implantation," in *International Electron Devices Meeting. Technical Digest (Cat.*

- *No.01CH37224*), IEEE, p. 37.4.1-37.4.4. doi: 10.1109/IEDM.2001.979640.
- [50] N. E. B. Cowern *et al.*, "Mechanisms of B deactivation control by F co-implantation," *Applied Physics Letters*, vol. 86, no. 10, Mar. 2005, doi: 10.1063/1.1870131.
- [51] H. A. W. el Mubarek and P. Ashburn, "Reduction of boron thermal diffusion in silicon by high energy fluorine implantation," *Applied Physics Letters*, vol. 83, no. 20, pp. 4134–4136, Nov. 2003, doi: 10.1063/1.1622434.
- [52] C. M. Osburn, D. F. Downey, S. B. Felch, and B. S. Lee, "Ultra-shallow junction formation using very low energy B and BF₂ sources," in *Proceedings of 11th International Conference on Ion Implantation Technology*, IEEE, pp. 607–610. doi: 10.1109/IIT. 1996.586472.
- [53] J.-H. Lee and H.-J. Lee, "The Analysis of p-MOSFET Performance Degradation due to BF₂ Dose Loss Phenomena," *Transactions on Electrical and Electronic Materials*, vol. 6, no. 1, pp. 1–5, Feb. 2005, doi: 10.4313/TEEM.2005.6.1.001.
- [54] M. N. Kham, I. Matko, B. Chenevier, and P. Ashburn, "Reduced boron diffusion under interstitial injection in fluorine implanted silicon," *Journal of Applied Physics*, vol. 102, no. 11, Dec. 2007, doi: 10.1063/1.2822465.
- [55] K. Fujii, K. Kikuta, and T. Kikkawa, "Sub-quarter micron titanium salicide technology with in-situ silicidation using high-temperature sputtering," in 1995 Symposium on VLSI Technology. Digest of Technical Papers, Japan Soc. Appl. Phys, pp. 57–58. doi: 10.1109/VLSIT.1995.520856.
- [56] C. W. Yap, Soh-Yun Siah, E. H. Lim, T. K. Lee, and F. H. Gn, "Fluorine effects on silicidation of BF₂*-implanted narrow poly lines," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference (Cat. No.99EX247)*, IEEE, pp. 38–40. doi: 10.1109/IITC.1999.787071.
- [57] S. Z. M. Saad, T. C. Lik, M. A. Othman, P. Holger, and S. H. Herman, "An improved P+/N diode leakage current in BiCMOS technologies with fluorine co-implant," in 2012 10th IEEE International Conference on Semiconductor Electronics (ICSE), IEEE, Sep. 2012, pp. 690-693. doi: 10.1109/SMElec.2012. 6417237.
- [58] H. Yin et al., "Effect of End-of-Range Defects on Device Leakage in Direct Silicon Bonded (DSB) Technology," in 2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), IEEE, Apr. 2008, pp. 34–35. doi: 10.1109/VTSA.2008.4530786.
- [59] R. R. Robison and M. E. Law, "Fluorine diffusion: models and experiments," in *Digest. International Electron Devices Meeting,* IEEE, pp. 883–886. doi: 10.1109/IEDM.2002.1175978.
- [60] F. Salehuddin, I. Ahmad, F. A. Hamid, A. Zaharim, H. A. Elgomati, and B. Y. Majlis, "Impact of Salicide and Source/Drain Implants on Leakage Current and Sheet Resistance in 45nm NMOS Device," *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol. 2, no. 1, pp. 35–41, Jun. 2010.
- [61] P. D. Agnello, "Process requirements for continued

- scaling of CMOS—the need and prospects for atomic-level manipulation," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 317–338, Mar. 2002, doi: 10.1147/rd.462.0317.
- [62] C.-C. Chenl, Q. F. Wang, F. Jonckx, J.-S. Jenq, and K. Maex, "Ti-Salicide Improvement by Preamorphization for ULSI Applications," *MRS Proceedings*, vol. 402, p. 89, Feb. 1995, doi: 10.1557/PROC-402-89.
- [63] D. C. Kerr, "Method of improving silicide sheet resistance by implanting fluorine," US005994210A, Nov. 30, 1999
- [64] Z. G. Xiao, H. Jiang, J. Honeycutt, C. M. Osburn, G. McGuire, and G. A. Rozgonyi, "TiSi₂ Thin Films Formed on Crystalline and Amorphous Silicon," MRS Proceedings, vol. 181, p. 167, Feb. 1990, doi: 10.1557/PROC-181-167.
- [65] Z. Dezhang, P. Haochang, Z. Fuying, C. Jianqing, and C. Dexin, "Formation of titanium silicide and shallow junctions by BF₂+ implantation and low temperature annealing," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 39, no. 1–4, pp. 288–290, Mar. 1989, doi: 10.1016/0168-583X(89)90789-1.
- [66] Horng Nan Chern, Chung Len Lee, and Tan Fu Lei, "Improvement of polysilicon oxide characteristics by

- fluorine incorporation," *IEEE Electron Device Letters*, vol. 15, no. 5, pp. 181–182, May 1994, doi: 10.1109/55.291593.
- [67] T. Yoshida *et al.*, "Revisited study of fluorine implantation impact on negative bias temperature instability for input/output device of automotive micro controller unit," *Japanese Journal of Applied Physics*, vol. 57, no. 4S, p. 04FD16, Apr. 2018, doi: 10.7567/JJAP.57.04FD16.
- [68] R. E. I. Schropp, "Improved material properties of amorphous silicon from silane by fluorine implantation: Application to thin-film transistors," *Journal of Applied Physics*, vol. 65, no. 9, pp. 3706–3711, May 1989, doi: 10.1063/1.342598.
- [69] K. Nauka, J. Amano, M. P. Scott, E. R. Weber, J. E. Turner, and R. Tsai, "Correlation Between Ti-Silicided Shallow Junction Diode Leakage and Titaniun Diffusion during TiSi₂ Fornation," *MRS Proceedings*, vol. 71, p. 319, Feb. 1986, doi: 10.1557/PROC-71-319.
- [70] D. F. Downey and K. S. Jones, "The role of extended defects on the formation of ultra-shallow junctions in ion implanted ¹¹B+, ⁴⁹BF₂, ⁷⁵As+ and ³¹P+," in *1998 International Conference on Ion Implantation Technology. Proceedings (Cat. No.98EX144)*, IEEE, pp. 897–901. doi: 10.1109/IIT.1998.813813.