International Journal of Nanoelectronics and Materials
IJNeaM
ISSN 1985-5761 | E-ISSN 2232-1535

Design of translinear circuit-based temperature-independent reference current

Alaa H. Mohammed [a], Maizan Muhamad [a] *, Norhafizah Burham [a], and Hanim Hussin [a]

[a]*Faculty of Electrical Engineering, Universiti Teknologi MARA, 40450 Shah Alam, Selangor, Malaysia*
** Corresponding author. Tel.: +60123208217; e-mail: maizan@uitm.edu.my*

Received 29 August 2024, Revised 12 November 2024, Accepted 25 November 2024

ABSTRACT

A reference current, which is widely used to bias analog circuits at an appropriate operating point, is one of the parameters that must remain stable under the temperature changes. This paper aims to design a circuit with a stable reference current over a wide range of temperatures and low power consumption. Since the mobility of carriers in MOS devices is temperature-dependent, the new design uses a translinear principle-based square root circuit in combination with two current source circuits to cancel the thermal effects of the carriers' mobility on the produced current. The square root circuit of the proposed reference current circuit was designed in a 0.1 µm CMOS technology to operate in the weak inversion region to achieve the linear property and guarantee a slight increase in saturation current when the drain-to-source voltage increases. The new approach circuit was designed using the SPICE Multisim simulator where MOS devices with 0.1 µm, 1 µm, and 10 µm process parameters were modeled using virtual components to increase the reference current to a larger value. The simulation results show an output current of 25.06 µA across a temperature range of 0 to 100°C with a temp coefficient of 92ppm/°C and a power consumption of only 1 µW at 1 V supply voltage. Thus, the new approach presented in this paper largely contributes to improving the performance of integrated circuits such as ultra-low-power op-amps.

Keywords: *Reference current, Temperature compensation, Translinear circuit, Temperature coefficient*

1. INTRODUCTION

Access to credible and temperature-independent reference currents is usually an important aspect in the design of integrated circuits. Current references are broadly used in designing analog circuits to provide a suitable operating point for the desired applications. However, the stability of the reference current relies on the stabilities of the voltage source and the resistor used. The optimized solution to provide a constant and temperature-independent bias current is the use of the translinear circuit technique. The translinear circuit is the circuit that performs its function using the translinear principle, where translinearity is the linear dependence of transconductance on the current that occurs in components with the exponential current-voltage relationship. This circuit is a current-mode circuit that can be built by transistors that satisfy an exponential current-voltage characteristic, such as bipolar junction transistors and MOS transistors in weak inversion.

Some of the previous propositions in designing the current references use the complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) currents [1–3]. These propositions have used the method of the sum of CTAT and PTAT currents generated at the resistors across base-to-emitter voltage and the difference base-to-emitter voltage of bipolar junction PNP transistors. Although these topologies have a low sensitivity to the temperature, the temperature coefficient is dependent on the resistors that these circuits are designed with. Therefore, to set the output current value, the resistors should be trimmed to save a zero temperature coefficient.

The most recent propositions in the design of the current sources use a variety of techniques. These techniques include using a β-multiplier circuit, in which only four MOS transistors and two bipolar junction PNP transistors are used in CMOS technology with one trimmed resistor [4]. This circuit was implemented in a 0.35 µm CMOS technology to generate a 16 µA current with a temperature coefficient of 105 ppm/°C over a temperature range from 0 to 110°C. However, a digital calibration circuit is required in this method for trimming the resistor and setting the output current. A reference current circuit, which consumes a power of 1.02 nW, was designed by only PMOS transistors to provide low dependence on temperature and enable trim-free operation [5]. In this circuit, the average temperature coefficient was 282 ppm/°C for a temperature range from −40°C to 120°C, and the generated reference current was 35 nA. However, this method requires an additional circuit for the trimming.

A 10.95 nA reference current circuit has been reported that features a temperature coefficient of 127 ppm/°C over a temperature range from −20 to 120°C [6]. This circuit was implemented in 0.18 µm CMOS technology with an operating voltage of 1.8 V and power consumption of 122 nW. However, this circuit requires an auxiliary circuit to compensate for temperature variations. Amendments to the peaking current reference have been proposed using MOS transistors that operate in the sub-threshold and strong inversion region [7]. In these modifications, the

temperature compensation technique was achieved by adding a source degeneration resistor to the conventional peaking current source structure. This design was simulated in a 0.18 µm process in both weak and strong inversion regions, where the generated output currents were 1.5 µA and 40 µA over a temperature range from −40°C to 100°C. A low-power and high-precision reference voltage and current have been presented in a single simple circuit, where the reference voltage is derived from the threshold voltage difference between the input and output with temperature-independent bias current, and the reference current is the reference voltage divided by a temperature-insensitive resistor [8]. This design was implemented in 0.18 µm CMOS technology, where the value of the reference voltage and current reference at room temperature were 368 mV and 9.77 nA with temperature coefficients of 43.1 ppm/°C for the reference voltage and 149.8 ppm/°C for the reference current, over a temperature range from −40 to 125°C. However, this design requires a resistor made up of a series connection of PTAT resistors, and CTAT resistors in a series.

A method for designing a current source with external electrical references has been proposed to separate the stability of the current source from the noise characteristics of the main power supply [9]. However, in this approach, the current source stability is restricted by the quality of components used in the design, such as the voltage reference chips, resistors, and power supplies. An ultra-low-power reference current circuit based on threshold voltage was reported, which consumes power in a range of pico-watt at 0.5 V supply voltage [10]. This circuit was designed in a 40 nm CMOS technology, where the power consumption was 8.2 pW with a temperature coefficient of 18.6 ppm/°C over a temperature range from 0°C to 85°C. However, it is hard to design a reference current circuit based on threshold voltage with power consumption in the range of pico-watt because the use of a resistor for voltage-to-current conversion requires a very high resistor (in the range of GΩ) to generate a current within pico-ampere range.

A CMOS reference current circuit was presented that operates based on the threshold voltage difference between two same-type NMOS devices, with different channel lengths working in the sub-threshold region for low-power applications [11]. In this circuit, the output current was 11.6 nA and the temperature coefficient was 169 ppm/°C over a temperature range from −40°C to 120°C. The implementation of this design was in 0.18 µm CMOS technology. However, this method of design required temperature-independent resistance. Many researchers have proposed a variety of techniques in the design of temperature-independent reference current circuits, such as ΔVBE-based reference current, smart-bias-based reference current, division-based reference current, and calibration-based reference current [12]. Each of these proposed techniques has restrictions on the stability of the reference current against temperature. A low-power reference voltage and reference current have been reported in one simple circuit for battery-powered applications [13]. In this circuit, the reference voltage was derived from the band-gap topology, and the reference current was gained by summing PTAT current and CTAT current. This design has been implemented in a 0.18 µm CMOS process, where the measured reference voltage and reference current were 1.2 V and 51 nA, with temperature coefficients of 32.7 ppm/°C and 89 ppm/°C respectively, over a temperature range from −45 to 125°C. However, this method required two feedback loops, with two resistors that should be independent of temperature, one is a negative feedback loop, and the other is a positive feedback loop.

An on-chip reference current generator with a fully off-chip resistor has been proposed in 0.18µm CMOS technology [14]. The simulation results have shown that the proposed design has 31% more precision compared to the conventional on-chip reference current generator. This method requires cascade MOS devices with different sizes such that they are closer to the sub-threshold region. Two approaches for self-biased current references have been reported for reducing noise, mismatch, and impact of supply voltage variation and temperature [15]. The first approach consists of a current loop with one linear current mirror, one nonlinear current mirror, and two complementary nonlinear current mirrors. The second approach is designed in a 0.18 µm CMOS technology and consists of multiple nonlinear current mirrors connected in series within a loop. However, this design requires a large number of cascaded MOS devices, resulting in an increase in power consumption. Thus, the new approach presented in this work is effective over a wide range of temperatures (0–100°C) with a lower temp coefficient of 92 ppm/°C and a higher stable output current of 25.06 µA.

2. THE REFERENCE CURRENT CIRCUIT

Since the mobility μ and threshold voltage V_{TH} of the MOS device are functions of the absolute temperature T, where they are related to T by Equations (1) and (2) [16, 17]:

$$\mu(T) = \mu_0 (T/T_0)^{-1.5} \quad (1)$$

$$V_{TH}(T) = V_{TH0} + \alpha_{TH}(T - T_0) \quad (2)$$

where μ_0 is the surface mobility at T_0, T_0 is the absolute temperature measured in Kelvin (273.15°K), V_{TH0} is the threshold voltage at T_0 and α_{TH} is the coefficient of the threshold voltage temperature (–3 mV/°C), the output reference current (I_o) should be independent of these parameters. In this paper, canceling out the effect of these parameters on the current I_o is by using a combination structure from the square root circuit, which is based on the translinear principle with two current source circuits. In one of the current source circuits, the output current (I_1) is directly proportional to the mobility μ, while in the other current source circuit, the output current (I_2) is inversely proportional to the mobility μ, as indicated in Figures 1 and 2.

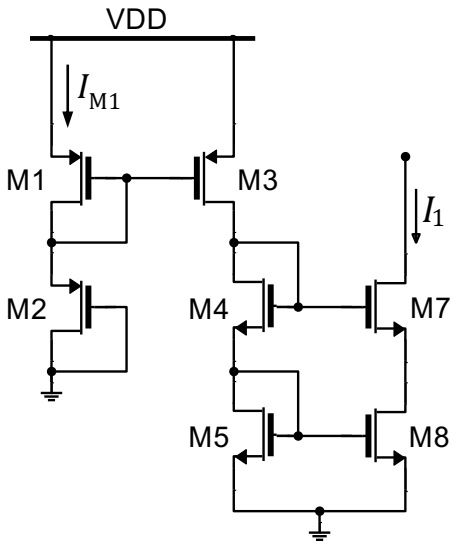

Figure 1. I_1 directly proportional to μ

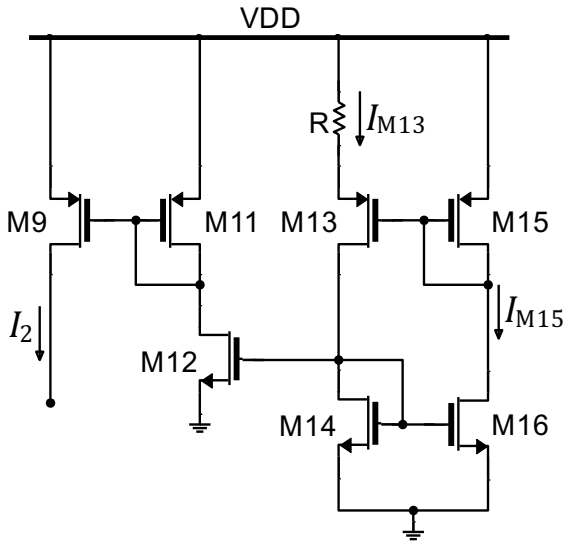

Figure 2. I_2 inversely proportional to μ

In the circuit of Figure 1, the current passing through the PMOS M1 (I_{M1}) is expressed as Equation (3):

$$I_{M1} = \frac{\mu_h c_{ox} \left(\frac{W}{L}\right)_{M1} VDD^2}{2\left(1 + \sqrt{\frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{M2}}}\right)^2} \quad (3)$$

Referring to the circuit in Figure 1, since M1 and M3 act as current mirrors, then $I_{M3} = I_{M1}$. It follows that, since M4, M7, and M5, M8 is also a current mirror, $I_{M1} = I_{M3} = I_1$, that is according to Equation (4):

$$I_1 = \frac{\mu_h c_{ox} \left(\frac{W}{L}\right)_{M1} VDD^2}{2\left(1 + \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}}\right)^2} \quad (4)$$

Thus, in the circuit in Figure 1, I_1 is directly proportional to the surface mobility μ_h. In the circuit in Figure 2, the current passing through the PMOS M13 (I_{M13}) is expressed as Equation (5):

$$I_{M13} = \frac{2\left(1 - \sqrt{\frac{(W/L)_{M15}}{(W/L)_{M13}}}\right)^2}{\mu_h c_{ox} R^2 \left(\frac{W}{L}\right)_{M15}} = I_{M14} \quad (5)$$

Referring to the circuit in Figure 2, since $V_{GS14} = V_{GS12}$, then $I_{M12} = I_{M14}$. It follows that, since M9 and M11 acting as current mirror,

$$I_{M14} = I_2 \quad (6)$$

Thus, from Equation (5),

$$I_2 = \frac{2\left(1 - \sqrt{\frac{(W/L)_{M15}}{(W/L)_{M13}}}\right)^2}{\mu_h c_{ox} R^2 (W/L)_{M15}} \quad (7)$$

Thus, Equation (7) states that I_2 is inversely proportional to μ_h in the circuit in Figure 2.

To cancel out the effect of the surface mobility, μ_h, which is a function of the absolute temperature T, the square root circuit is used. The work idea of the square root circuit is based on the translinear principle (TLP). TLP states that in the loop containing an even number of translinear elements (TEs) that only goes through voltage connections of TEs arranged in a clockwise (CW) and counterclockwise (CCW), the product of the currents through the CW TEs is equal to the product of the currents through the CCW TEs. TEs are the elements that obey the exponential current-voltage relationship, such as the MOS devices that operate in the sub-threshold region (weak inversion). Thus, the translinear MOS devices follow the following relationship as in Equation (8):

$$I = I_0 e^{V/V_T} \quad (8)$$

where I_0 is a pre-exponential current that has a relationship with the device dimensions and V_T is the thermal voltage. Based on TLP, the loop that only goes through the voltage connections of TEs is a translinear loop, where in this loop, because the voltage around the loop that goes from the V connections that follow CW to the V connections that follow CCW must be zero,

$$\sum_{CW} V_i = \sum_{CCW} V_i \quad (9)$$

From Equation (8):

$$V = V_T \ln\left(\frac{I}{I_0}\right) \quad (10)$$

Thus, based on Equation (10), in the translinear loop that has an even number of translinear elements arranged in a CW and CCW:

$$\sum_{\mathrm{CW}} \ln\left(\frac{I_i}{I_{0i}}\right) = \sum_{\mathrm{CCW}} \ln\left(\frac{I_i}{I_{0i}}\right) \tag{11}$$

From Equation (11), by using the natural logarithm properties:

$$\prod_{\mathrm{CW}} \left(\frac{I_i}{I_{0i}}\right) = \prod_{\mathrm{CCW}} \left(\frac{I_i}{I_{0i}}\right) \tag{12}$$

In a MOS transistor that operates in the weak inversion region, where $V_{GS} < V_{TH}$, the drain current I_{ST}, which is the sub-threshold leakage current, is given by the Equation (13) [19]:

$$I_{\mathrm{ST}} \approx \alpha \left(\frac{W}{L}\right) e^{(V_{\mathrm{GS}}-V_{\mathrm{TH}})/\eta V_T} \tag{13}$$

where $\alpha = \mu c_{ox} (V_T)^2 (\eta-1)$, μ is the surface mobility of NMOS or PMOS device, and η is a coefficient that depends on the doping concentration of the MOS device. Hence, from Equation (13):

$$V_{\mathrm{GS}} = \eta V_T \ln\left[\frac{I_{\mathrm{ST}}}{\alpha(W/L)}\right] + V_{\mathrm{TH}} \tag{14}$$

Thus, based on the TLP, if the loop contains an even number of MOS devices that function as TEs and connected only through VGS connections, then, the V_{GSi} summation with clockwise and counterclockwise are equal, that is:

$$\sum_{\mathrm{CW}} V_{\mathrm{GS}i} = \sum_{\mathrm{CCW}} V_{\mathrm{GS}i} \tag{15}$$

Substituting Equation (14) in (15) gives:

$$\sum_{\mathrm{CW}} \ln\left[\frac{I_{\mathrm{ST}i}}{\alpha(W/L)_{\mathrm{M}i}}\right] = \sum_{\mathrm{CCW}} \ln\left[\frac{I_{\mathrm{ST}i}}{\alpha(W/L)_{\mathrm{M}i}}\right] \tag{16}$$

Or, by using natural logarithm properties:

$$\ln\left[\prod_{\mathrm{CW}} \frac{I_{\mathrm{ST}i}}{\alpha\left(\frac{W}{L}\right)_{\mathrm{M}i}}\right] = \ln\left[\prod_{\mathrm{CCW}} \frac{I_{\mathrm{ST}i}}{\alpha\left(\frac{W}{L}\right)_{\mathrm{M}i}}\right] \tag{17}$$

It follows that:

$$\prod_{\mathrm{CW}} \frac{I_{\mathrm{ST}i}}{(W/L)_{\mathrm{M}i}} = \prod_{\mathrm{CCW}} \frac{I_{\mathrm{ST}i}}{(W/L)_{\mathrm{M}i}} \tag{18}$$

Hence, the circuit topology that achieves the TLP using the MOS devices with 0.1 µm technology is shown in Figure 3.

It is observed from the topology of the circuit shown in Figure 3 that the loop is passing only through V_{SG} connections, where V_{SG6} and V_{SG10} of M6 and M10 are CW, while V_{SG17} and V_{SG18} of the MOS transistor M17 and the MOS transistor M18 are CCW. Therefore, based on Equation (18),

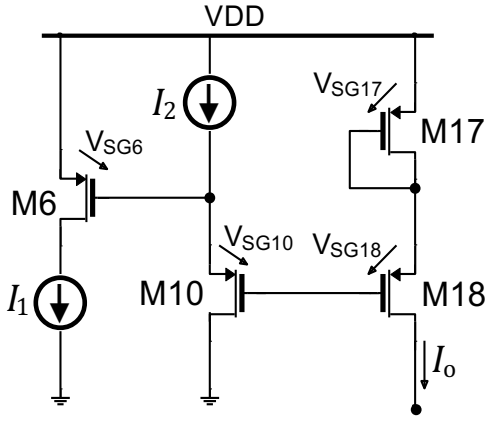

Figure 3. Circuit topology that achieves the TLP

$$\prod_{i=6,10} \frac{I_{\mathrm{ST}i}}{\left(\frac{W}{L}\right)_{\mathrm{M}i}} = \prod_{i=17,18} \frac{I_{\mathrm{ST}i}}{\left(\frac{W}{L}\right)_{\mathrm{M}i}} \tag{19}$$

Or, since $I_{ST6} = I_1$, $I_{ST10} = I_2$ and $I_{ST17} = I_{ST18} = I_o$,

$$\frac{I_1 I_2}{(W/L)_{\mathrm{M6}}(W/L)_{\mathrm{M10}}} = \frac{I_o^2}{(W/L)_{\mathrm{M17}}(W/L)_{\mathrm{M18}}} \tag{20}$$

Thus, from Equation (20), the output current I_o of the proposed reference current is,

$$I_o = \sqrt{\frac{(W/L)_{\mathrm{M17}}(W/L)_{\mathrm{M18}}}{(W/L)_{\mathrm{M6}}(W/L)_{\mathrm{M10}}}}\sqrt{I_1 I_2} \tag{21}$$

Equation (21) indicates the interaction between the circuit of the translinear principle and current sources shown in Figures 1 and 2 by canceling the effect of temp-dependent μ_h by multiplying the currents I_1 and I_2 described by Equations (4) and (7). Thus, substituting Equations (4) and (7) in Equation (21) gives the temp-independent output current of the proposed reference current circuit as:

$$I_o = \frac{\sqrt{\beta_1\beta_2}\left(1-\sqrt{\beta_3}\right)\mathrm{VDD}}{\left[\mathrm{R}\left(1+\sqrt{\beta_4}\right)\right]} \tag{22}$$

Where:

$$\beta_1 = \frac{(W/L)_{\mathrm{M17}}(W/L)_{\mathrm{M18}}}{(W/L)_{\mathrm{M6}}(W/L)_{\mathrm{M10}}} \tag{23}$$

$$\beta_2 = (W/L)_{\mathrm{M1}}/(W/L)_{\mathrm{M15}} \tag{24}$$

$$\beta_3 = (W/L)_{\mathrm{M15}}/(W/L)_{\mathrm{M13}} \tag{25}$$

$$\beta_4 = (W/L)_{\mathrm{M1}}/(W/L)_{\mathrm{M2}} \tag{26}$$

Thus, the complete proposed circuit of the temperature-independent reference current is shown in Figure 4.

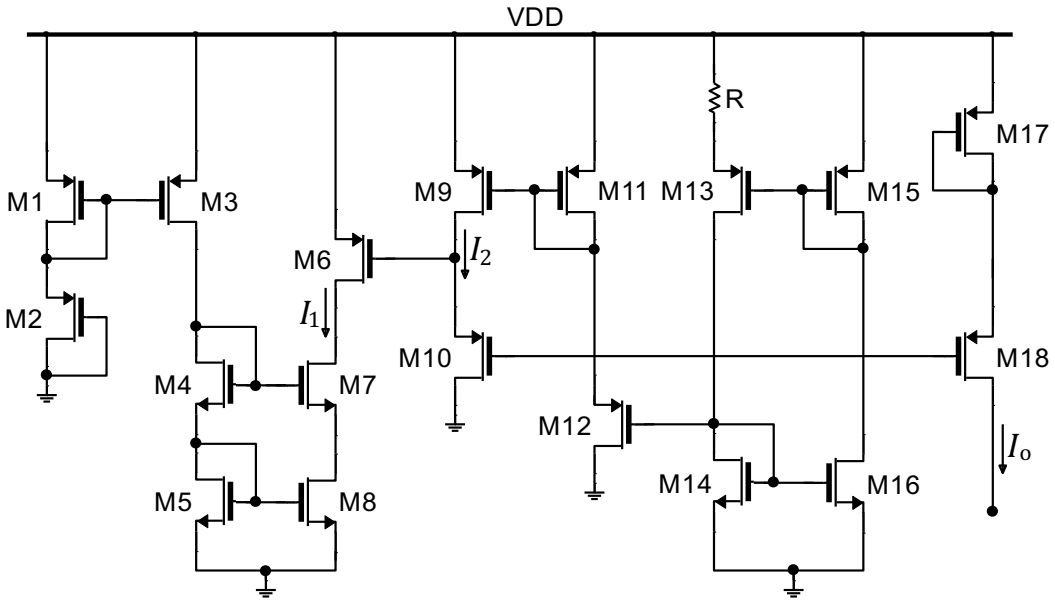

Figure 4. The proposed circuit of the temperature-independent reference current

In this work, the ratios of β used are $\beta_1 = \beta_2 = 1$ and $\beta_3 = \beta_4 = 0.01$, and, for the temperature coefficient of resistance to be insignificant, the value of the resistor R was chosen to be 100 kΩ. Table 1 lists the sizes and types of the MOS transistors used in the design of the proposed reference current circuit.

Table 1. Sizes and types of the MOS transistors used in the design of the reference current circuit

Device Name	Type	W/L (μm/μm)
M1, M15	PMOS	1/10
M2, M13	PMOS	10/1
M3, M6, M9, M10, M11, M17, M18	PMOS	1/0.1
M4, M5, M7, M8, M12, M14, M16	NMOS	1/0.1

3. THE RESULTS

3.1. Output Current vs. Temperature

Figure 5 shows the output current vs. Temperature. In this aspect of the simulation, the reference current circuit was tested over a temperature range from 0 to 100°C. The output current over this range of temperature has been varied from 25.06 µA to 24.83 µA with a temperature coefficient of 92 ppm/°C. So, the change is only 0.23 µA. This means that the output current is stable against fluctuations in temperature. This insignificant change is due to the temperature coefficient (TC) of the resistor R which is 20 ppm/°C. However, for more accuracy, a binary-weighted trimming circuit can be used for the resistor R to cancel out the effect of the resistance's TC. In contrast, using the binary-weighted trimming circuit for the resistor R will complicate the design and increase the consumption of power.

3.2. Output Voltage vs. Temperature

Figure 6 shows the output voltage of the proposed reference current circuit versus the temperature in Celsius degrees.

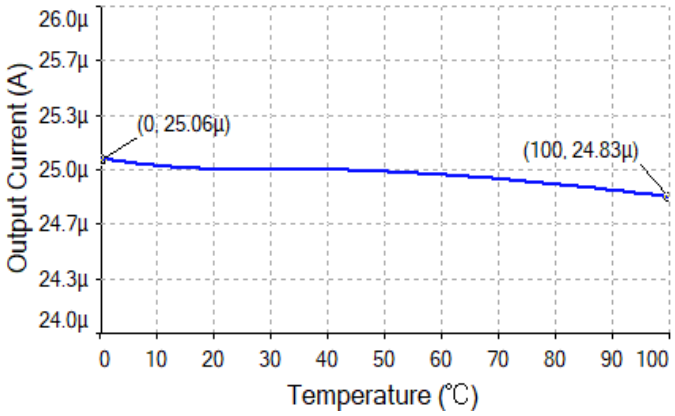

Figure 5. Output current of the proposed reference current circuit vs. temperature

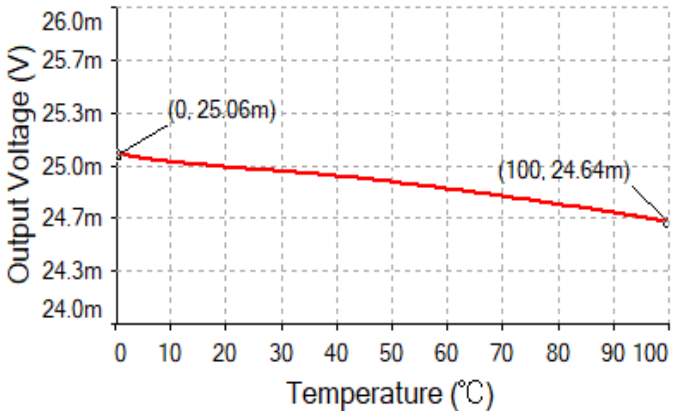

Figure 6. Output voltage of the proposed reference current circuit vs. the temperature

In this test, the change in the output voltage across the chosen temperature range was only 0.42 mV. This slight deviation in the output voltage is due to the TC of the resistor R. However, the transient analysis of the output voltage versus the temperature change reported stability with no change during the time as shown in Figure 7.

3.3. Output Current vs. the Change in VDD

Figure 8 shows the output current of the proposed circuit versus the change in the voltage supply VDD.As indicated in Figure 8, the output current of the proposed design changes exponentially with changes in the supply voltage. This type of change is due to the use of the translinear circuit. Thus, the proposed reference current in this paper is significantly sensitive to variations in supply voltage. Table 2 represents a comparison between the best results of the previous propositions and this work.

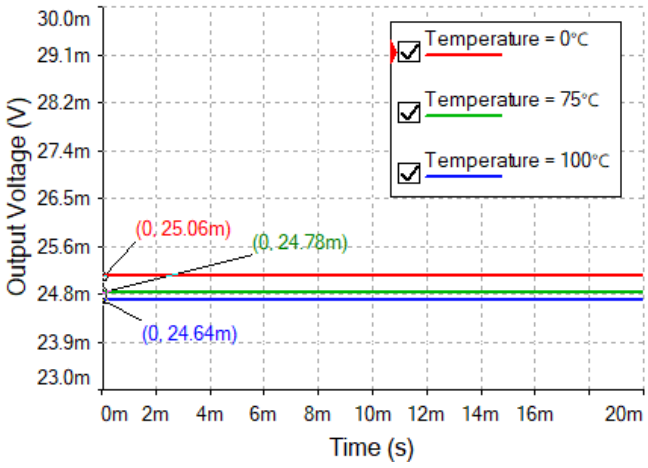

Figure 7. Transient analysis of the output voltage vs. the temperature change

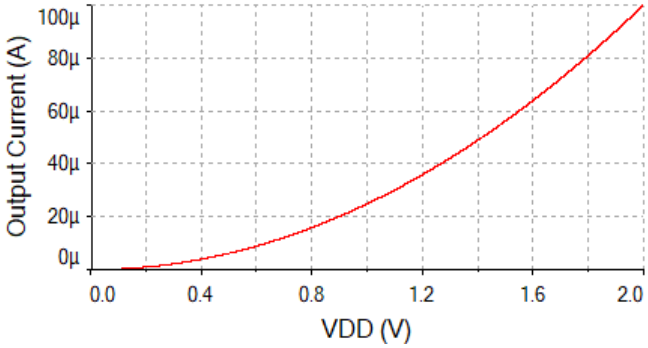

Figure 8. Output current of the proposed reference current circuit vs. the change in the voltage supply

4. CONCLUSIONS

The circuit topology presented in this paper offers an operating of stable current and voltage reference over a wide range of temperatures. The test results show that the proposed circuit of the reference current is suitable for low-power applications, especially for ultra-low-power op-amps. In this circuit, temperature stability of the output current achieved by only one-time trimming of the temperature coefficient. This can reduce fabrication costs and minimize power consumption.

ACKNOWLEDGMENTS

This research was supported by the Fundamental Research Grant Scheme (FRGS: FRGS/1/2024/TK07/UITM/02/18), Ministry of Higher Education (MOHE). We gratefully thank the College of Engineering, Universiti Teknologi MARA, for helping in this work.

REFERENCES

[1] C. Zhao, R. Geiger, and D. Chen, "A compact low-power supply-insensitive CMOS current reference," in *2012 IEEE International Symposium on Circuits and Systems*, IEEE, May 2012, pp. 2825–2828. doi: 10.1109/ISCAS.2012.6271899.

[2] Y.-T. Wang, D. Chen, and R. L. Geiger, "A CMOS supply-insensitive with 13ppm/°C temperature coefficient current reference," in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, IEEE, Aug. 2014, pp. 475–478. doi: 10.1109/MWSCAS.2014.6908455.

[3] C. Wu, W. L. Goh, C. L. Kok, W. Yang, and L. Siek, "A low TC, supply independent and process compensated current reference," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, IEEE, Sep. 2015, pp. 1–4. doi: 10.1109/CICC.2015.7338488.

[4] D. Osipov and S. Paul, "Temperature-Compensated β-Multiplier Current Reference Circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1162–1166, Oct. 2017, doi: 10.1109/TCSII.2016.2634779.

[5] Q. Dong, I. Lee, K. Yang, D. Blaauw, and D. Sylvester,

Table 2. A Comparison between the best results of the previous propositions and this work

Ref.	Tech. (µm)	TC (ppm/°C)	I_o (A)	Temp. range (°C)	VDD (V)
[4]	0.35	105	16 µ	0 to 110	3
[5]	0.18	282	35 n	–40 to 120	2
[6]	0.018	127	11 n	–20 to 12	1.8
[7]	0.18	571	1.5 µ	–40 to 100	1.8
[8]	0.18	149	9.7 µ	–40 to 125	3
[10]	0.13	18.6	2.4 p	0 to 85	0.5
[11]	0.18	169	10.6 n	–40 to 120	2
This work	0.1	92	25.06 µ	0 to 100	1

"A 1.02nW PMOS-only, trim-free current reference with 282ppm/°C from −40°C to 120°C and 1.6% within-wafer inaccuracy," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, IEEE, Sep. 2017, pp. 19–22. doi: 10.1109/ESSCIRC.2017.8094515.

[6] D. Cordova, A. C. de Oliveira, P. Toledo, H. Klimach, S. Bampi, and E. Fabris, "A sub-1 V, nanopower, ZTC based zero-VT temperature-compensated current reference," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, IEEE, May 2017, pp. 1–4. doi: 10.1109/ISCAS.2017.8050289.

[7] M. S. Eslampanah Sendi, S. Kananian, M. Sharifkhani, and A. M. Sodagar, "Temperature Compensation in CMOS Peaking Current References," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1139–1143, Sep. 2018, doi: 10.1109/TCSII.2018.2805832.

[8] L. Wang and C. Zhan, "A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3457–3466, Sep. 2019, doi: 10.1109/TCSI.2019.2927240.

[9] I. Fan *et al.*, "Externally Referenced Current Source with Stability Down to 1 nA/A at 50 mA," *IEEE Transactions on Instrumentation and Measurement*, vol. 68, no. 6, pp. 2129–2135, Jun. 2019, doi: 10.1109/TIM.2018.2885502.

[10] H. Zhuang, J. Guo, C. Tong, X. Peng, and H. Tang, "A 8.2-pW 2.4-pA Current Reference Operating at 0.5 V With No Amplifiers or Resistors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1204–1208, Jul. 2020, doi: 10.1109/TCSII.2019.2936874.

[11] Q. Huang, C. Zhan, L. Wang, Z. Li, and Q. Pan, "A −40°C to 120°C, 169 ppm/°C Nano-Ampere CMOS Current Reference," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 9, pp. 1494–1498, Sep. 2020, doi: 10.1109/TCSII.2020.3009838.

[12] S. Lee and E. Sánchez-Sinencio, "Current Reference Circuits: A Tutorial," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 830–836, Mar. 2021, doi: 10.1109/TCSII.2021.3049518.

[13] W. Huang, L. Liu, and Z. Zhu, "A Sub-200nW All-in-One Bandgap Voltage and Current Reference Without Amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 121–125, Jan. 2021, doi: 10.1109/TCSII.2020.3007195.

[14] M. Shahghasemi and K. M. Odame, "A Constant g_m Current Reference Generator with Pseudo Resistor-Based Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 3, pp. 1115–1124, Mar. 2022, doi: 10.1109/TCSI.2021.3123279.

[15] D. Veit and J. Oehm, "A Current Reference with Multiple Nonlinear Current Mirrors to Reduce Noise, Mismatch, and Impact of Supply Voltage Variation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 5, pp. 1729–1733, May 2023, doi: 10.1109/TCSII.2023.3260164.

[16] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS: Circuit Design, Layout, and Simulation*. New York: IEEE Press, 1998.

[17] Y. Tsividis, *Operation and modeling of the MOS transistor*. New York: McGraw-Hill, 1987.

[18] W. Liu *et al.*, "Chapter 2: Physics-Based Derivation of I-V Model," in *BSIM3v3.2.2 MOSFET Model Users' Manual*, Berkeley, CA: The Regents of the University of California, 1999, pp. 21–240.

[19] "Sub Threshold Current." [Online]. Available: https://asic-soc.blogspot.com/2008/04/sub-threshold-current.html