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Temperature Characterization and Performance Enhancement of a 7nm FinFET Structure Using HK Materials and GaAs as Metal Gate (MG)

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ABSTRACT

The progress in semiconductor technology has played a crucial role in enhancing human existence by introducing significant innovations. The pursuit of high-performance devices utilizing novel materials has emerged as a crucial avenue for surmounting the existing limitations of silicon-based technologies. This paper presents an evaluation of the diverse short channel effects (SCEs) exhibited by the double gate n-FinFET structure, considering the influence of temperature on channel materials using metal gate (MG) as Gallium Arsenide (GaAs) alongside High-K dielectric oxide materials such as Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3) and Lanthanum Aluminum Oxide ($LaAlO_3$) in comparison with traditional Silicon Dioxide (SiO_2). The investigation and presentation of the impact of gate length (L_g), channel width (W_{ch}), doping, and varying Temperature (275k-450k) on several short channel effects (SCEs), namely Drain Induced Barrier Lowering (DIBL), Subthreshold Slope (SS), threshold voltage (V_{th}) roll-off, Transconductance (g_m) and ON-OFF current ratio (I_{ON} / I_{OFF}) have been thoroughly examined using the aforementioned materials. The utilization of FinFET technology using HK-MG presents notable benefits in terms of mitigating the subthreshold swing while concurrently maintaining a low drain-induced barrier lowering (DIBL) effect.

Keywords: *Short channel effects, DIBL, Transconductance, Threshold voltage, Subthreshold swing, ON-OFF current ratio*

1. BACKGROUND

The process of scaling Metal Oxide Semiconductor Field Effect Transistors (MOSFET) has yielded a substantial increase in device density per wafer, consequently resulting in a remarkable reduction in the cost per chip [1]. The transition from the era of microelectronics to the emerging era of nanoelectronics will not only facilitate the widespread integration of electronic components, enabling their miniaturization and cost reduction to the extent that they can be incorporated into virtually any object, including dissolvable and wearable products [2], [3]. The downsizing of transistors, resulting from device scaling, also brings forth additional advantages. Specifically, the reduction in the size of interconnects diminishes the distance that electrons must traverse, thereby decreasing resistance along the path. Consequently, this reduction in resistance leads to improvements in circuit delays, power consumption, and speed [4]. Typically, when the channel length reaches a comparable scale to the depletion-layer widths of the source and drain, a MOSFET device is deemed to be in a state of brevity, leading to the emergence of what is commonly referred to as short-channel effects (SCEs). It is a widely accepted principle to prioritize the effective gate length, ensuring it exceeds the thickness of the dielectric oxide region by a factor of no less than 40 (L_g>40*T_{ox}) [5]. This would impose additional constraints on the scalability within the nanoscale domain. In order to address this inherent constraint, researchers have devised a strategy involving the utilization of high-k Dielectric (HK) oxide materials in conjunction with metal gate (MG) for advanced / non-planar field-effect transistor (FET) structures like FinFETs [6]–[9].

The covalent bonds exhibited by elements belonging to group III-IV are indeed captivating constituents of the two-dimensional (2D) materials class [10]. These elements namely Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3), and Lanthanum Aluminum Oxide ($LaAlO_3$) with dielectric constants of k=24, 25, and 30 respectively possess remarkable attributes such as sleek surfaces, free of dangling bonds and an atomic thinness that is truly remarkable [11], [12]. Consequently, devices predicated upon these materials exhibit notable electron mobility and substantial ON/OFF current ratios [13]. In the context of HK dielectrics exhibiting elevated oxygen diffusivities at elevated temperatures, it is reasonable to anticipate the occurrence of rapid oxygen diffusion through the oxides when subjected to annealing processes accompanied by an excessive abundance of oxygen [14]. The assessment of mobility serves as a pivotal parameter in the evaluation of a HK dielectric as a viable substitute for SiO_2 [15], [16]. The aforementioned approach holds significant influence over various transistor metrics, including but not limited to saturation drain current ($I_{d(sat)}$), switching speed, threshold voltage (V_{th}), transconductance (g_m), Drain Induced Barrier

Lowering (DIBL), and subthreshold swing (SS) [3]. The employment of FinFET technology with HK-MG offers a number of advantages, the most significant of which is the reduction of the subthreshold swing, which is accomplished while simultaneously keeping the DIBL impact at a low level [17], [18].

This study investigates the impact of temperature on a GaAs FinFET device [10], [18], incorporating ultrathin HfO_2, La_2O_3, and $LaAlO_3$ layers, operating at the 7nm technology node. The ongoing investigation pertains to the identification of the most optimal candidate when compared to traditional SiO2, specifically in terms of SCEs. The device was meticulously designed using predictive technology modeling (PTM) [19] and subjected to simulations across a temperature range spanning from 275k to 450k [20]. The structural arrangement of the paper is delineated as follows: Section 2 expounds upon the intricate architecture of non-planar FinFETs. Section 3 elucidates the simulation setup, wherein a comprehensive examination is conducted on the methodologies and models employed to simulate the devices utilizing the HK-MG approach. Within Section 4, an in-depth exploration is conducted on the evaluation of transfer performance. This evaluation encompasses five distinct parameters, namely SS, Saturation Drain Current ($I_{d(sat)}$), g_m, V_{th}, DIBL, and the current ratio I_{ON} / I_{OFF}. Ultimately, the culminating observations are delineated within the conclusion and future scope section.

2. NON-PLANAR FINFET ARCHITECTURE INCORPORATING HK-MG MATERIALS

The figure presented in Figure 1 showcases the three-dimensional bird's eye view of the non-planar FinFET with high-k spacer technology architectures selected for this study [1], [17]. It comprises various parameters, including the gate length, L_g (also known as the channel length), the fin width, W_{ch} (alternatively referred to as the channel width or fin thickness), and other pertinent features as illustrated in Figure 1 and Table 1. The vertical dimension of the fin, denoted as H, is utilized in FinFETs to enable enhanced gate control via the implementation of a relatively thicker Oxide Thickness (T_{ox}) on the fin structure. Moreover, the oxide is strategically positioned on both lateral aspects of the fin's side walls and the uppermost surface of the fin, preceding the establishment of the gate contact. The specification of the thickness of the side wall oxide is denoted by the variables T_{ox1} and T_{ox2}. FinFETs are advanced field-effect transistors that possess three distinct gates. Among these gates, the third gate is specifically attributed to the small segment that extends over the top of the fin structure. The nomenclature denoting the length of the source and drain regions is commonly designated as L_s and L_d respectively. Furthermore, the overlapping of the source and drain regions is conventionally symbolized by O_s and O_d. The aforementioned structural parameters are visually depicted in Figure 1 and its device modeling parameters using predictive technology modeling (ptm) are expressed in Table 1.; the template arranges everything for you in a user-friendly.

The FinFET, with its vertical thin channel, provides substantial manipulation of SCEs and electrostatic parameters, while also exhibiting a reduced level of fabrication intricacy when compared to the MOSFET [21]. The primary aim of this endeavor is to establish equitably proportioned underlap regions on either side of the channel, specifically towards the source/drain. These regions will then be adorned with three distinct dielectric spacer materials, namely HfO2 with a dielectric constant of 24, La_2O_3 with a dielectric constant of 25, and $LaAlO_3$ with a dielectric constant of 30. Next, we proceed to analyze the advantages and disadvantages pertaining to the operational capabilities of the devised apparatus employing GaAs as MG and distinct HK materials, in contrast to the conventional SiO_2 FinFET. The gate wrapped structure assumes the responsibility of augmenting gate control and bestowing superior electrical control over the channel, thereby mitigating the leakage current and subduing the short channel effects (SCEs). Furthermore, it is worth noting that the FinFET structure serves the purpose of eliminating the conventional practice of channel doping, thereby mitigating the adverse effects associated with threshold voltage fluctuation. In contrast to silicon (Si), SiO_2 exhibits a thermal conductivity that is diminished by two orders of magnitude, thereby compromising the operational efficiency of the device. The phenomenon referred to is commonly known as the self-heating effect [3], [21].

The material used for the gate and dielectric layer has undergone significant evolution, transitioning from a polysilicon gate with a silicon dioxide dielectric layer to a more advanced configuration featuring a metal gate combined with an HK dielectric layer. As the process node continues to decrease in size, the utilization of HK dielectric

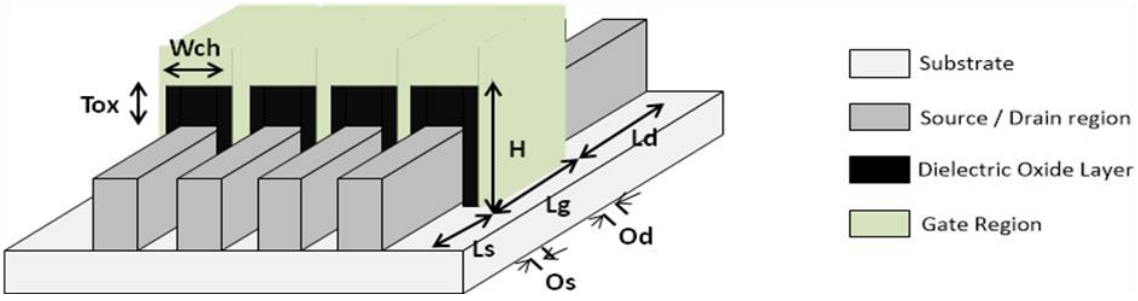


Figure 1. FinFET Device Structure

Table 1. 7nm FinFET Device parameters

Parameter	Value
Channel Length (L_g)	15nm
Channel Width (W_{ch})	7nm
Channel Height (H)	18nm
Oxide Thickness or thickness of the fin (t_{ox} / t_{fin})	6.5nm
Source or Drain Length (L_s or L_d)	2nm
Source or Drain Overlap to Gate (O_s or O_d)	0.2nnm
Source or Drain Doping concentration	3.00E+26 cm-3
Channel Doping	2.86.00E+25 cm-3
Gate Voltage (V_g)	0.7V
Temperature (in Kelvin)	275k to 450k
Drain Voltage (V_d)	0.01 – 0.69V
HK Oxide Material	Hafnium Oxide (HfO_2) Lanthanum Oxide (La_2O_3) Lanthanum Aluminum Oxide ($LaAlO_3$)
Metal Gate Material	Gallium Arsenide (GaAs)

materials such as HfO_2, La_2O_3, and $LaAlO_3$ has proven to be efficacious in augmenting the gate oxide capacitance and mitigating the gate leakage that arises from the thinning of the SiO_2 layer. The substitution of polysilicon with metal gates presents a viable solution to mitigate the polysilicon depletion effect, thereby enhancing carrier mobility through a more optimal integration of HK dielectric materials. The source and drain regions are comprised of a heavily doped layer of Gallium Arsenide (GaAs) in order to minimize contact resistance. The gate strip traverses the slender GaAs fin, thereby giving rise to the resulting three-dimensional (3D) FinFET architecture.

3. EVALUATION AND ANALYSIS OF TRANSFER PERFORMANCE

It is unequivocally imperative that the primary pivotal prerequisite pertains to the 'k' value followed by the bandgap (eV). The requisite altitude should possess a sufficient elevation to ensure economic viability for a substantial quantity of scaling nodes. The requisite 'k' of the MG ought to exceed 12 while the value of 'k' should ideally fall within the range of 25 to 30 for the HK oxide material. Nevertheless, it should be noted that excessively higher 'k' values can result in the undesirable occurrence of a potent fringing field extending from the gate to the source/drain regions. The presence of fringing fields induces additional electric fields from the source/drain to the channel, thereby diminishing the efficacy of gate control and compromising performance by extravagating short-channel effects. On the other hand, the HK material should possess a bandgap of not less than 5eV. The primary aim of device scaling is to engender the development of diminutive yet expeditious devices. The attainment of high velocity necessitates a corresponding elevation in the magnitude of the source-drain current, a parameter that is intrinsically contingent upon carrier mobility. The evaluation of mobility plays a crucial role in assessing the viability of a high-k dielectric as a potential replacement for SiO_2. These material characteristics exert a substantial impact on a multitude of performance metrics. The parameters of interest in FinFETs, namely the saturation current ($I_{d(sat)}$), threshold voltage (V_{th}) roll-off, Transconductance (g_m) and ON-OFF current ratio (I_{ON} / I_{OFF}), drain-induced barrier lowering (DIBL), and sub-threshold swing (SS) exhibit significant sensitivity to variations in temperature. Typically, these performance parameters exhibit a negative correlation with rising temperatures. This phenomenon can be attributed to a multitude of factors as illustrated below:

a) *Diminishment of Mobility*: It is a well-established phenomenon that the mobility of carriers tends to diminish as the temperature rises. This can be attributed to the heightened occurrence of scattering events and interactions with phonons. Moreover, the reduction in mobility can be attributed to amplified lattice vibrations and intensified phonon interactions occurring at elevated temperatures. This, in turn, affects the performance parameters.
b) *Variation in Channel Resistance*: The resistance exhibited by the channel region in the FinFET is subject to alteration in response to temperature fluctuations, primarily attributed to heightened scattering phenomena and lattice vibrations. Increased channel resistance has the potential to impede the passage of electric current, thereby exerting a detrimental effect on the overall performance metrics.
c) *Doping Effects*: The influence of temperature on the doping concentration and distribution within the FinFET structure can have discernible effects on the transfer performance. Modifications in doping profiles have the potential to induce variations in the depletion region, carrier concentration, and mobility, consequently exerting an influence on the fundamental traits of the transistor.
d) *Increased Thermal Generation*: The phenomenon of increased thermal generation occurs when the ambient temperature rises, leading to heightened production of electron-hole pairs within the device. The drain current is influenced by the presence of thermally generated carriers. Nevertheless, the consequences of heightened thermal generation are eclipsed by the decline in carrier mobility, leading to a comprehensive diminution in the saturation drain current as well as other performance metrics.

There exists a pressing necessity to optimize these parameters in order to surpass the constraints imposed by temperature dependencies. The attainment of this optimization is realized through the utilization of the HK-MG FinFET Structure meticulously crafted for the 7nm technology node. The graphical representation of the fluctuations in performance metrics in relation to temperature can be observed in Figure 2 for DIBL, g_m, SS, V_{th}, and $I_{d(sat)}$. Also, Table 2 illustrates the variation of I_{ON}/I_{Off} for various HK materials varied over a temperature range.

If the ratio between the ON-current (I_{ON}) and the OFF-current (I_{OFF}) in a FinFET exhibits a negative correlation with temperature, it indicates a decline in the device's capacity to sustain a substantial I_{ON} in comparison to I_{OFF} as the temperature escalates. This conduct denotes a decline in operational efficacy and energy conservation capabilities when subjected to elevated temperatures. Based on the data presented in Table 2, it becomes apparent that the high-k (HK) materials HfO_2 and La_2O_3 do not exhibit superior performance compared to SiO_2 material. However, it is noteworthy that the $LaAlO_3$ material shows promising potential to surpass SiO_2, with a significant improvement of approximately 1.28E+04 at ambient temperature (t=300K) and approximately 5.58E+02 at a higher temperature of t=450K. The I_{ON} / I_{OFF} current ratio serves as a quantitative assessment of the ratio between the ON-current (I_{ON}) and the OFF-current (I_{OFF}), thereby assuming a pivotal role in the evaluation of their performance attributes. A superior I_{ON}/I_{OFF} ratio denotes enhanced device performance and heightened power efficiency, manifesting in accelerated switching speed, elevated noise margin, and superior transistor scaling capabilities.

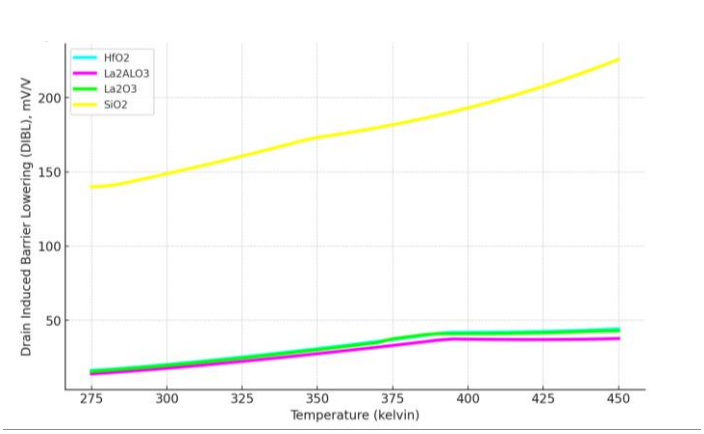
If one were to observe the phenomenon of Drain-Induced Barrier Lowering (DIBL) in a FinFET, it would be noted that the extent of this effect is directly proportional to the rise in temperature. Consequently, as the temperature increases, the impact of the drain voltage on the reduction of the threshold voltage becomes more prominent. This observed phenomenon suggests that the device's vulnerability to Drain-Induced Barrier Lowering (DIBL) is amplified under elevated temperature conditions. A rise in Drain Induced Barrier Lowering (DIBL) in conjunction with temperature variations signifies a diminishment in the efficacy of channel control, a surge in leakage current, a shift in threshold voltage, an influence on subthreshold behavior, as well as an effect on power dissipation and efficiency. Based on the analysis of Figure 2 (a), it is apparent that the traditional SiO_2 material exhibits a more pronounced Drain-Induced Barrier Lowering (DIBL) variation in response to temperature fluctuations, whereas the HK materials demonstrate a comparatively more consistent slope. Thereby, indicating a notable enhancement in the FinFET's performance.

If the transconductance (g_m) of a FinFET exhibits a positive correlation with temperature, it implies that the device's efficacy in converting alterations in input voltage into corresponding modifications in output current is enhanced with escalating temperatures. The phenomenon of transconductance exhibiting an upward trend in response to temperature variations can be ascribed to a multitude of contributing factors, including but not limited to the augmentation of amplification capabilities, the bolstering of carrier mobility, the mitigation of scattering effects, and the refinement of gate control mechanisms. Upon careful examination of Figure 2 (b), it becomes evident that the conventional SiO_2 material showcases a diminished variation in the transconductance (g_m) when subjected to changes in temperature. Conversely, the HK materials exhibit a relatively more pronounced and consistent slope in this regard. Henceforth, this observation denotes a conspicuous amelioration in efficacy.

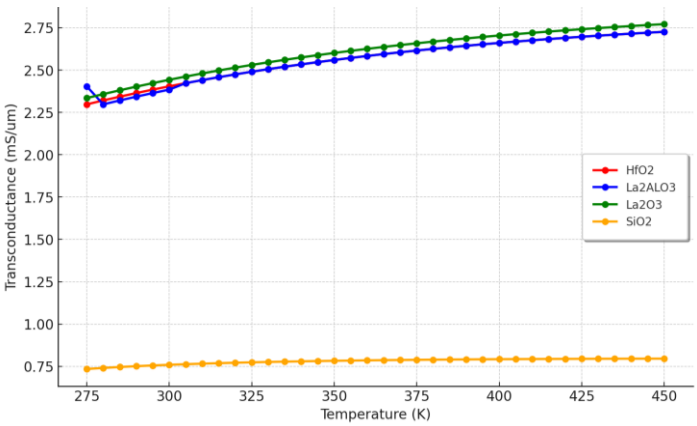
In the event that the subthreshold swing (SS) of a FinFET exhibits an upward trend in response to elevated temperatures, it can be inferred that the device's capacity to effectively govern the transistor's operation within the subthreshold region experiences a decline concomitant with rising temperatures. The observed behavior implies that the subthreshold swing demonstrates a positive temperature coefficient. The manifestation of an elevated subthreshold swing in a FinFET device signifies a diminished efficacy in regulating the flow of current within the subthreshold region. The subthreshold swing can be

Table 2. Variation of I_{ON} / I_{OFF} for various HK materials varied over a temperature range

Temp. (k)	ION / IOFF Ratio			
	SiO_2	HfO_2	La_2O_3	$LaAlO_3$
275	8.93E+10	1.58E+09	5.74E+06	2.67E+15
280	6.99E+10	1.04E+09	3.71E+06	1.74E+15
285	5.51E+10	6.94E+08	2.44E+06	1.15E+15
290	4.39E+10	4.7E+08	1.62E+06	7.75E+14
295	3.51E+10	3.23E+08	1.09E+06	5.28E+14
300	2.84E+10	2.24E+08	7.47E+05	3.64E+14
305	2.31E+10	1.57E+08	5.16E+05	2.54E+14
310	1.89E+10	1.12E+08	3.61E+05	1.79E+14
315	1.55E+10	80395878	2.55E+05	1.28E+14
320	1.29E+10	58347147	1.82E+05	9.22E+13
325	1.07E+10	42759053	1.32E+05	6.71E+13
330	8.97E+09	31627821	9.58E+04	4.93E+13
335	7.55E+09	23602846	7.05E+04	3.66E+13
340	6.39E+09	17764164	5.22E+04	2.74E+13
345	5.43E+09	13478819	3.91E+04	2.07E+13
350	4.64E+09	10307088	2.94E+04	1.57E+13
355	3.98E+09	7940645	2.24E+04	1.2E+13
360	3.43E+09	6161376	1.71E+04	9.29E+12
365	2.97E+09	4813663	1.32E+04	7.22E+12
370	2.58E+09	3785561	1.02E+04	5.65E+12
375	2.25E+09	2995906	7.99E+03	4.45E+12
380	1.97E+09	2385406	6.28E+03	3.53E+12
385	1.73E+09	1910430	4.96E+03	2.81E+12
390	1.52E+09	1538643	3.95E+03	2.26E+12
395	1.34E+09	1245923	3.15E+03	1.82E+12
400	1.19E+09	1014154	2.54E+03	1.47E+12
405	1.06E+09	829646.4	2.05E+03	1.2E+12
410	9.46E+08	681993.3	1.66E+03	9.83E+11
415	8.46E+08	563235.5	1.36E+03	8.09E+11
420	7.59E+08	467252.2	1.11E+03	6.68E+11
425	6.83E+08	389310.5	9.16E+02	5.55E+11
430	6.16E+08	325731.1	7.58E+02	4.63E+11
435	5.57E+08	273639.5	6.29E+02	3.87E+11
440	5.04E+08	230778.7	5.24E+02	3.25E+11
445	4.58E+08	195368	4.39E+02	2.75E+11



(a)



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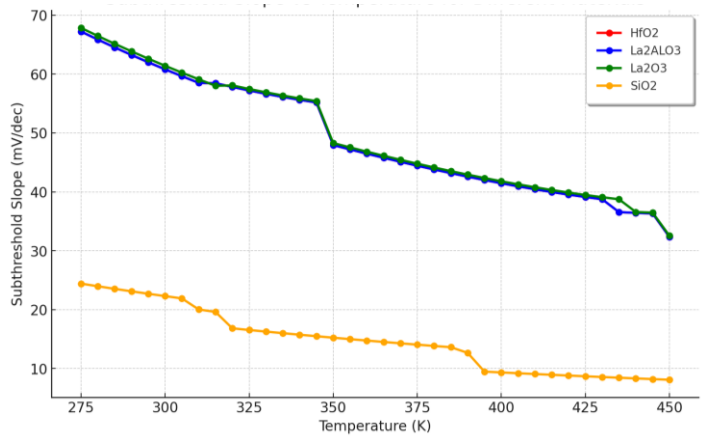

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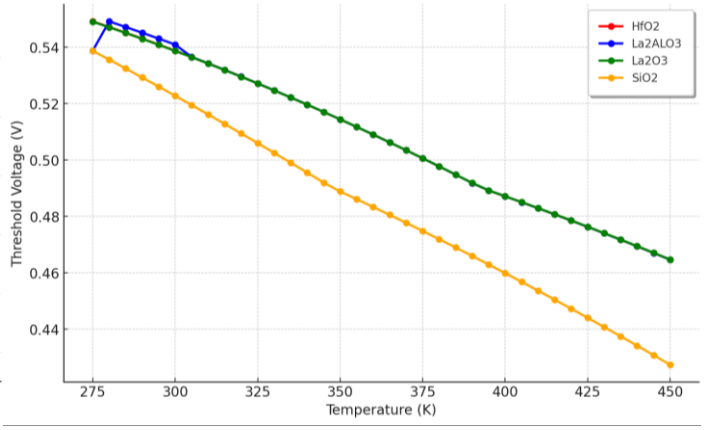
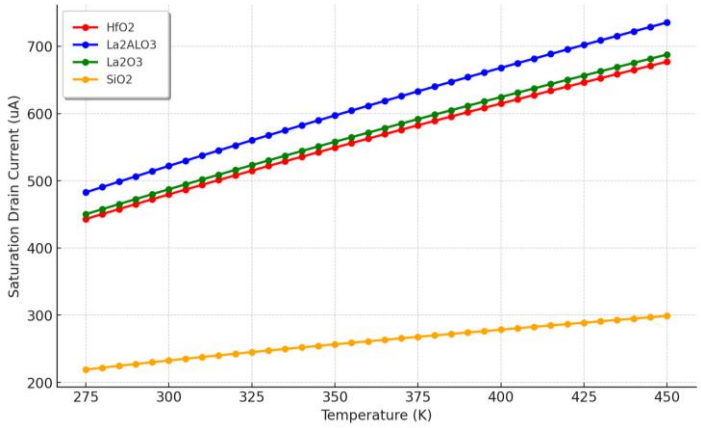


(d)



(e)

Figure 2. Performance metrics (a) DIBL, (b) g_m, (c) SS, (d) V_{th}, and (e) $I_{d(sat)}$

defined as a quantitative assessment of the rate at which the drain current undergoes variations in response to alterations in the gate voltage within the subthreshold domain. This particular domain refers to the operational state of the transistor wherein it exhibits feeble conduction or remains in an inactive state. An increase in SS alongside temperature fluctuations indicates a reduction in the efficiency of the weakly conducting region, leading to implications for power consumption, limitations in sensitivity and precision, as well as variations in threshold voltage. Based on the analysis of Figure 2(c), it is apparent that the traditional SiO_2 material exhibits a more pronounced SS variation in response to temperature fluctuations along with its higher value, whereas the HK materials demonstrate a comparatively more consistent slope alongside maintaining a smaller value. Hence, indicating a notable enhancement in the FinFETs performance.

In the event that the threshold voltage (V_{th}) of a FinFET exhibits a negative temperature coefficient, it implies that the operational voltage necessary to activate the transistor diminishes concomitantly with escalating temperature levels. The observed behavior implies that the threshold voltage demonstrates a negative temperature coefficient. A reduction in the threshold voltage as a function of temperature indicates an augmentation in conductivity and an amplification in the current drive. The presence of a

negative temperature coefficient in the threshold voltage of a transistor signifies an increased susceptibility of the transistor's behavior to variations in temperature. A reduced threshold voltage facilitates the activation of the transistor, thereby leading to a heightened capacity for current conduction. The aforementioned characteristic can prove to be advantageous in scenarios where there is a need for high-performance or high-speed operation. This is due to the fact that it facilitates expedited switching and enables a greater current output. The reduction of the threshold voltage can indeed augment the conductivity of the transistor. However, it is important to note that this adjustment may also result in an elevation of the leakage current, particularly within the subthreshold region. Based on the results of Figure 2(d), it is evident that the conventional SiO_2 material displays a smaller variation in threshold voltage in response to changes in temperature, but the HK materials present a somewhat less steep slope. This observation suggests a significant improvement in the performance of FinFETs.

The saturation drain current ($I_{d(sat)}$) is a parameter that characterizes the upper limit of current conduction within a transistor when it is fully activated and functioning within the saturation region. The observed phenomenon of an augmented $I_{d(sat)}$ in response to temperature variations suggests a heightened conductivity of the transistor as temperature levels rise. The utilization of this approach can prove to be advantageous in various applications that necessitate a greater current drive, such as power amplifiers or circuits that require high-performance capabilities. Furthermore, it is worth noting that there exists a positive correlation between the $I_{d(sat)}$ and temperature, which consequently results in an elevation of power dissipation within the transistor. As the magnitude of the electric current passing through the device intensifies, a commensurate augmentation in power consumption occurs, thereby engendering a collateral escalation in thermal energy production. The aforementioned issue may arise in scenarios where the optimization of power efficiency and the effective management of thermal conditions are of utmost importance. The gain characteristics of amplification circuits may be influenced by the temperature-dependent increase in saturation drain current, thereby exerting an influence on the comprehensive performance of the circuit. Based on the results of Figure 2(e), it is evident that the conventional SiO_2 material displays a smaller saturation drain current in response to changes in temperature, but the HK materials present a better $I_{d(sat)}$. This observation suggests a significant improvement in the performance of FinFETs.

Table 3 presents the simulation metrics pertaining to the utilization of 7nm FinFET technology, in juxtaposition with the prevailing state-of-the-art methodologies. The Group III-V elements exhibit comparatively elevated I_{ON} and diminished I_{OFF} values in relation to the Group III-IV elements when considering gate lengths of similar magnitude. This disparity is crucial in effectively managing I_{OFF} and attaining enhanced performance. The primary impetus behind the transition to FinFET technology at gate lengths below 14nm stemmed from the pronounced manifestation of I_{OFF}in planar devices. It has been observed that FinFET architecture offers superior suppression of short-channel effects (SCE), reduced switching times, and increased current density. Controlling the dynamic threshold voltage (V_{th}) to mitigate the associated high capacitances presents a considerable challenge, thereby resulting in escalated fabrication expenses.

4. CONCLUSION

In conclusion, it can be inferred that FinFET devices present a notable improvement in the management of short channel effects (SCEs) when juxtaposed with conventional planar MOSFETs. The mitigation of SCEs is facilitated by the incorporation of fin-shaped channels within the three-dimensional architecture of FinFETs utilizing the HK-MG approach. A comprehensive grasp of the temperature dependency of Drain-Induced Barrier Lowering (DIBL), Transconductance, Subthreshold Swing, and threshold voltage is of utmost importance in the realm of designing resilient and dependable circuits based on FinFET technology. Through careful consideration of the implications and meticulous optimization of device design and fabrication processes, researchers possess the ability to harness the temperature-dependent. By doing so, they can effectively attain the desired performance, power efficiency, and reliability across a diverse range of temperature conditions. It is imperative to acknowledge that the temperature-dependent characteristics of saturation drain current exhibit variability contingent upon device parameters, process technologies, and operational circumstances. The characterization of the distinct behavior exhibited by FinFETs across varying temperature scenarios, along with the subsequent implementation of suitable design considerations, assumes paramount significance in the pursuit of attaining device operation that is both reliable and high-performing. However, the requirement for ongoing reduction in the size of transistors below the 7nm technology node is a formidable challenge that necessitates the development of novel structures like Gate All Around (GAA) FET in order to enhance gate control.

Table 3. State of art comparison

Reference	HK	MG	L_g (nm)	V_{th} (V)	g_m (mS/um)	DIBL (mV/V)	SS (mV/dec)	I_{ON} (uA/um)	I_{OFF} (nA/um)	I_{ON} / I_{OFF}
[22]	SiO_2	AuSb	14	-	-	75	80	-	-	-
[17]	SiO_2	Si_3N_4	16	0.24	-	50	72	292	7.5	38,933
[13]	Al_2O_3	GaN	10	0.2	0.49	-	-	1.43	-	-
[23]	SiO_2	GaAs	16	0.47	-	380	95	-	-	-
This Work	$LaAlO_3$	GaAs	7	0.42	2.3	20	70	690	3.88	177,835

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